

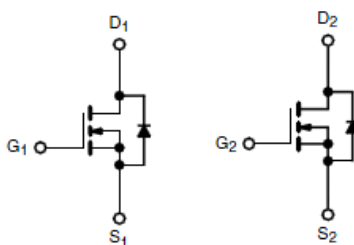
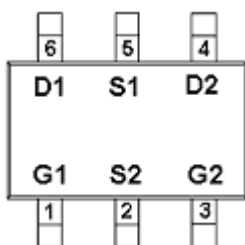
General Description

AFN6810W, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge. These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 100V/2.3A, $R_{DS(ON)}=310m\Omega@V_{GS}=10V$
100V/1.8A, $R_{DS(ON)}=320m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TSOP-6 package design

Pin Description (TSOP-6)



Application

- Power Management in Note book
- LED Display
- DC-DC System
- LCD Panel

Pin Define

Pin	Symbol	Description
1	G1	Gate 1
2	S2	Source 2
3	G2	Gate 2
4	D2	Drain 2
5	S1	Source 1
6	D1	Drain1

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN6810WTS6RG	N10YW	TSOP-6	Tape & Reel	3000 EA

- ※ N10 parts code
- ※ Y year code (0 ~ 9)
- ※ W week code (A ~ Z = 1 ~ 26 / a ~ z = 27 ~ 52)
- ※ AFN6810WTS6RG : 7" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	2.3
		T _A =70°C	1.8
Pulsed Drain Current	I _{DM}	4	A
Continuous Source Current(Diode Conduction)	I _S	1.5	A
Power Dissipation	P _D	T _A =25°C	2.0
		T _A =70°C	1.3
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	120	°C/W

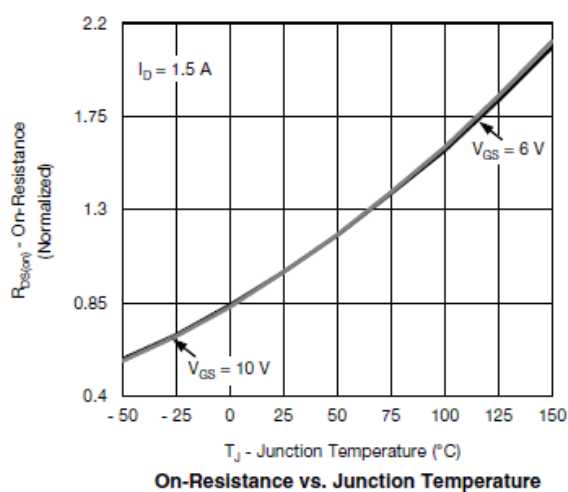
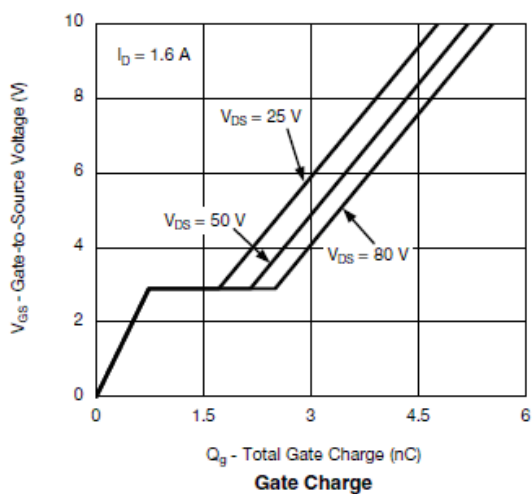
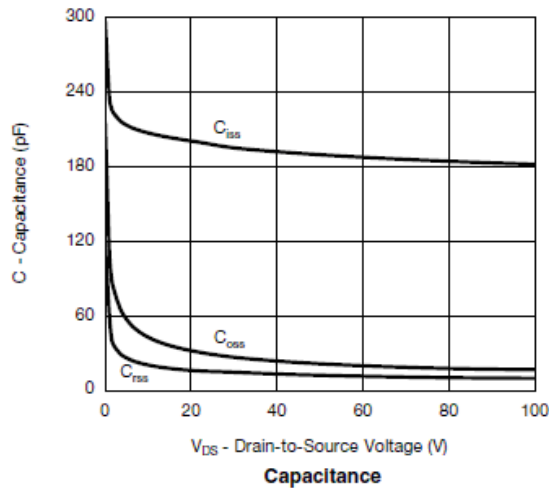
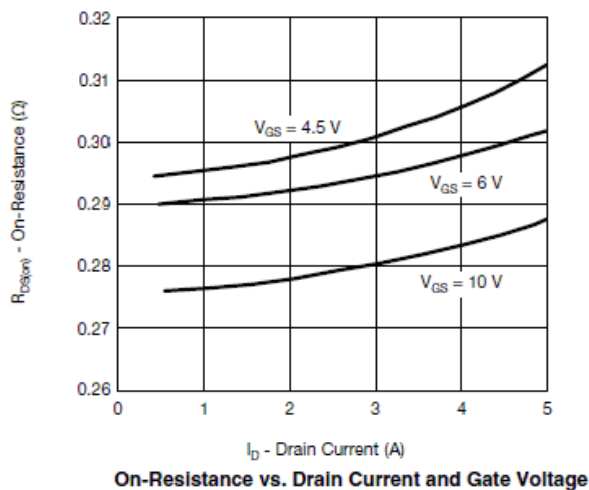
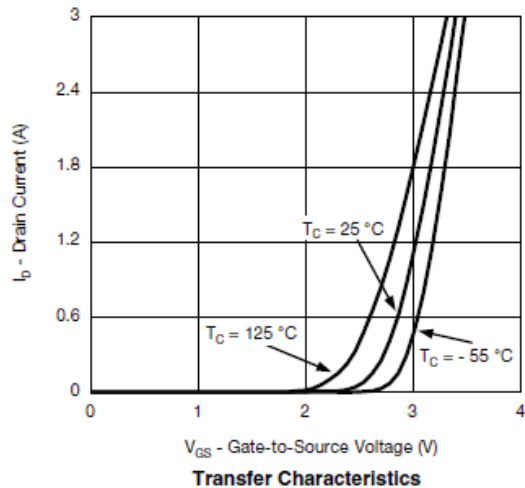
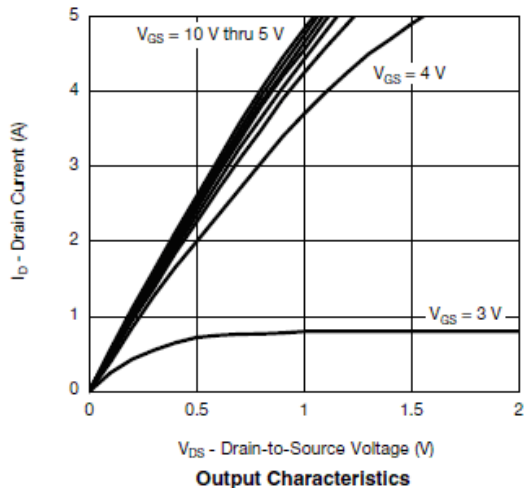
Electrical Characteristics

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0		2.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V			1	uA
		V _{DS} =80V, V _{GS} =0V T _J =85°C			10	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =4.5V	5			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.3A		270	310	mΩ
		V _{GS} =4.5V, I _D =1.8A		290	320	
Forward Transconductance	g _{FS}	V _{DS} =20V, I _D =1.5A		2		S
Diode Forward Voltage	V _{SD}	I _S =1.3A, V _{GS} =0V		0.85	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =50V, V _{GS} =4.5V I _D ≅1.6A		2.8	5.8	nC
Gate-Source Charge	Q _{gs}			0.75		
Gate-Drain Charge	Q _{gd}			1.4		
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V f=1MHz		200		pF
Output Capacitance	C _{oss}			22		
Reverse Transfer Capacitance	C _{rss}			13		
Turn-On Time	t _{d(on)}	V _{DD} =50V, R _L =39Ω I _D ≅1.3A, V _{GEN} =4.5V R _G =1Ω		25	50	ns
	t _r			20	50	
Turn-Off Time	t _{d(off)}			15	30	
	t _f			10	25	

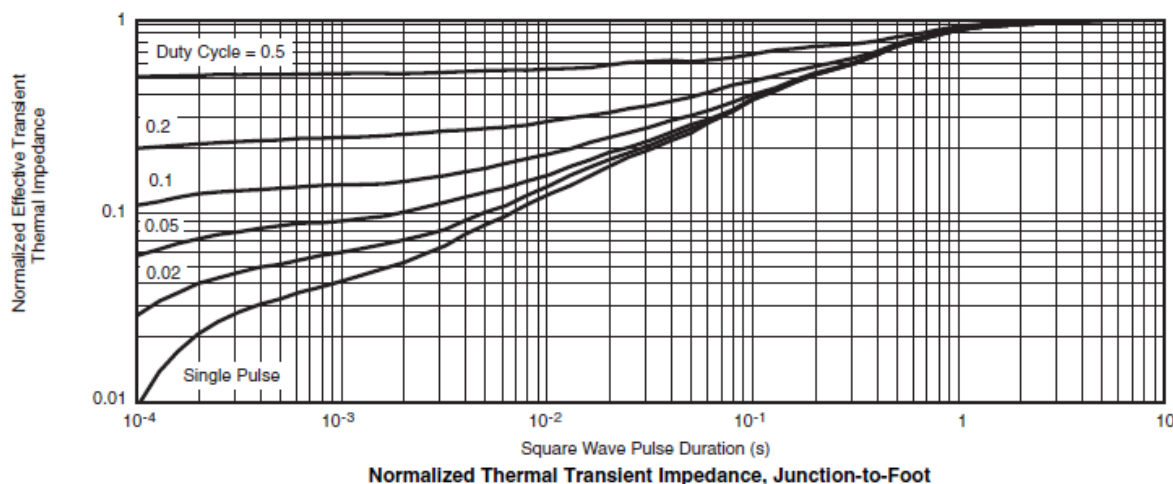
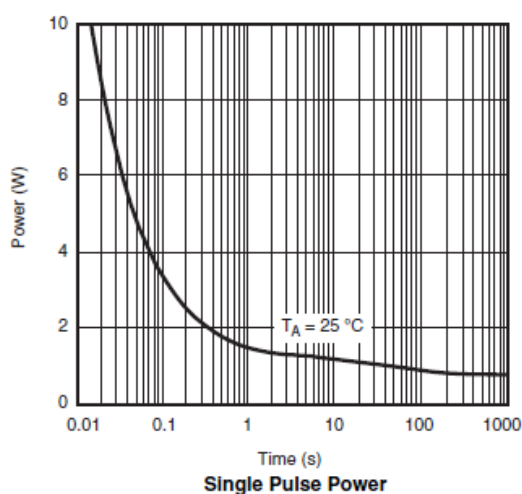
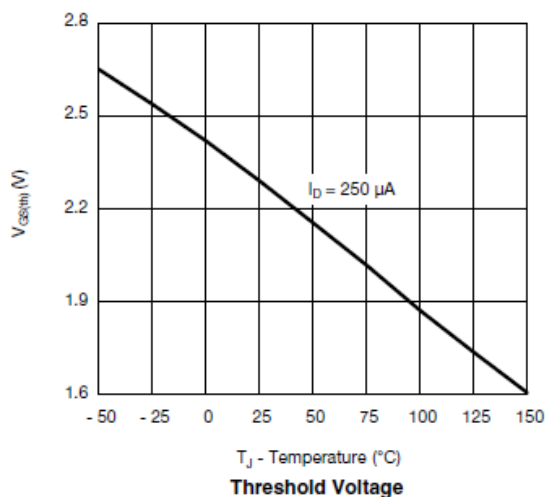
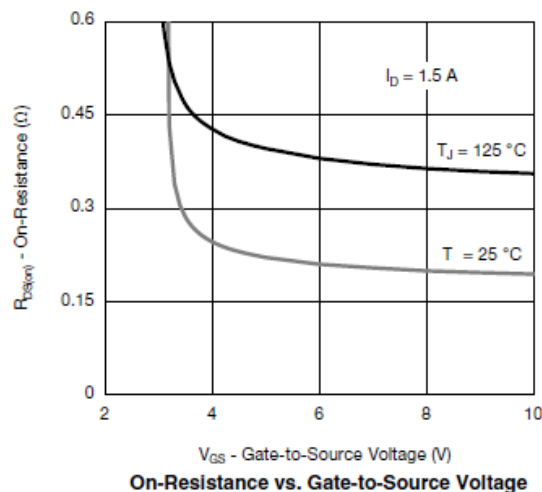
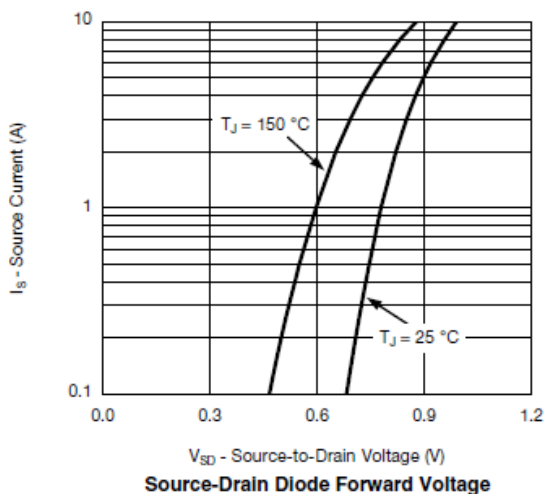


Typical Characteristics





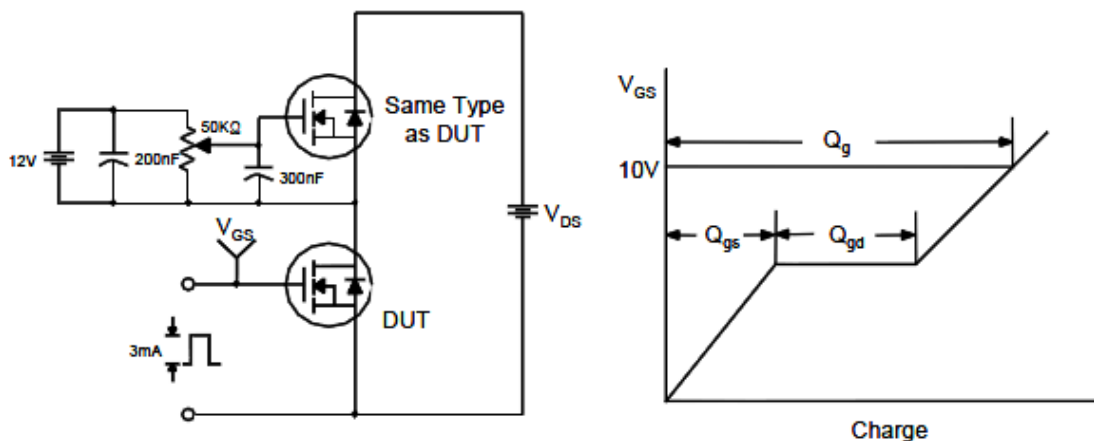
Typical Characteristics



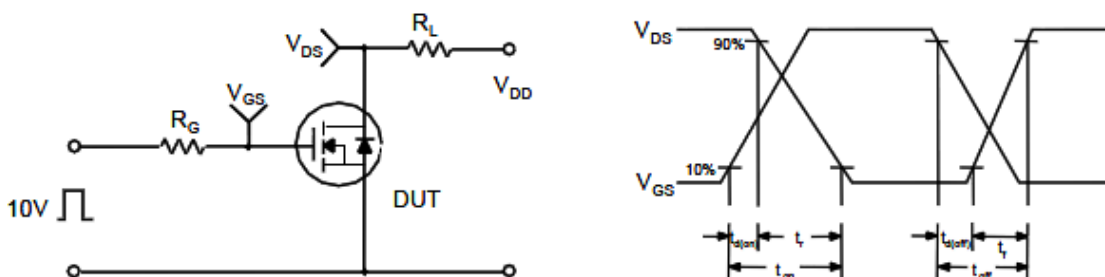


Typical Characteristics

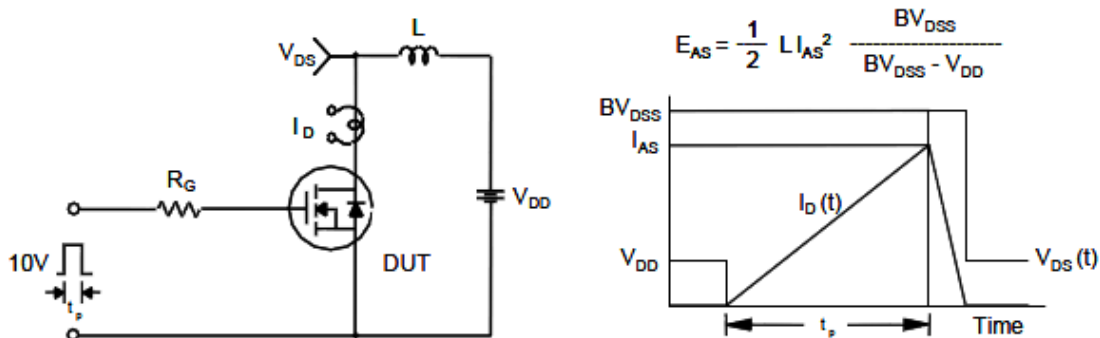
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

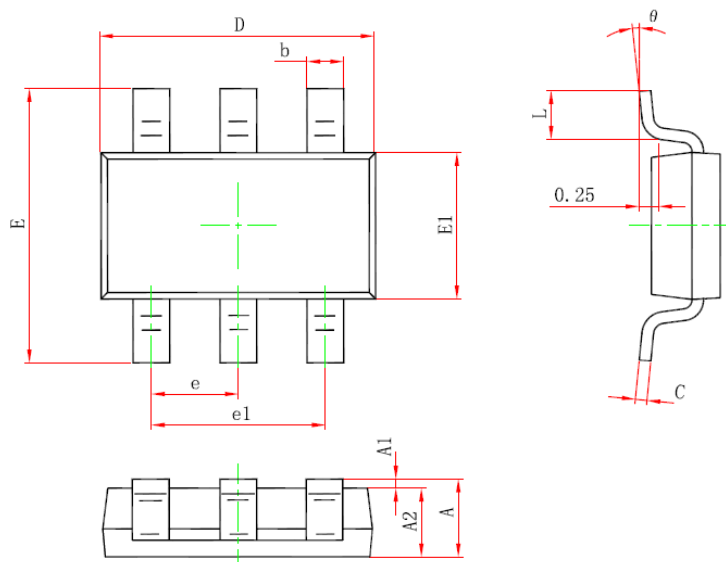


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (TSOP-6)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	---	0.900	---	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E1	1.600	1.700	0.063	0.067
E	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037(BSC)	
e1	1.90 (BSC)		0.075(BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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