Alfa-MOS Technology

AFN6870S

100V N-Channel Enhancement Mode MOSFET

General Description

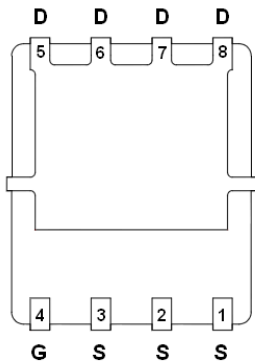
AFN6870S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

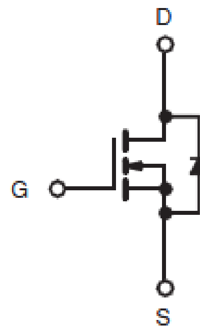
These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

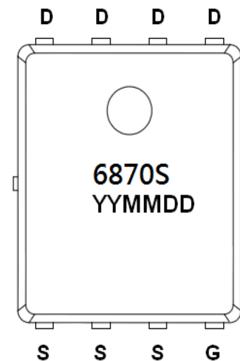
Features

- 100V/20A,$R_{DS(ON)}$=6.0mΩ@V_{GS}=10V
- 100V/15A,$R_{DS(ON)}$=8.0mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS (ON)}$
- DFN5X6-8L package design

Pin Description (DFN5X6-8L)







Application

- Networking / Telecom / Server
- LED Lighting Applications
- Quick Charger Applications
- DC-DC Primary Side Switch

Pin Define

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN6870SFN568RG	6870S	DFN5X6-8L	Tape & Reel	2500 EA

※ 6870S : Parts Code
※ YYMMDD : Date Code
※ AFN6870SFN568RG : 13”Tape & Reel ; Pb- Free ; Halogen- Free

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Absolute Maximum Ratings

(T_A=25℃ Unless otherwise noted)

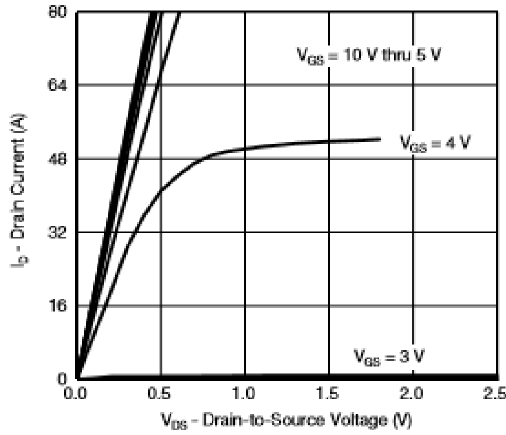
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	+20/-12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_{DSM}	24	A
	T_A=70℃		18	
Pulsed Drain Current		I_{DM}	280	
Continuous Source Current(Diode Conduction)	T_A=25℃	I_S	5.6	
Single Pulse Avalanche Current	L=0.1mH	I_{AS}	40	
		E_{AS}	80	mJ
Power Dissipation	T_A=25℃	P_D	6.25	W
	T_A=75℃		4.0	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient	t ≤ 10 s	$R_{\theta JA}$	15	℃/W
Maximum Junction-to-Case (Drain)	Steady-State	$R_{\theta JA}$	0.9	

Electrical Characteristics

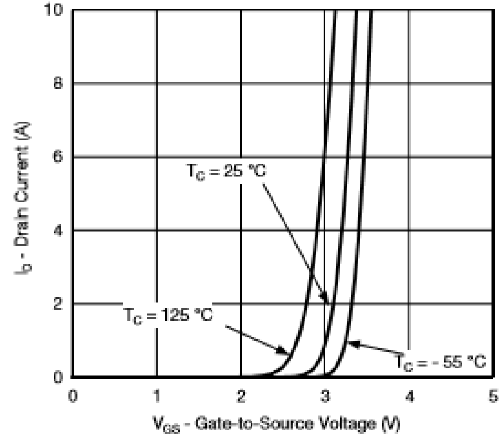
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0	1.6	2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=85℃			10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧5V,V_{GS}=10V	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		4.82	6.0	mΩ
		V_{GS}=4.5V,I_D=15A		6.72	8.0	
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A		68		S
Diode Forward Voltage	V_{SD}	I_S=5A,V_{GS}=0V		0.75	1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=4.5V I_D≡20A		25	50	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			10		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		2860		pF
Output Capacitance	C_{oss}			720		
Reverse Transfer Capacitance	C_{rss}			70		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=2.5Ω I_D≡20A,V_{GEN}=10V R_G=1Ω		15	30	ns
	t_r			15	30	
Turn-Off Time	$t_{d(off)}$			35	70	
	t_f			10	20	

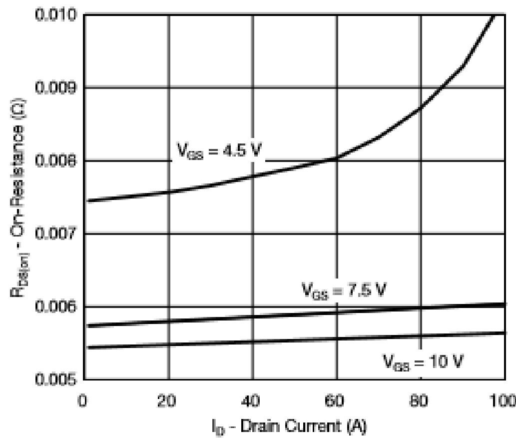
Typical Characteristics



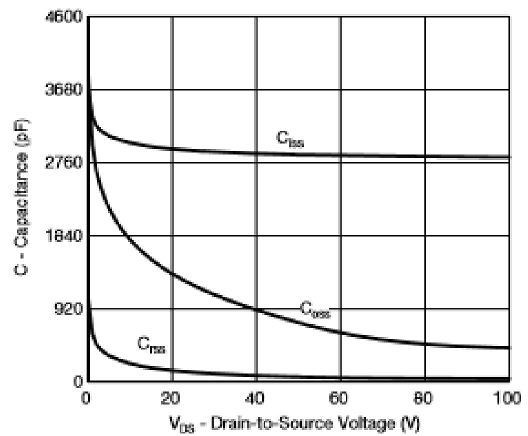
Output Characteristics



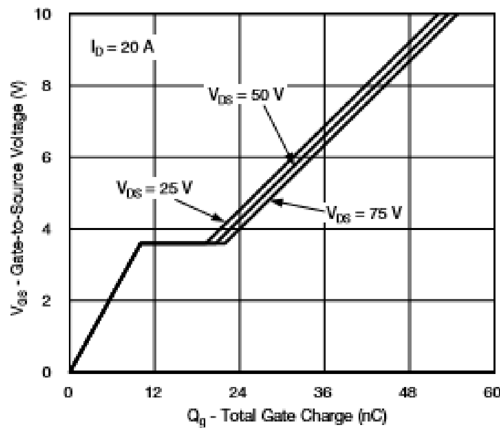
Transfer Characteristics



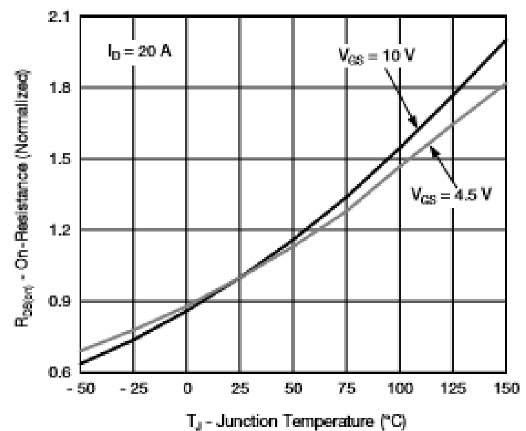
On-Resistance vs. Drain Current



Capacitance

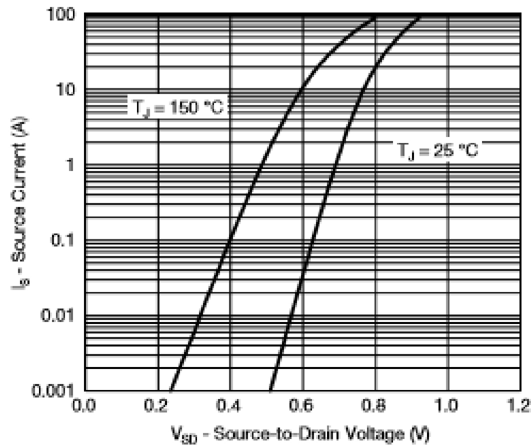


Gate Charge

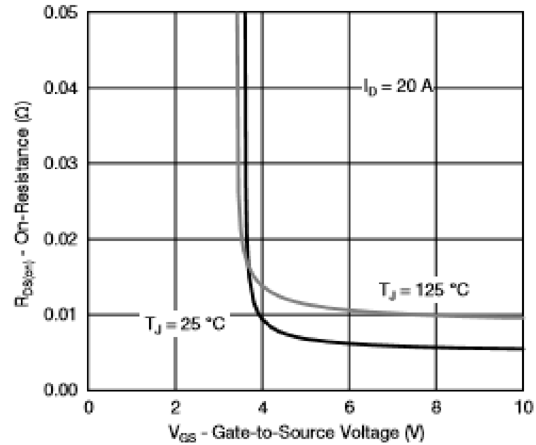


On-Resistance vs. Junction Temperature

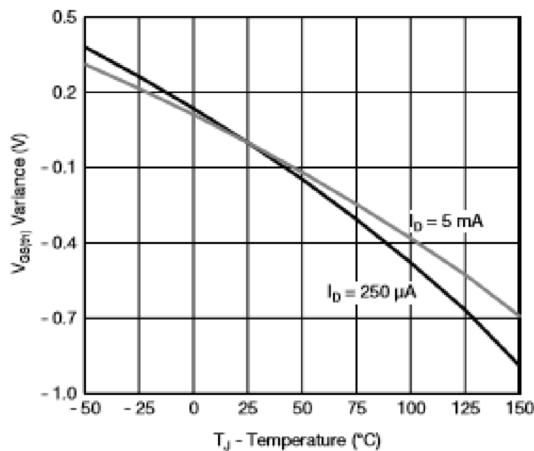
Typical Characteristics



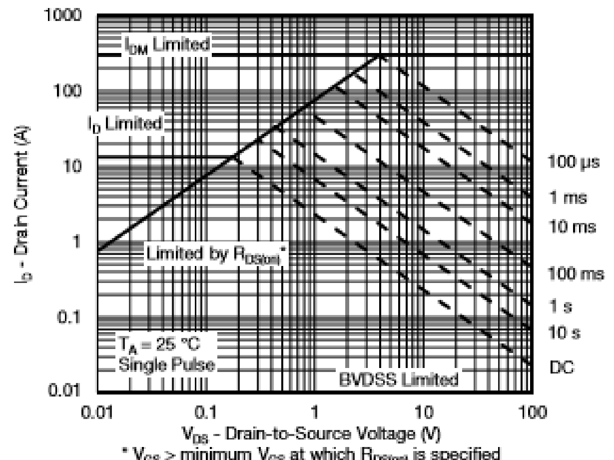
Source-Drain Diode Forward Voltage



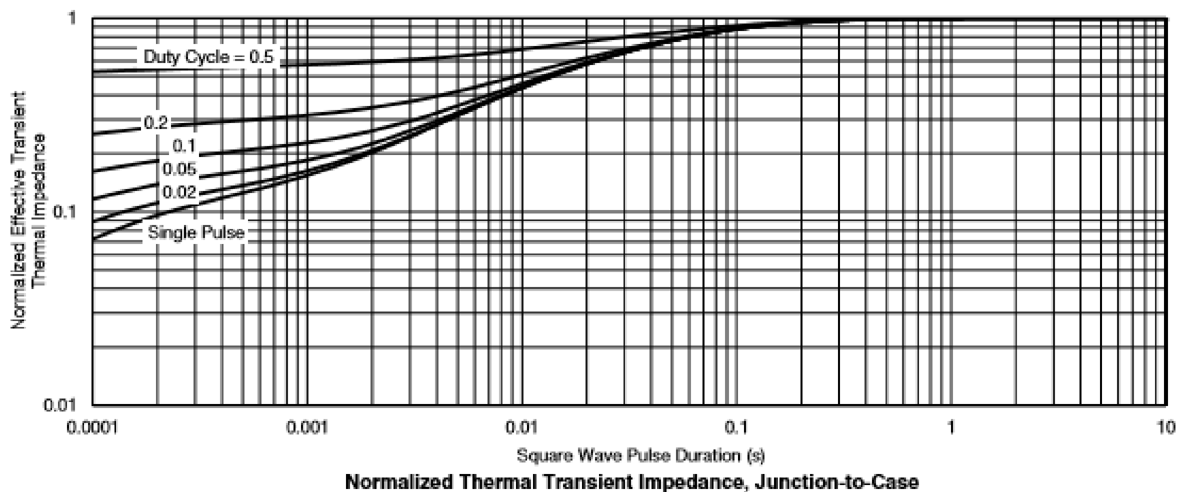
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



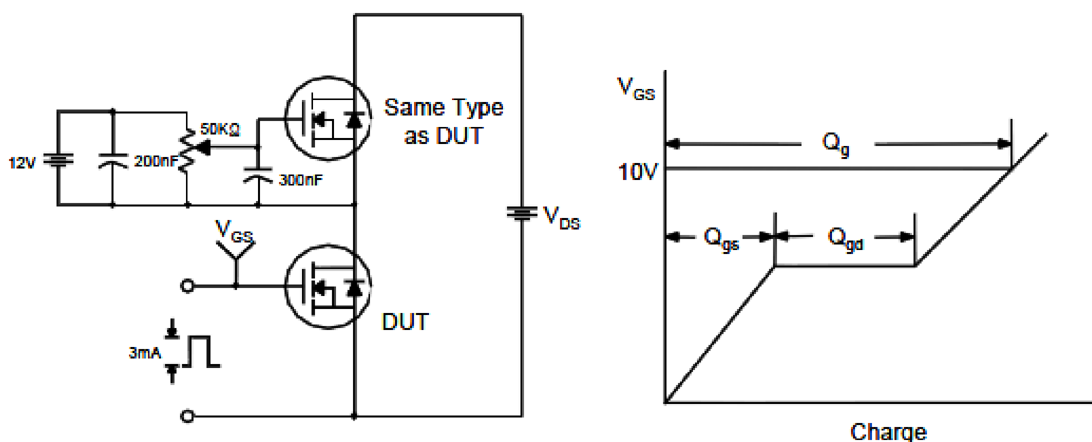
Safe Operating Area, Junction-to-Ambient



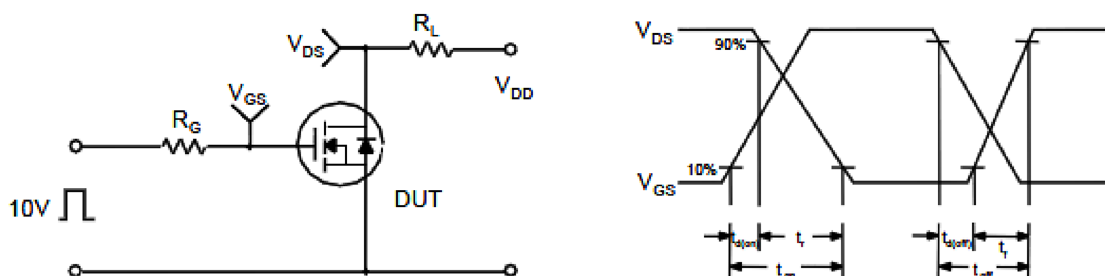
Normalized Thermal Transient Impedance, Junction-to-Case

Typical Characteristics

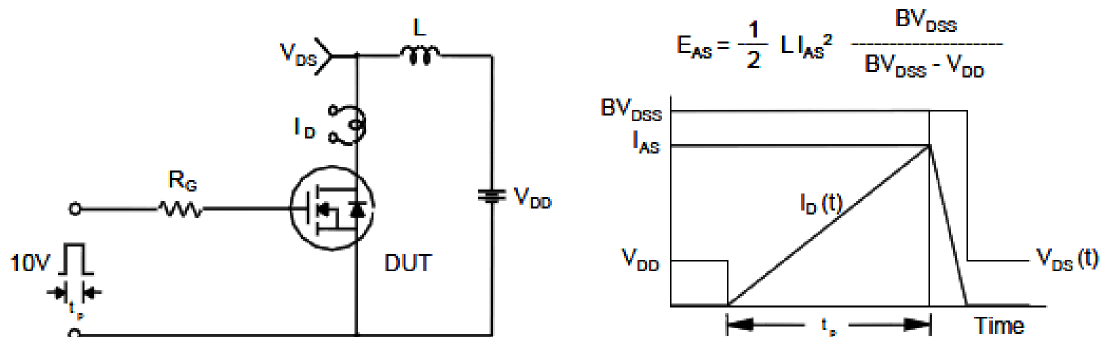
Gate Charge Test Circuit & Waveform



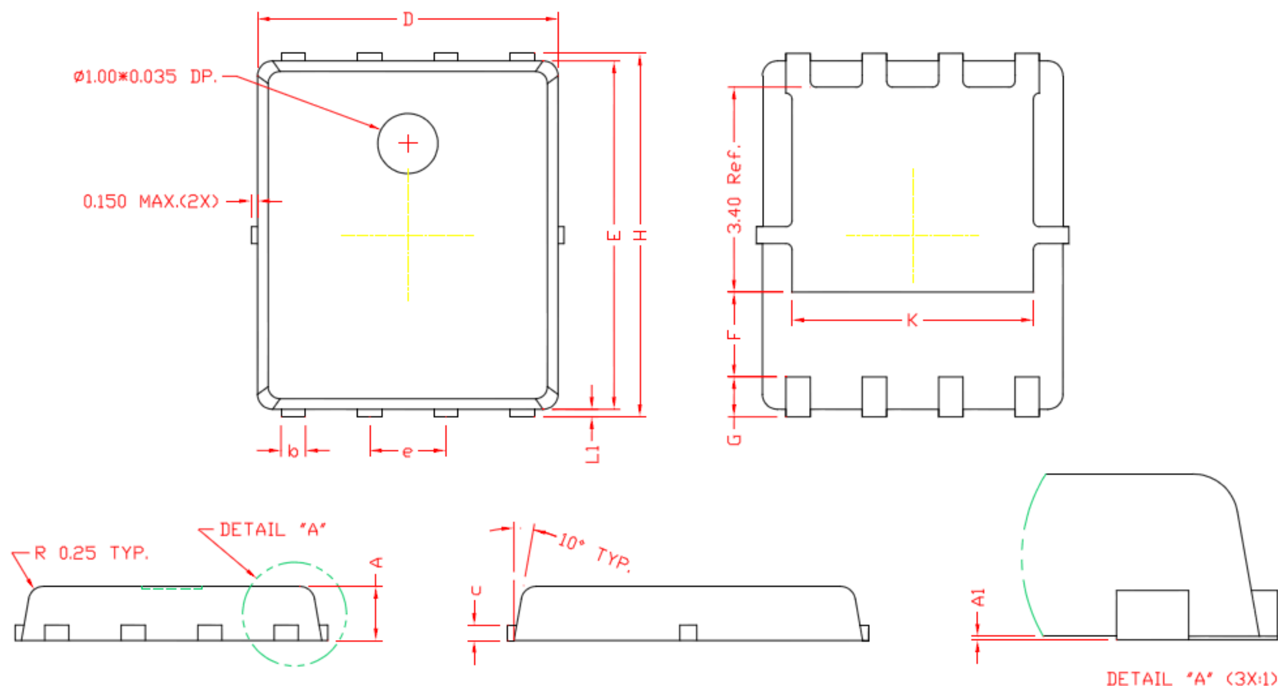
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Package Information (DFN5X6-8L)



DIMENSIONS

REF.	Millimeters		REF.	Millimeters	
	Min.	Max.		Min.	Max.
A	0.80	1.00	E	5.70	5.90
A1	0.00	0.05	e	1.27 BSC.	
b	0.35	0.49	H	5.95	6.20
c	0.254 Ref.		L1	0.10	0.18
D	4.90	5.10	G	0.60 Ref.	
F	1.40 Ref.		K	4.00 Ref.	

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