Alfa-MOS Technology

AFN7002LDS
60V N-Channel
## Enhancement Mode MOSFET

General Description

AFN7002LDS, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 60V/0.5A , $R_{DS(ON)}$=2.4Ω@V_{GS}=10V
- 60V/0.4A , $R_{DS(ON)}$=3.0Ω@V_{GS}=4.5V
- 60V/0.3A , $R_{DS(ON)}$=6.5Ω@V_{GS}=2.5V
- 60V/0.2A , $R_{DS(ON)}$=9.0Ω@V_{GS}=1.8V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- ESD Protection Diode design–in
- SOT-363 package design

Pin Description (SOT-363)
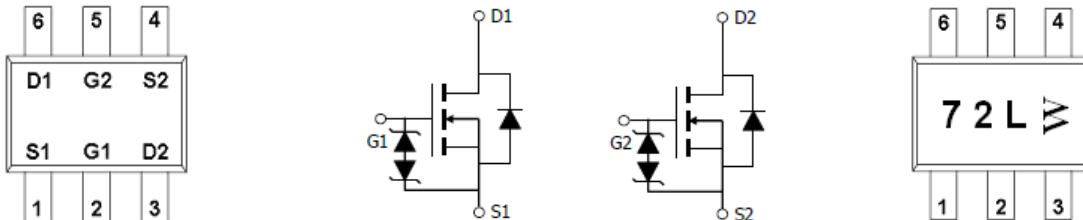
Application

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Load/Power Switching Smart Phones, Pagers

Pin Define

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	D2	Drain 2
4	S2	Source 2
5	G2	Gate 2
6	D1	Drain1

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN7002LDSS36RG	72LW	SOT-363	Tape & Reel	3000 EA

※ 72L Parts code
※ W Month code
※ AFN7002LDSS36RG : 7" Tape & Reel ; Pb- Free ; Halogen –Free

AFN7002LDS
60V N-Channel
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Absolute Maximum Ratings

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	0.64	A
	T_A=70℃		0.35	
Pulsed Drain Current		I_{DM}	0.8	A
Continuous Source Current(Diode Conduction)		I_S	0.8	A
Power Dissipation	T_A=25℃	P_D	0.3	W
	T_A=70℃		0.2	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃

Electrical Characteristics

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.7	1.1	1.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			5	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0V			1	uA
		V_{DS}=48V,V_{GS}=0V T_J=85℃			10	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=0.5A		1.05	2.4	Ω
		V_{GS}= 4.5V,I_D=0.4A		1.35	3.0	
		V_{GS}= 2.5V,I_D=0.3A		3.52	6.5	
		V_{GS}= 1.8V,I_D=0.2A		7.56	9.0	
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=0.2A		0.2		S
Diode Forward Voltage	V_{SD}	I_S=0.2A,V_{GS}=0V		0.75	1.4	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=30V,V_{GS}=10V I_D≡0.25A		1.5	2.5	pC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.5		
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz		28		pF
Output Capacitance	C_{oss}			10		
Reverse Transfer Capacitance	C_{rss}			5		
Turn-On Time	$t_{d(on)}$	V_{DD}=30V, R_G=6Ω I_D≡0.25A, V_{GEN}=10V		3	7	ns
	t_r			12	30	
Turn-Off Time	$t_{d(off)}$			18	40	
	t_f			8	15	

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Typical Characteristics

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

**On-Resistance vs. Junction Temperature**

Typical Characteristics

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient
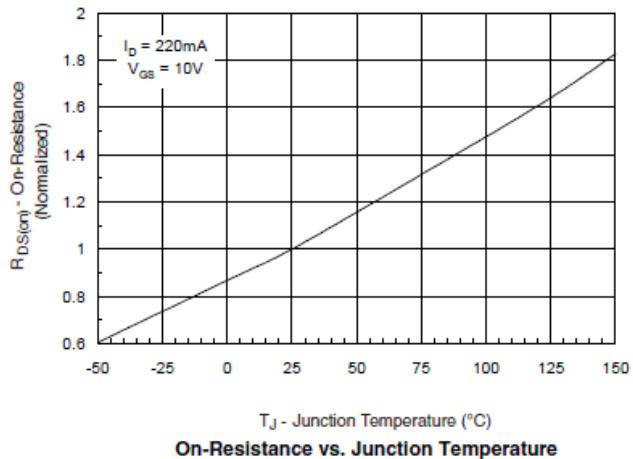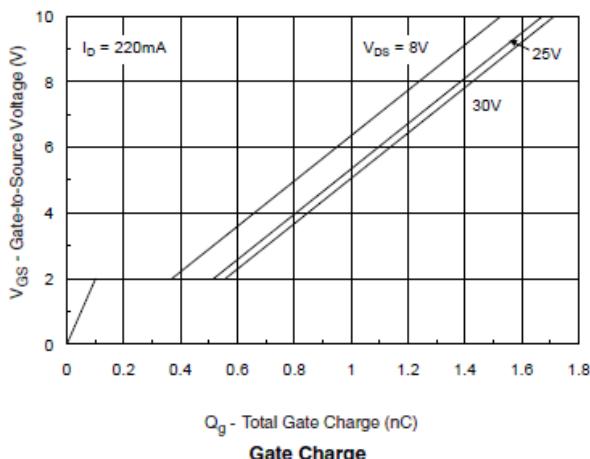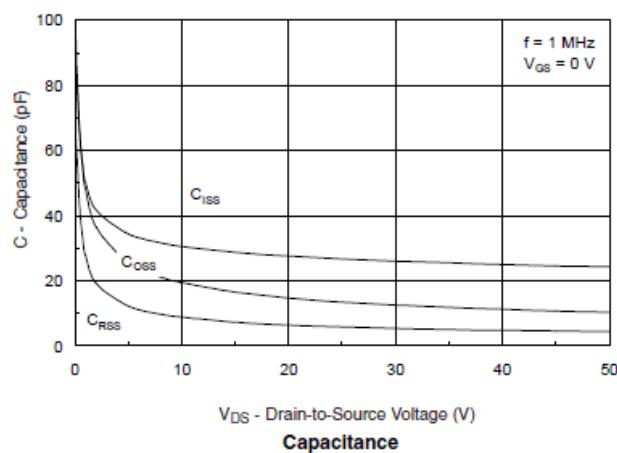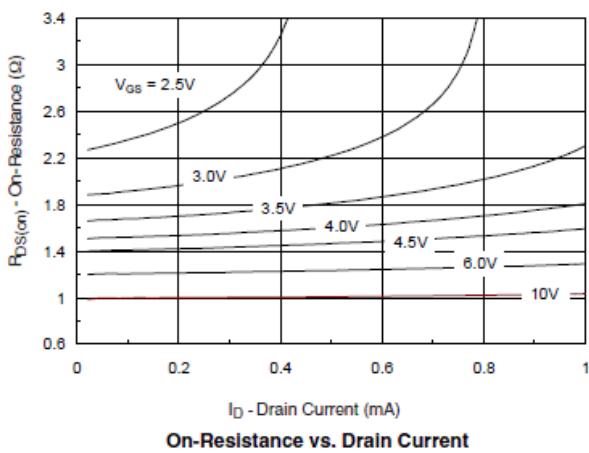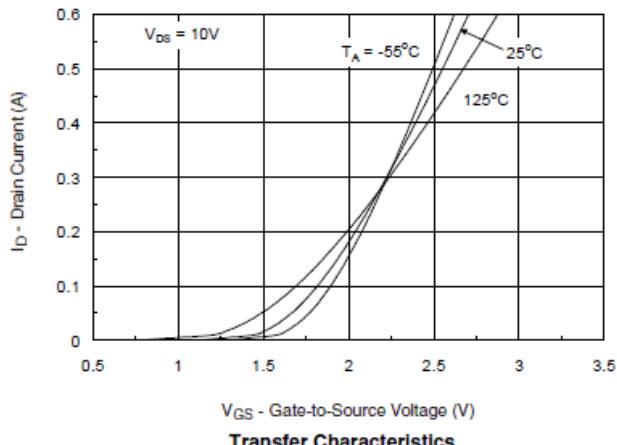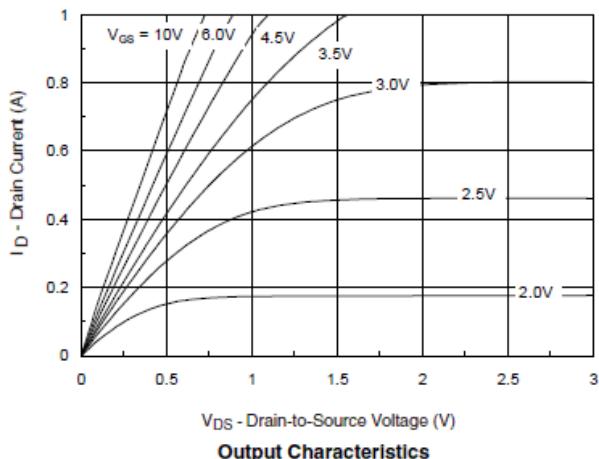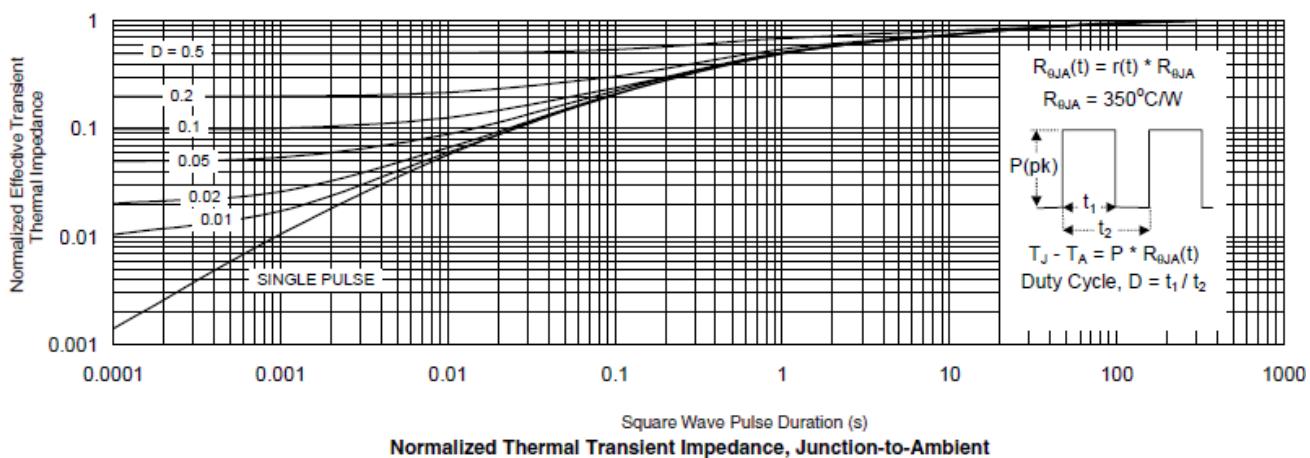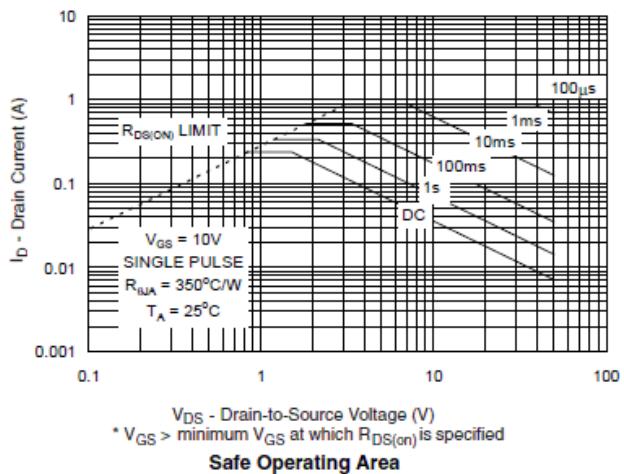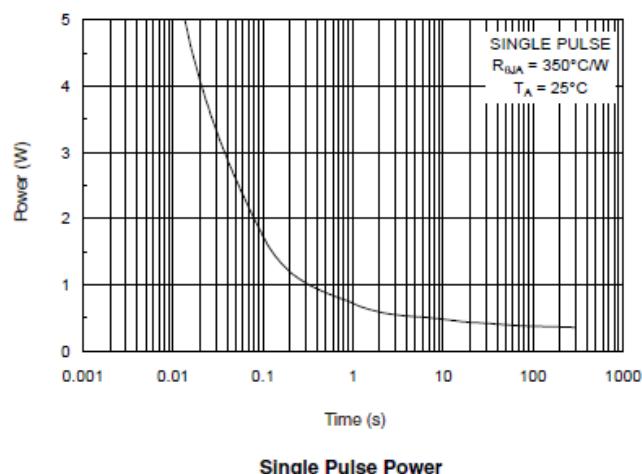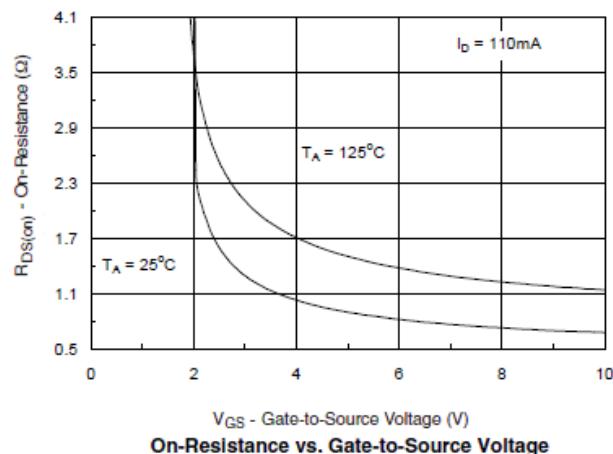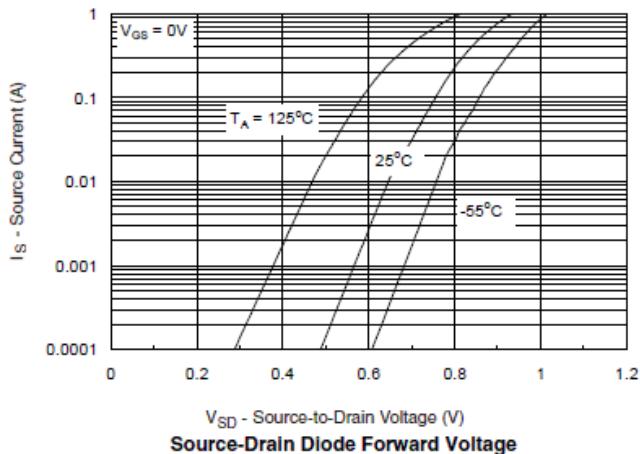
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Typical Characteristics

Gate Charge Test Circuit & Waveform
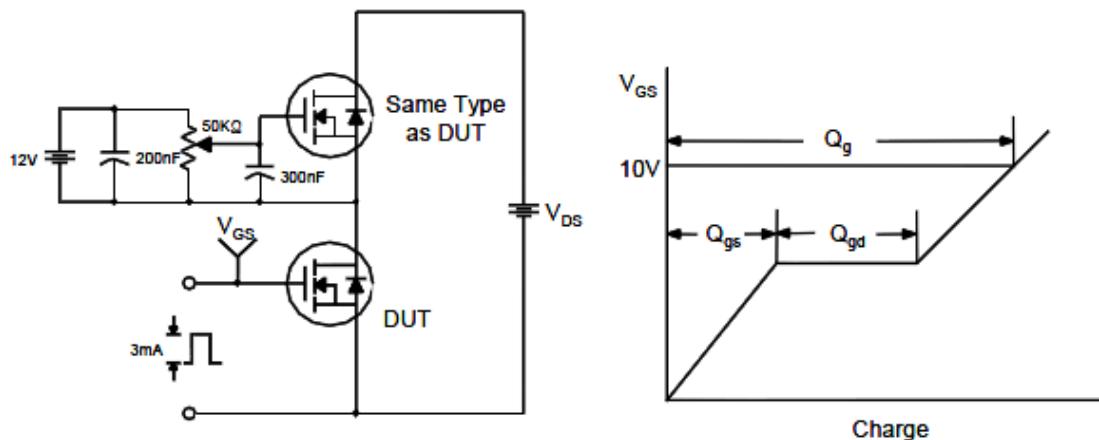
Resistive Switching Test Circuit & Waveforms
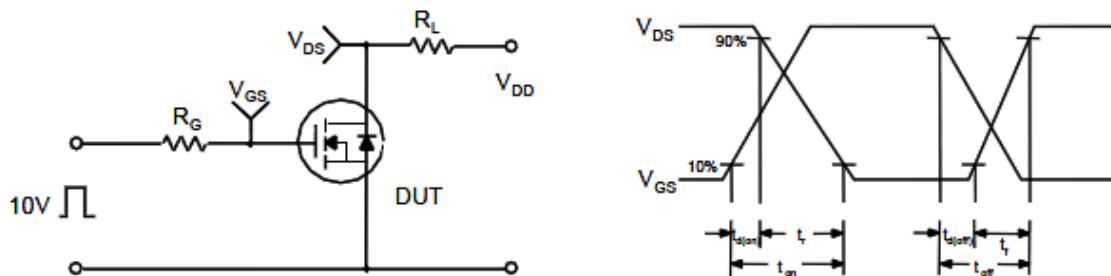
Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \ \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$
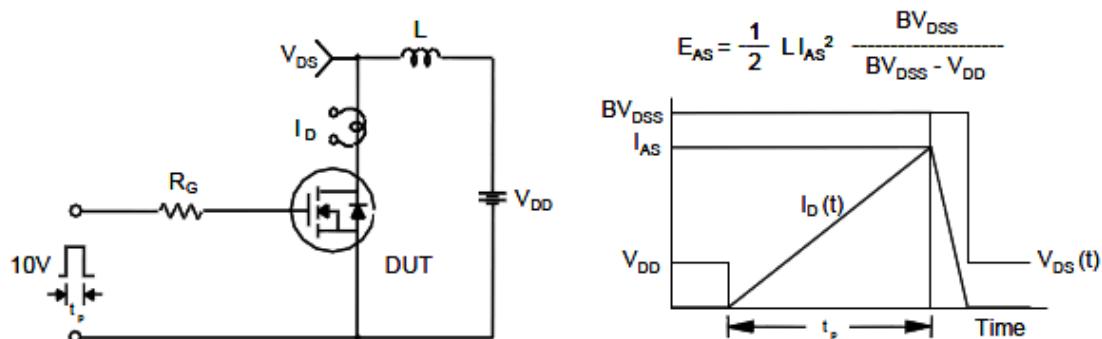
Package Information (SOT-363)
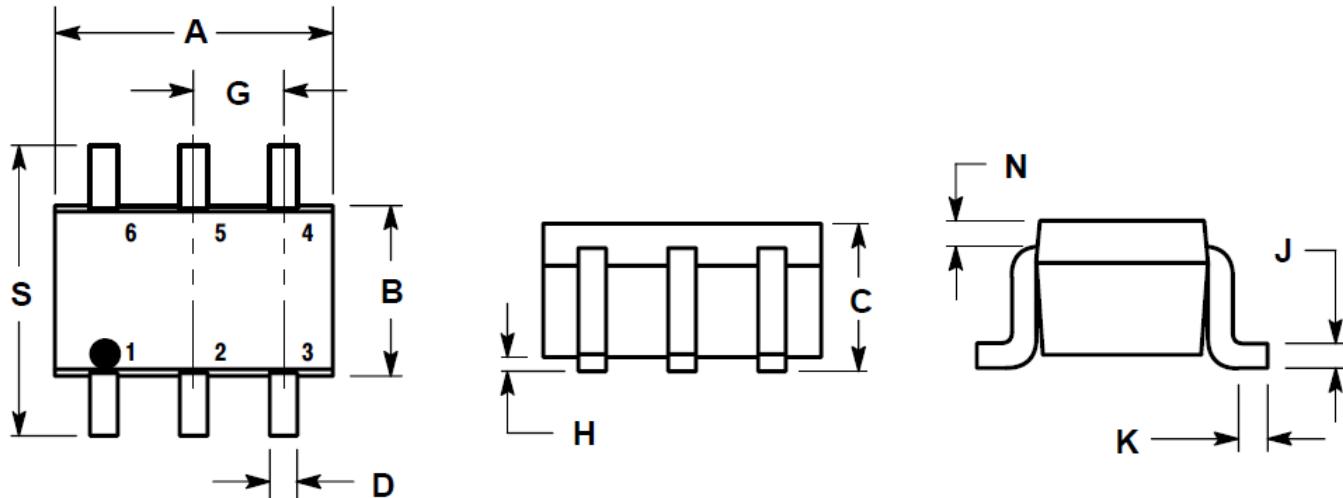
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20