Alfa-MOS Technology

AFP7119WS

200V P-Channel Enhancement Mode MOSFET

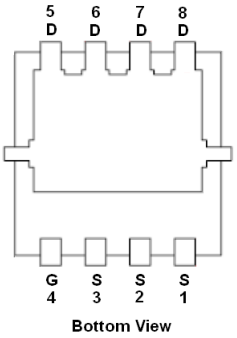
General Description

AFP7119WS, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.
These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

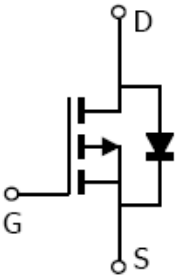
Features

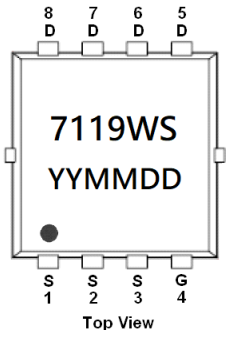
- I_D=-1.2A,$R_{DS(ON)}$=0.8 Ω@V_{GS}=-10V
- I_D=-1.0A,$R_{DS(ON)}$=0.85 Ω@V_{GS}=-6V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- DFN3.3X3.3-8L package design

Pin Description (DFN3.3X3.3-8L)



Bottom View





Top View

Application

- DC-DC Converter
- POL

Pin Define

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP7119WSFN308RG	7119WS	DFN3.3X3.3-8L	Tape & Reel	5000 EA

※ YY year code
※ MM month code
※ DD date code
※ AFP7119WSFN308RG : 13”Tape & Reel ; Pb- Free ; Halogen –Free

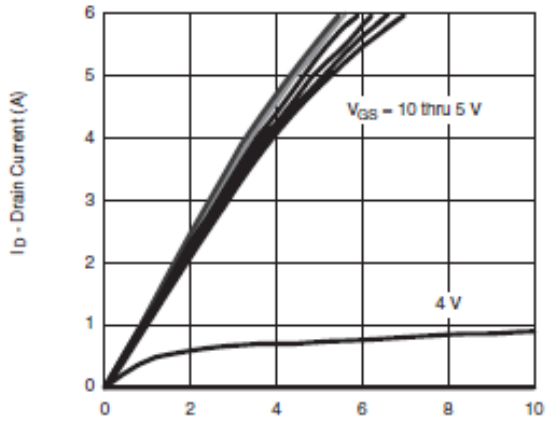
Absolute Maximum Ratings (T_A=25℃ Unless otherwise noted)

Parameter			Symbol	Value		Unit
Drain-Source Voltage			V_{DSS}	-200		V
Gate –Source Voltage			V_{GSS}	±20		V
Continuous Drain Current(T_J=150℃)	T_C=25℃	T_C=70℃	I_D	-3.8	-3.0	A
	T_A=25℃	T_A=70℃		-1.2	-1.0	
Pulsed Drain Current			I_{DM}	-5		A
Single pulse avalanche energy	L=0.1 mH		E_{AS}	1.0		mJ
Continuous Source Current (Diode Conduction)	T_C=25℃	T_A=25℃	I_S	-5	-3	A
Power Dissipation	T_C=25℃	T_C=70℃	P_D	50	30	W
	T_A=25℃	T_A=70℃		3.7	2.4	
Operating Junction Temperature			T_J	150		℃
Storage Temperature Range			T_{STG}	-50/150		℃
Thermal Resistance Junction-to-Case (Drain)			$R_{\theta JC}$	3.8		℃/W
Thermal Resistance-Junction to Ambient			$R_{\theta JA}$	35		

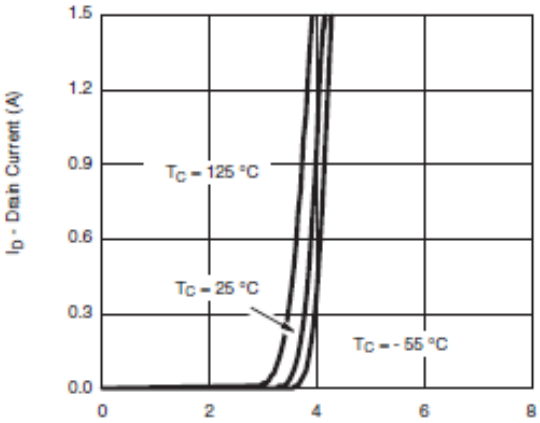
Electrical Characteristics (T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-200	-215		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-2.0	-3.0	-4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-160V,V_{GS}=0V			-1	uA
		V_{DS}=-160V,V_{GS}=0V T_J=85℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧-10V,V_{GS}=-10V	-3			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-1.2A		0.72	0.8	Ω
		V_{GS}=-6V,I_D=-1.0A		0.75	0.85	
Forward Transconductance	g_{FS}	V_{DS}=-15V,I_D=-1.0A		4		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V		-0.75	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-100V,V_{GS}=-6V I_D≡-1A		12	25	nC
Gate-Source Charge	Q_{gs}			3.2		
Gate-Drain Charge	Q_{gd}			5.5		
Gate Resistance	R_g	f=1MHz		5.5	15	Ω
Pulse Diode Forward Current	I_{SM}				-12	A
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V f=1MHz		700		pF
Output Capacitance	C_{oss}			40		
Reverse Transfer Capacitance	C_{rss}			30		
Turn-On Time	$t_{d(on)}$	V_{DD}=-100V,R_L=100Ω I_D≡-1.0A,V_{GEN}=-10V R_G=1.0Ω		10	20	ns
	t_r			12	25	
Turn-Off Time	$t_{d(off)}$			25	50	
	t_f			15	30	
Body Diode Reverse Recovery Time	t_{rr}	I_F=- 4 A, dI/dt=100 A/μs, T_J = 25 ℃		70	100	ns
Body Diode Reverse Recovery Charge	Q_{rr}			220	280	nC

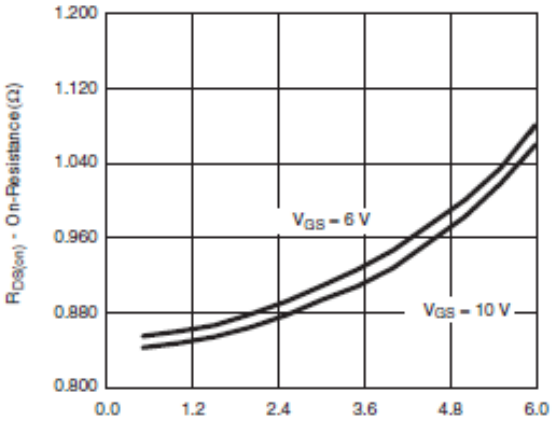
Typical Characteristics



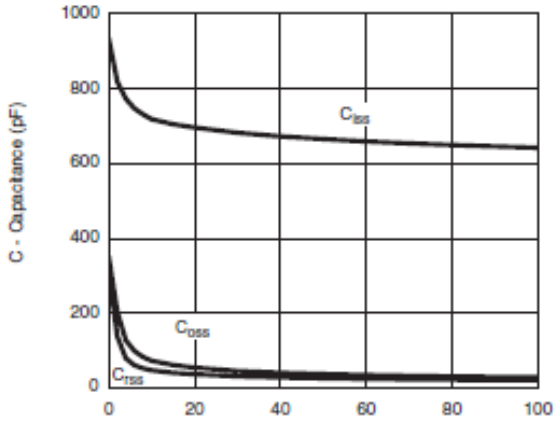
Output Characteristics



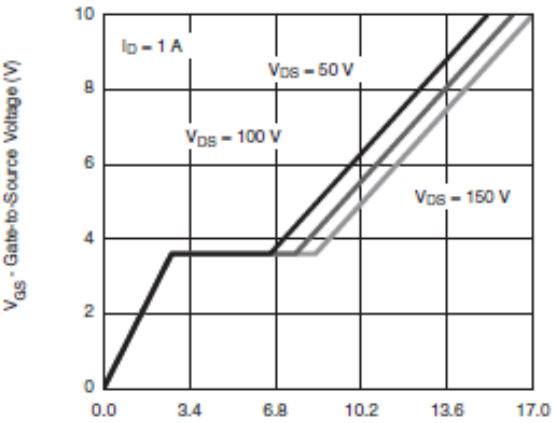
Transfer Characteristics



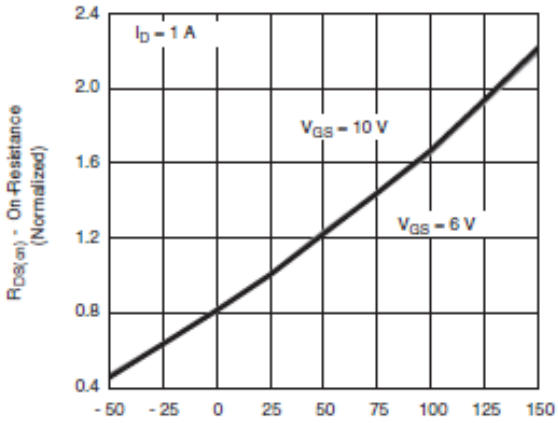
On-Resistance vs. Drain Current



Capacitance

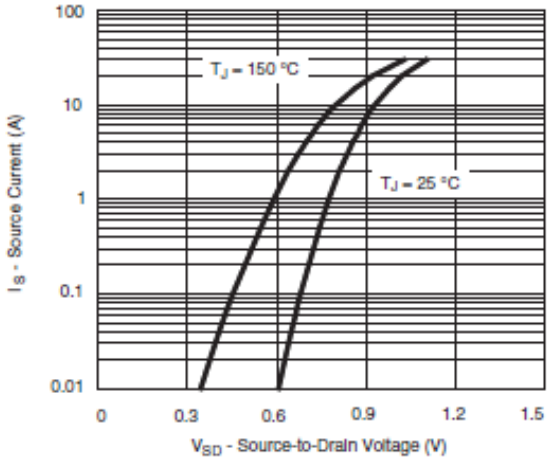


Gate Charge

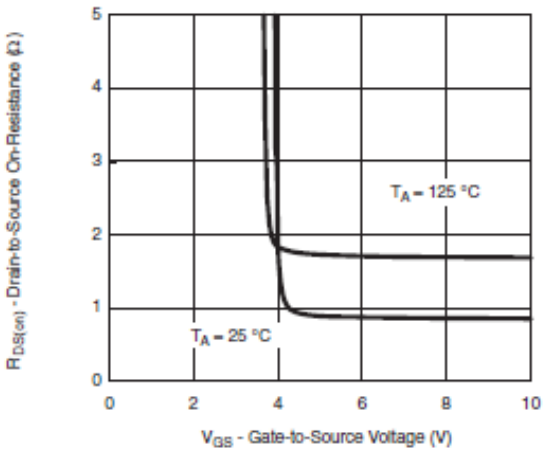


On-Resistance vs. Junction Temperature

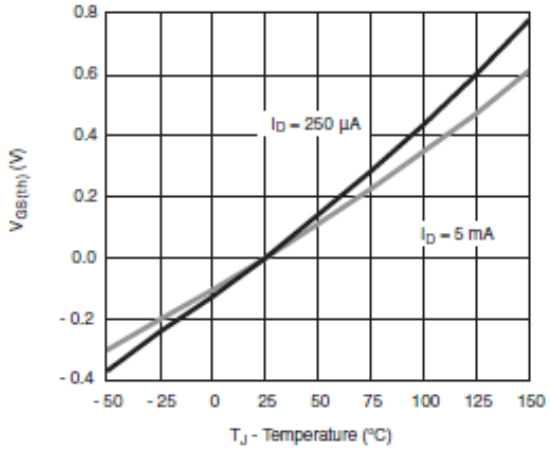
Typical Characteristics



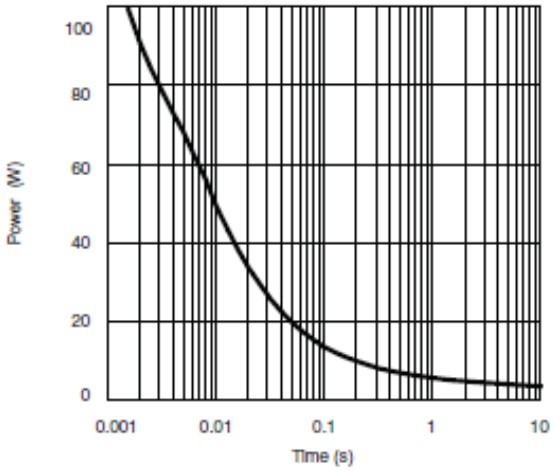
Source-Drain Diode Forward Voltage



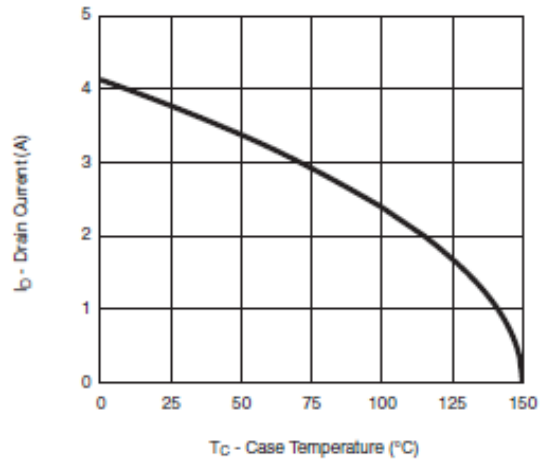
On-Resistance vs. Gate-to-Source Voltage



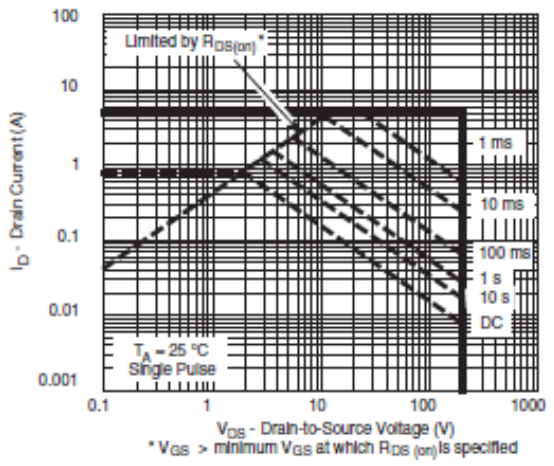
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

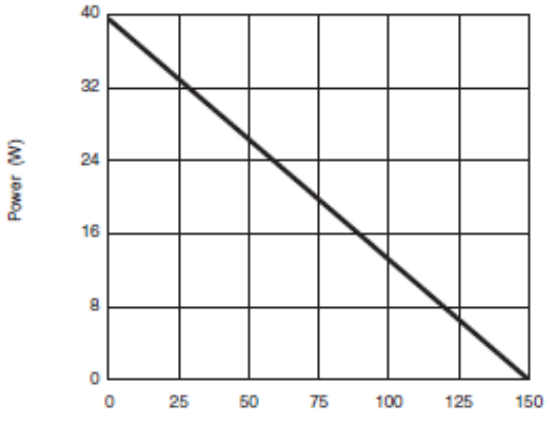


Current Derating*

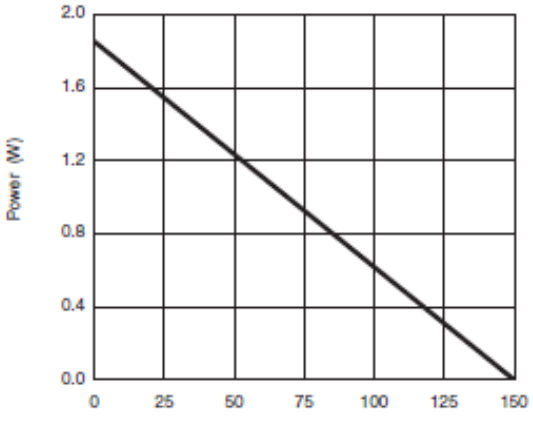


Safe Operating Area, Junction-to-Ambient

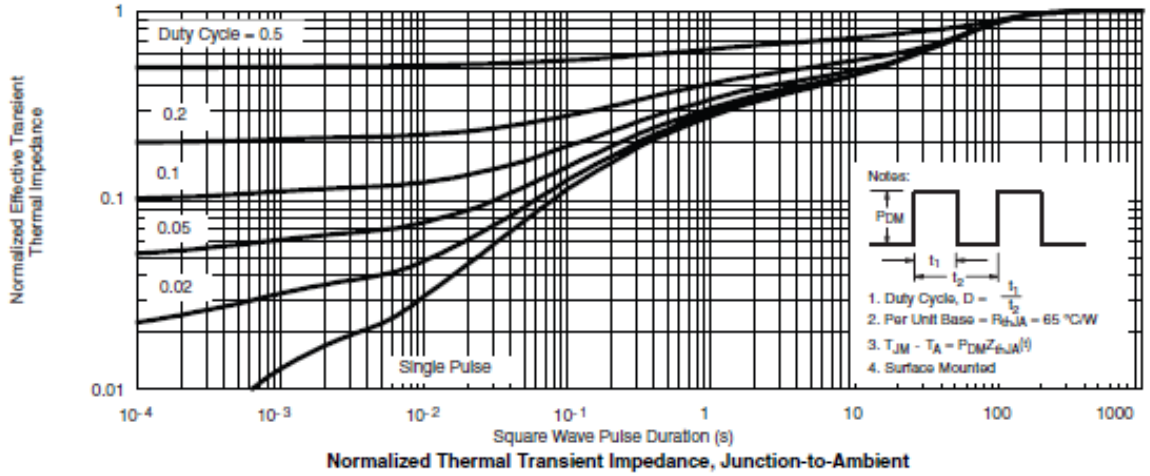
Typical Characteristics



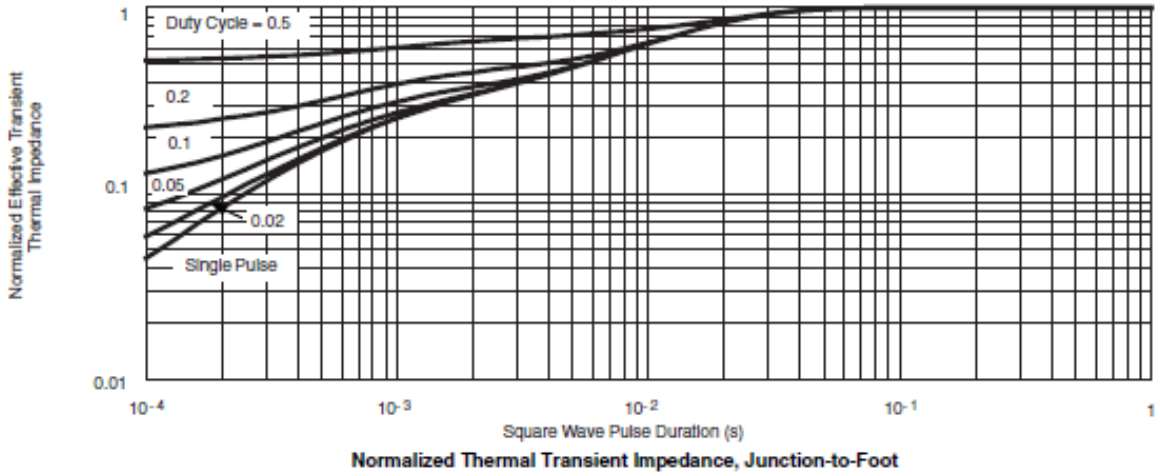
Power, Junction-to-Case



Power, Junction-to-Ambient



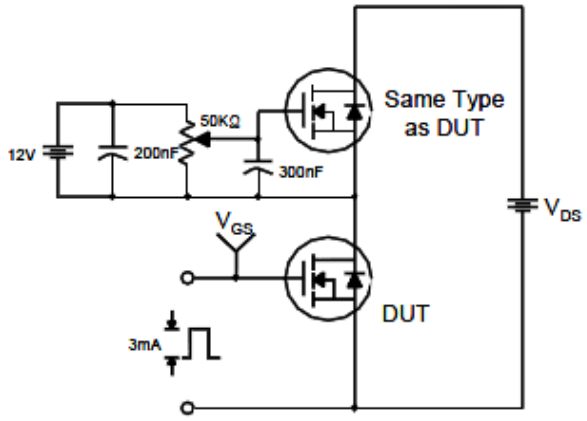
Normalized Thermal Transient Impedance, Junction-to-Ambient

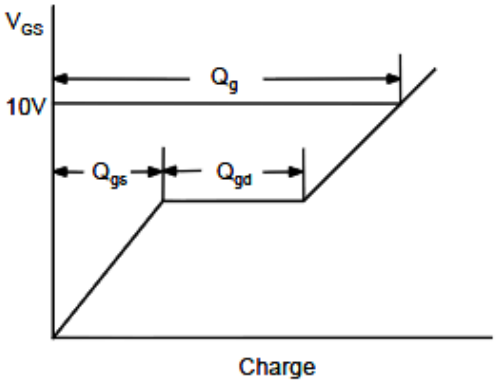


Normalized Thermal Transient Impedance, Junction-to-Foot

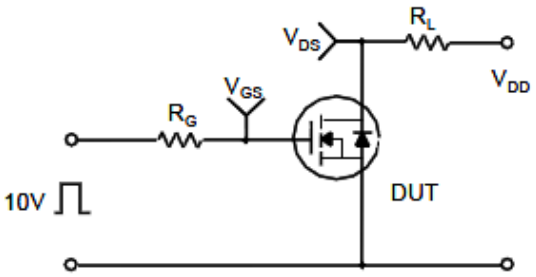
Typical Characteristics

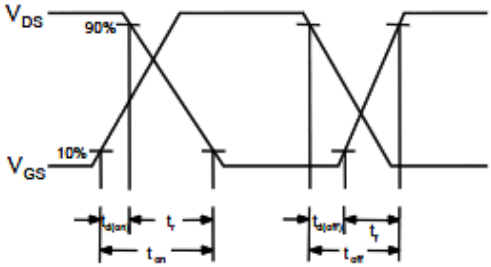
Gate Charge Test Circuit & Waveform



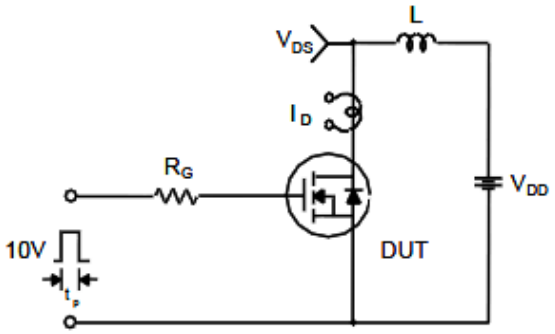


Resistive Switching Test Circuit & Waveforms

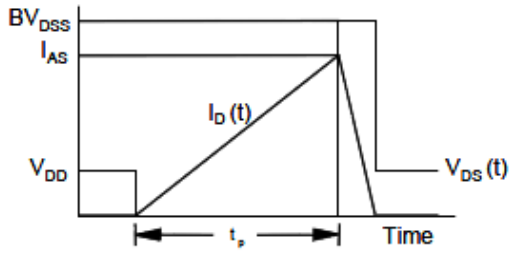




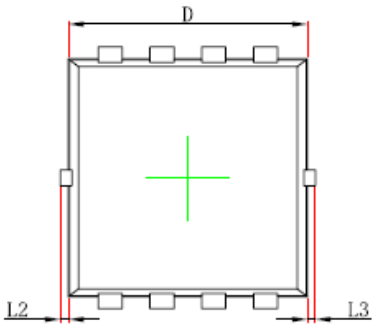
Unclamped Inductive Switching Test Circuit & Waveforms



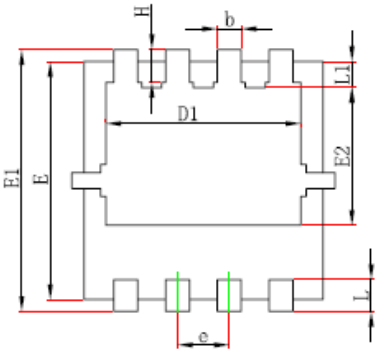
$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



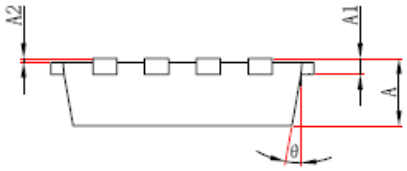
Package Information (DFN3.3X3.3-8L)



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)
Tel : 886 2) 2651 3928
Fax : 886 2) 2786 8483
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