Alfa-MOS Technology

AFP7463S
40V P-Channel Enhancement Mode MOSFET

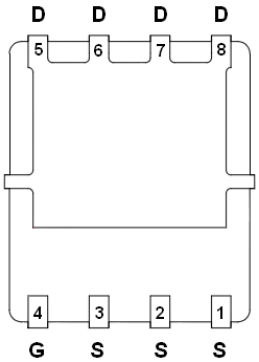
General Description

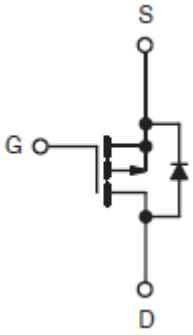
AFP7463S, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.
These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- -40V/-15A,$R_{DS(ON)}$=12mΩ@V_{GS}=-10V
- -40V/-10A,$R_{DS(ON)}$=15mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- DFN5X6-8L package design

Pin Description (DFN5X6-8L)





Application

- Load Switch
- Adaptor Switch
- Notebook PC

Pin Define

Pin	Symbol	Description
4	G	Gate
1~3	S	Source
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP7463SFN568RG	7463S	DFN5X6-8L	Tape & Reel	2500 EA

※ 7463S : Parts Code
※ YYMMDD : Date code
※ AFP7463SFN568RG : 13”Tape & Reel ; Pb- Free ; Halogen- Free

Absolute Maximum Ratings

(T_A=25℃ Unless otherwise noted)

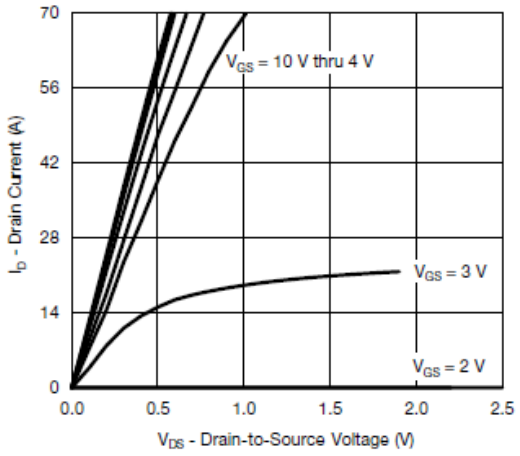
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-40	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_{DSM}	-17	A
	T_A=70℃		-14	
Pulsed Drain Current		I_{DM}	-65	
Continuous Source Current(Diode Conduction)		I_S	-4.0	
Single Pulse Avalanche Current		I_{AS}	-25	
Power Dissipation	T_A=25℃	P_{DSM}	4.2	W
	T_A=75℃		2.7	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient	t ≤ 10 s	$R_{\theta JA}$	20	℃/W
Thermal Resistance-Junction to Case	Steady-State	$R_{\theta JC}$	2.1	

Electrical Characteristics

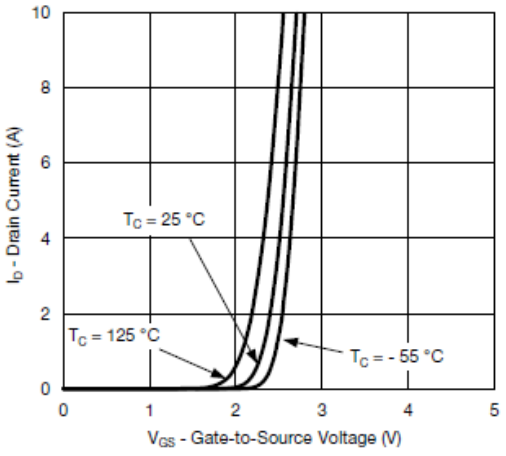
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D= -250uA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D= -250uA	-1.0		-2.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}= ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= -32V,V_{GS}=0V			-1	uA
		V_{DS}= -32V,V_{GS}=0V T_J=85℃			-20	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧ -10V,V_{GS}= -10V	-25			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V,I_D= -15A		10	12	mΩ
		V_{GS} = -4.5V,I_D= -10A		13	15	
Forward Transconductance	g_{FS}	V_{DS}= -10V,I_D= -15A		40		S
Diode Forward Voltage	V_{SD}	I_S= -1A,V_{GS}=0V		-0.8	-1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-20V,V_{GS}=-4.5V I_D= -10A		45	90	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			20		
Input Capacitance	C_{iss}	V_{DS}=-20V,V_{GS}=0V f=1MHz		4150		pF
Output Capacitance	C_{oss}			435		
Reverse Transfer Capacitance	C_{rss}			400		
Turn-On Time	$t_{d(on)}$	V_{DD}=-20V,R_L=2Ω I_D≡-10A,V_{GEN}=-10V R_G=1Ω		15	30	ns
	t_r			15	30	
Turn-Off Time	$t_{d(off)}$			55	110	
	t_f			12	25	

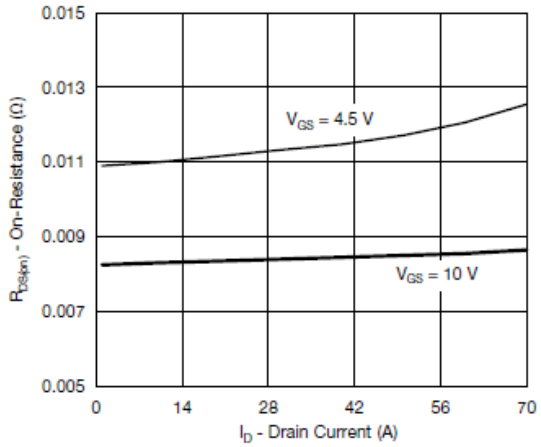
Typical Characteristics



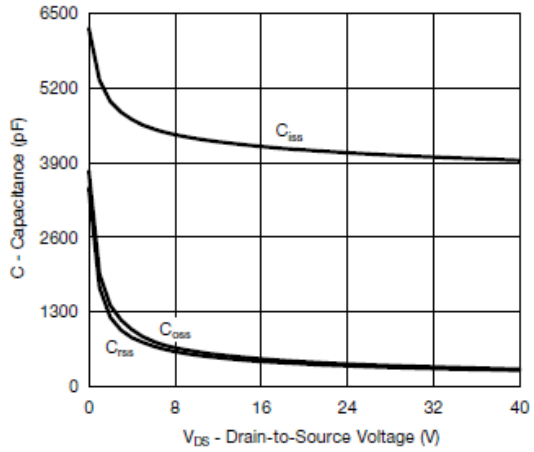
Output Characteristics



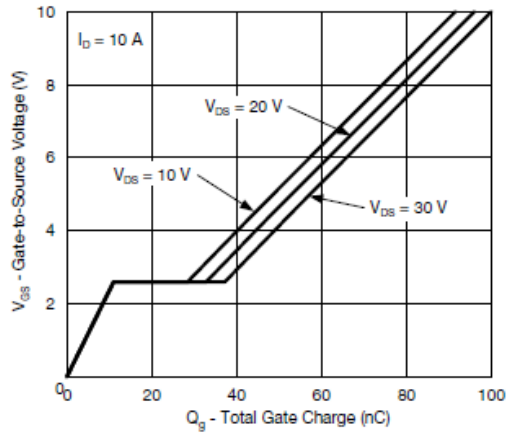
Transfer Characteristics



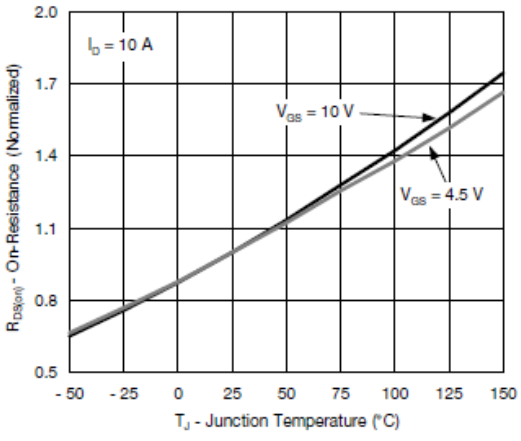
On-Resistance vs. Drain Current



Capacitance

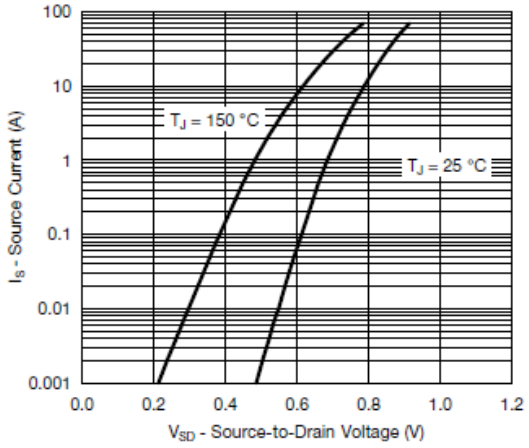


Gate Charge

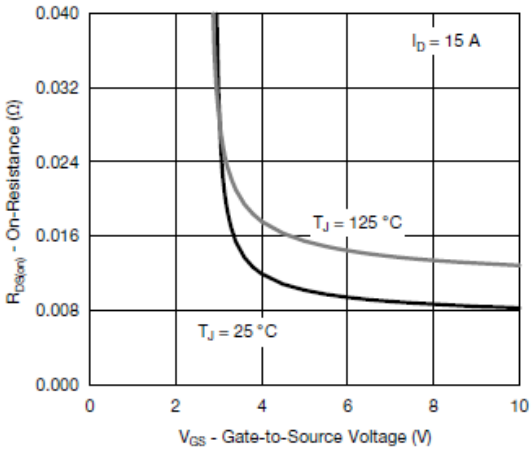


On-Resistance vs. Junction Temperature

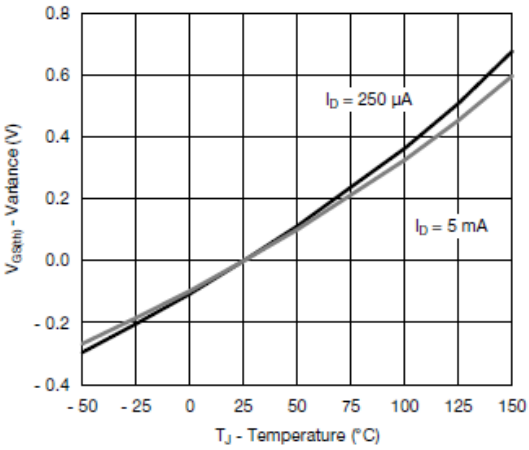
Typical Characteristics



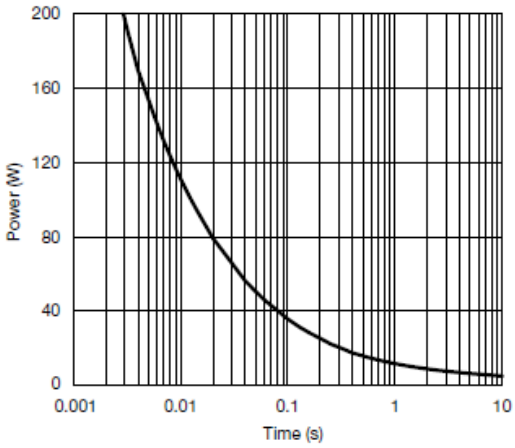
Source-Drain Diode Forward Voltage



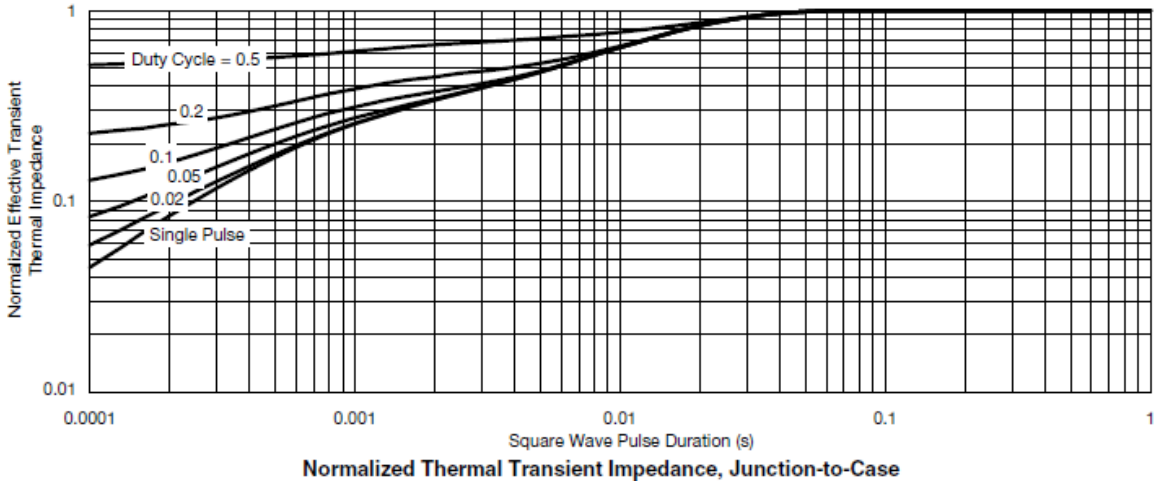
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



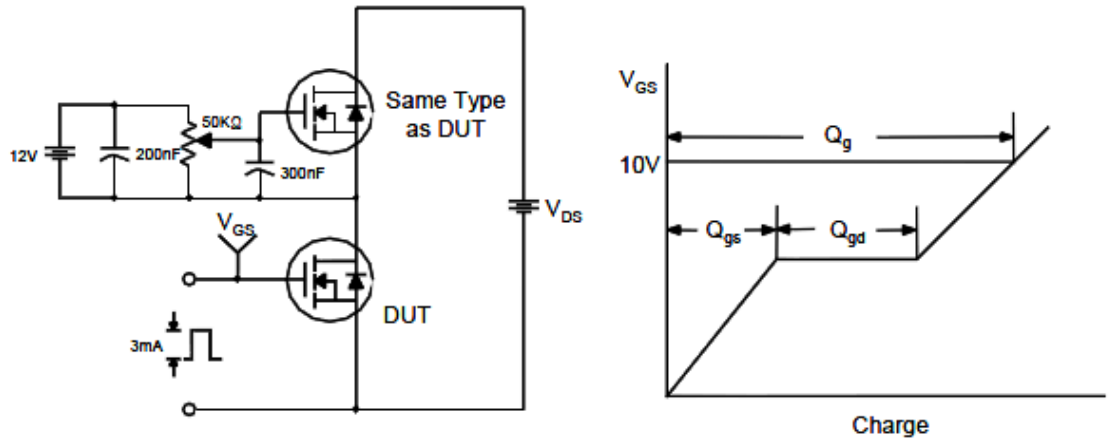
Single Pulse Power, Junction-to-Ambient



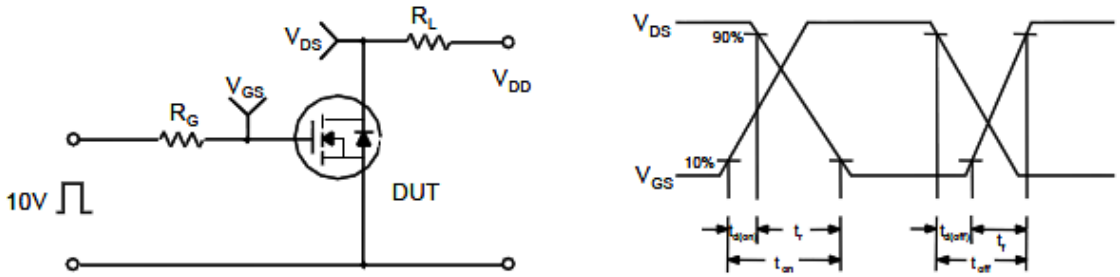
Normalized Thermal Transient Impedance, Junction-to-Case

Typical Characteristics

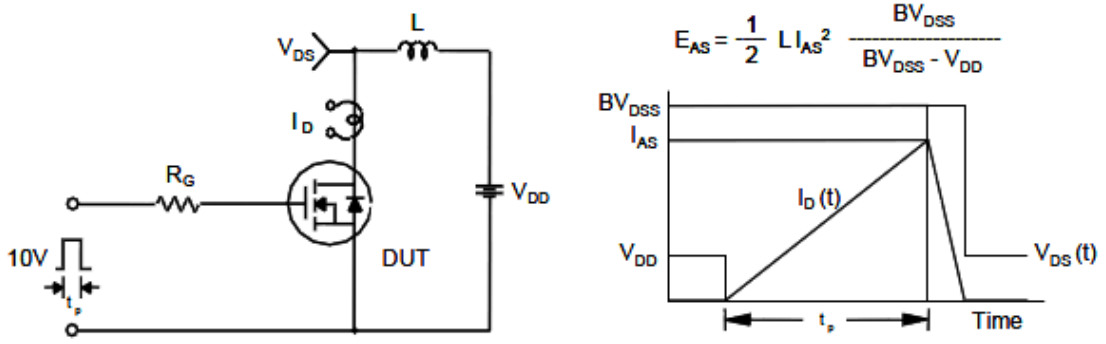
Gate Charge Test Circuit & Waveform



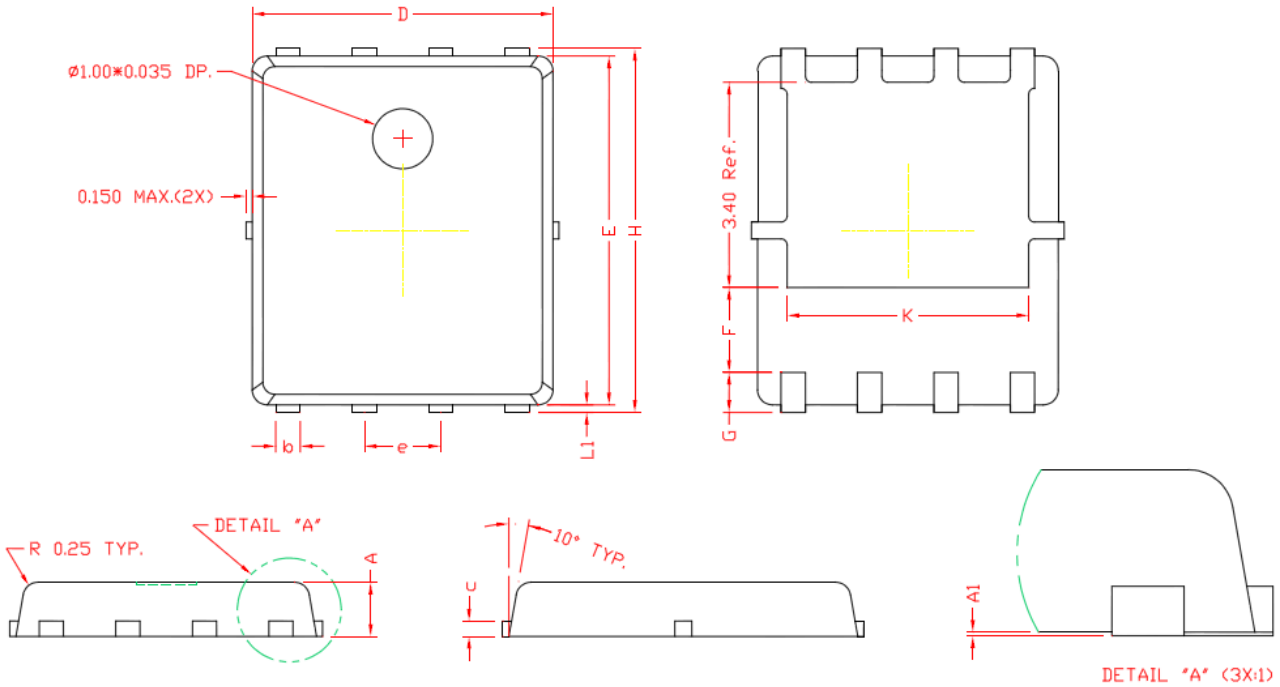
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Package Information (DFN5X6-8L)



DIMENSIONS

REF.	Millimeters		REF.	Millimeters	
	Min.	Max.		Min.	Max.
A	0.80	1.00	E	5.70	5.90
A1	0.00	0.05	e	1.27 BSC.	
b	0.35	0.49	H	5.95	6.20
c	0.254 Ref.		L1	0.10	0.18
D	4.90	5.10	G	0.60 Ref.	
F	1.40 Ref.		K	4.00 Ref.	

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