

Specification for TFT

AFR240240A1-1.3INTM

Revision V1.0



A	Orient Display
FR	TFT Type
240240	Resolution 240 x 240
A1	Serial A1
1.3	1.3", Module Dimension 26.16x29.22x1.79 mm
I	IPS Display
N	Top: -20~+70°C; Tstr: -30~+80°C
T	Transmissive/Normally Black
M	Medium Brightness, 470 cd/m2
/	No Touch Panel
/	Controller ST7789V2
/	8/9/16/18Bit MCU; 3/4SPI+16/18Bit RGB



Revision History

[illegible]

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses a amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit , back-light unit. The resolution of a 1.3 " TFT-LCD contains 240x240 pixels, and can display up to 65K/262K colors.

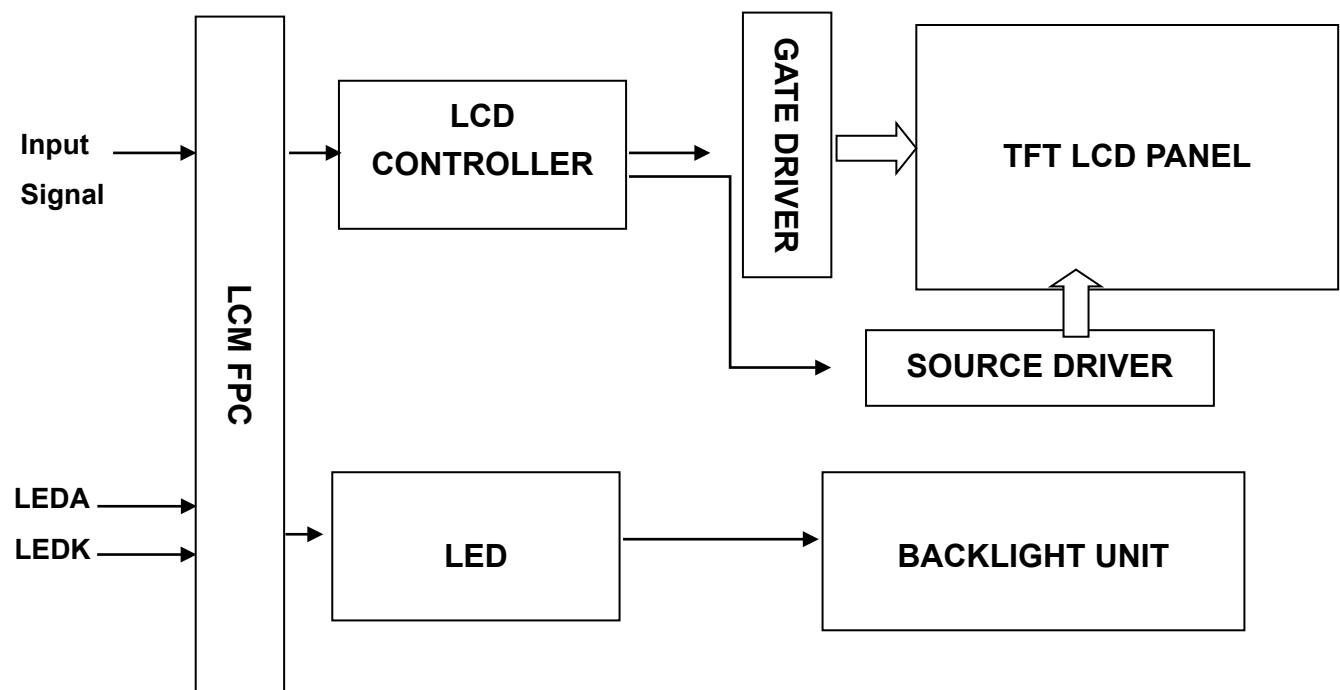
* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	23.4(H)*23.4(V) (1.3 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K	colors	
Number of pixels	240(RGB)*240	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.0975(H)*0.0975(V)	mm	
Viewing angle	ALL	o'clock	
Controller IC	ST7789V2	-	
LCM Interface	8/9/16/18bit MCU 3/4SPI+16/18BIT RGB 3-line/4-line Serial interface	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	

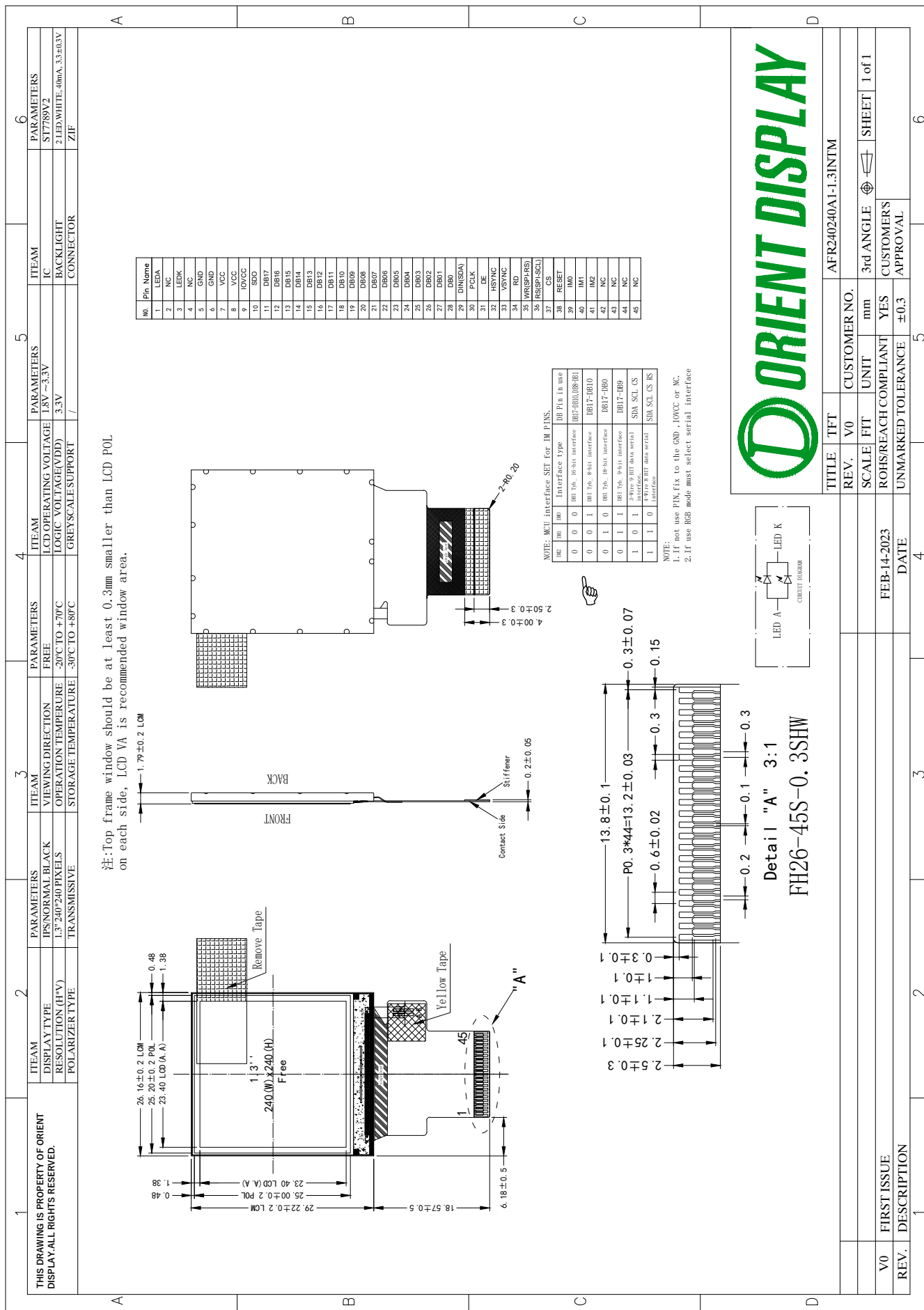
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	26.16	-	mm	
	Vertical(V)	-	29.22	-	mm	
	Depth(D)	-	1.79	-	mm	
Weight		-	2	-	g	

1. Block Diagram



2. Outline dimension



2. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	LEDA	Anode pin of backlight	P
2	NC	--	--
3	LEDK	Cathode pin OF backlight	P
4	NC	--	--
5	GND	Ground.	P
6	GND		
7	VCC	Supply voltage(3.3V).	P
8	VCC		
9	IOVCC	Supply voltage(1.65-3.3V).	P
10	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. If not used, let this pin open.	O
11-28	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
29	DIN(SDA)	When IM3: Low, SPI interface input/output pin. When IM3: High, SPI interface input pin. The data is latched on the rising edge of the SCL signal. If not used, please fix this pin at IOVCC or DGND level	I/O
30	PCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
31	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
32	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
33	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
34	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at IOVCC or GND when not in use.	I
35	WR(SPI-RS)	Write enable in MCU parallel interface. Display data/command selection pin in 4-line serial interface. Second Data lane in 2 data lane serial interface.	I

		If not used, please fix this pin at IOVCC or DGND.	
36	RS(SPI-SCL)	Display data/command selection pin in parallel interface. This pin is used to be serial interface clock. RS='1': display data or parameter. RS='0': command data. If not used, please fix this pin at IOVCC or DGND.	I
37	CS	Chip select input pin ("Low" enable). fix this pin at IOVCC or GND when not in use.	I
38	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
39	IM0	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.	I
40	IM1		
41	IM2		
42-45	NC	No Connection	--

NOTE: MCU interface SET for IM PINS.

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 16-bit interface	DB17-DB10, DB8-DB1
0	0	1	DBI Tyb_ 8-bit interface	DB17-DB10
0	1	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	1	1	DBI Tyb_ 9-bit interface	DB17-DB9
1	0	1	3-Wire 9 BIT data serial interface.	SDA SCL CS
1	1	0	4-Wire 8 BIT data serial interface	SDA SCL CS RS

NOTE:

- 1.If not use PIN, fix to the GND , IOVCC or NC.**
- 2.If use RGB mode must select serial interface**

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	640	800	--		(1)(2)
Response time	Rising	T_R+T_F		--	35	40	msec	(1)(3)
	Falling							
Color Gamut		S(%)		43	48	--	%	*
Color Filter Chromaticity	White	W_X		0.265	0.305	0.345		(1)(4) CA- 310
		W_Y		0.2833	0.3233	0.3633		
	Red	R_X		0.5315	0.5715	0.6115		
		R_Y		0.3056	0.3456	0.3856		
	Green	G_X		0.3172	0.3572	0.3972		
		G_Y		0.5127	0.5527	0.5927		
	Blue	B_X		0.1149	0.1549	0.1949		
		B_Y		0.0638	0.1038	0.1438		
Viewing angle	Hor.	Θ_L	CR>10	70	80	--		(1)(4)
		Θ_R		70	80	--		
	Ver.	Θ_U		70	80	--		
		Θ_D		70	80	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

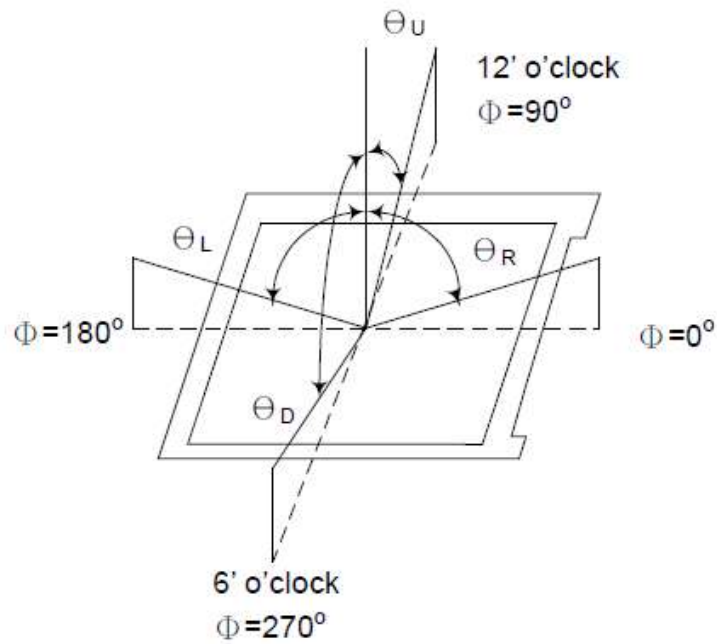
Ambient temperature : $25\pm 2^\circ\text{C}$

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

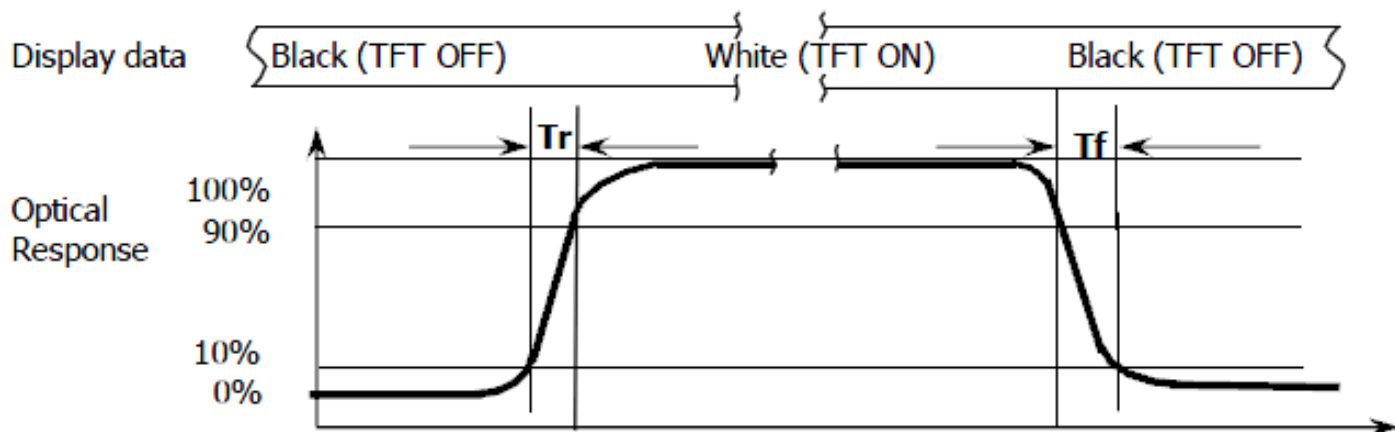
Note (1): Definition of Viewing Angle :



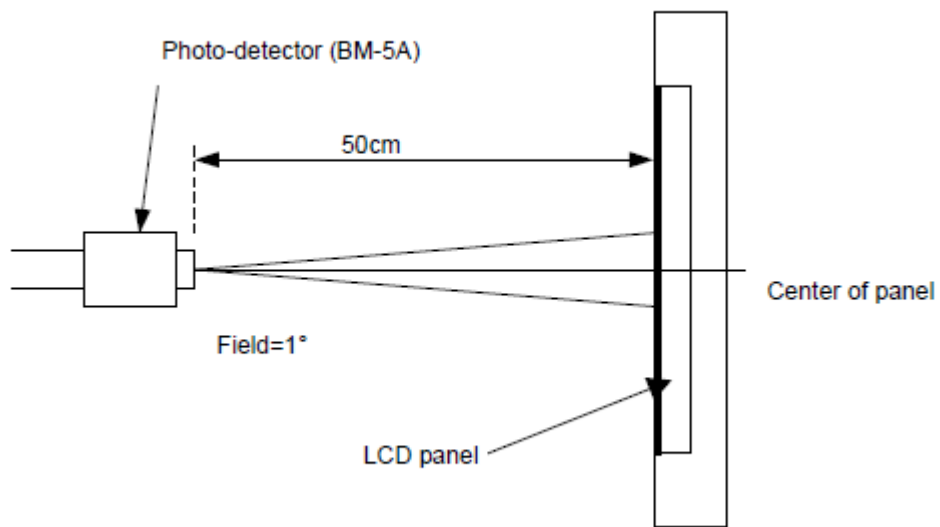
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCC	-0.3	4.6	V	Note1
Digital interface supply	IOVCC	-0.3	4.6	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily,

the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values

exceeding which the product may be physically damaged. Be sure to use the product within the range

of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCC	2.4	3.3	3.6	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	7	--	mA	
Level input voltage	V _{IH}	0.7*IOVCC	--	IOVCC	V	
	V _{IL}	GND	--	0.3*IOVCC	V	
Level output voltage	V _{OH}	0.8*IOVCC	--	IOVCC	V	
	V _{OL}	GND	--	0.2*IOVCC	V	

5.3 LED Backlight Characteristics

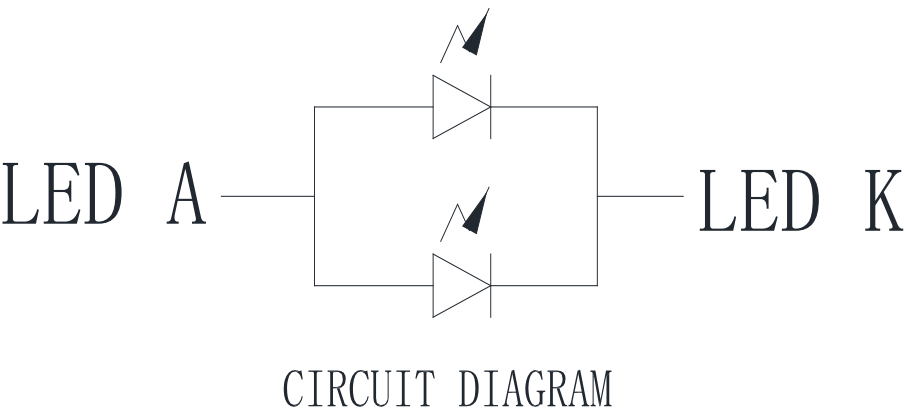
The back-light system is edge-lighting type with 2 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	35	40	--	mA	
Forward Voltage	V _F	--	3.3	--	V	
LCM Luminance	LV	420	470	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

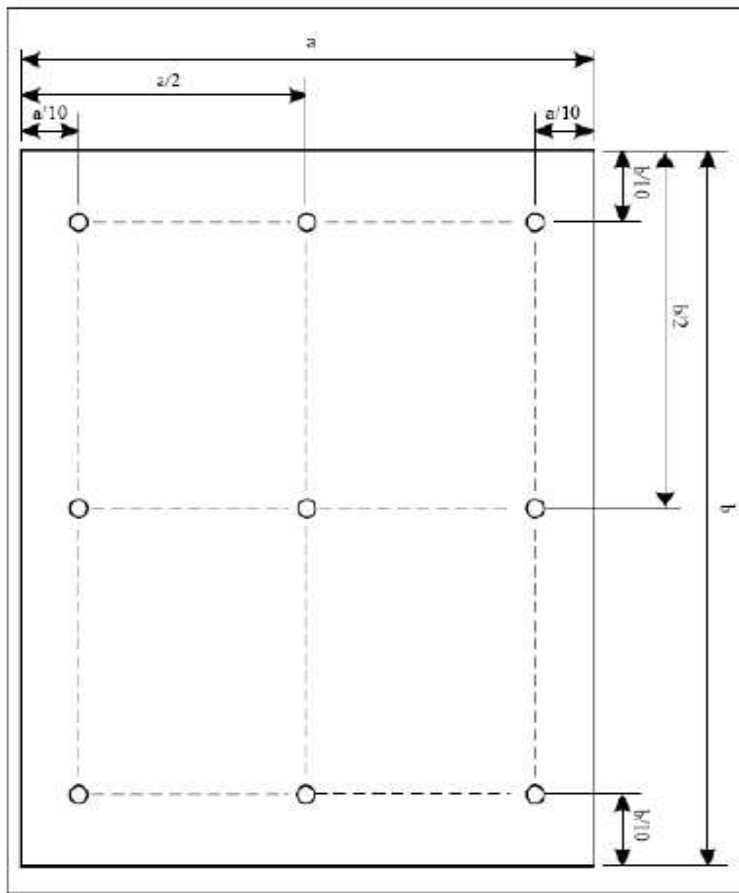
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



Note (3) Luminance Uniformity of these 9 points is defined as below:

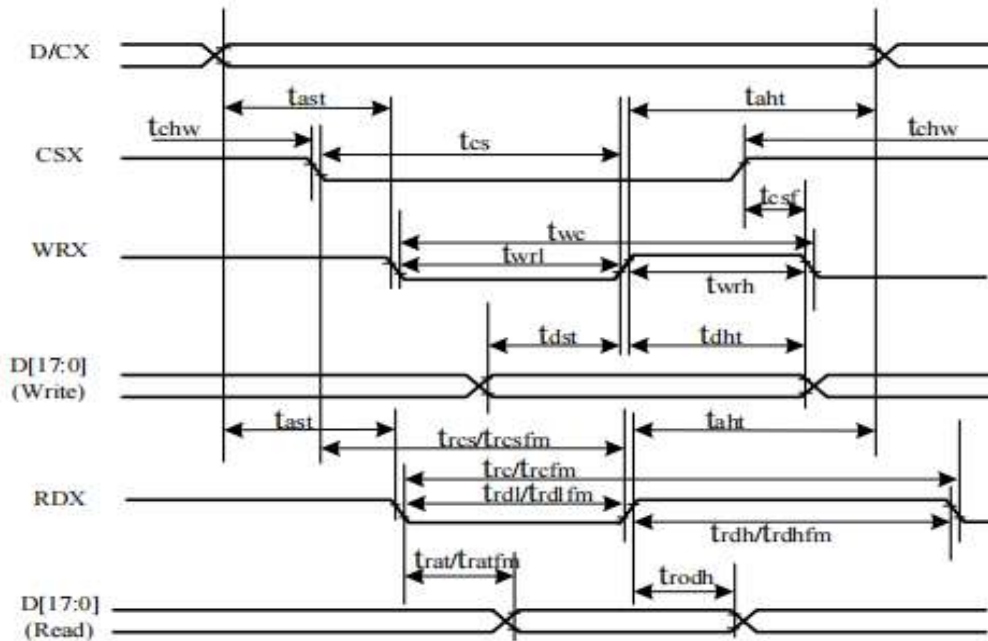


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristic

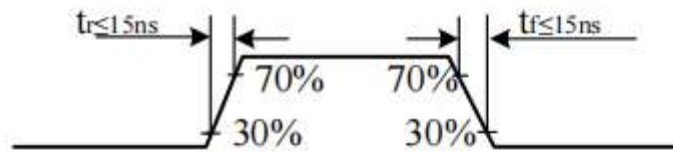
6.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time(Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time(Write)	15	-	ns	
	t _{rcs}	Chip Select setup time(Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time(Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write Cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX(FM)	t _{rcfm}	Read Cycle (FM)	380	-	ns	
	t _{rdhfm}	Read Control H duration(FM)	180	-	ns	
	t _{rdlfm}	Read Control L duration(FM)	200	-	ns	
RDX(ID)	t _{rc}	Read Cycle (ID)	160	-	ns	
	t _{rdh}	Read Control H pulse duration	90	-	ns	
	t _{rdl}	Read Control L pulse duration	70	-	ns	
D[17:0], D[15:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF
	t _{dht}	Write data hold time	10	-	ns	
D[8:0], D[7:0]	t _{rat}	Read access time	-	40	ns	For minimum CL=8pF
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

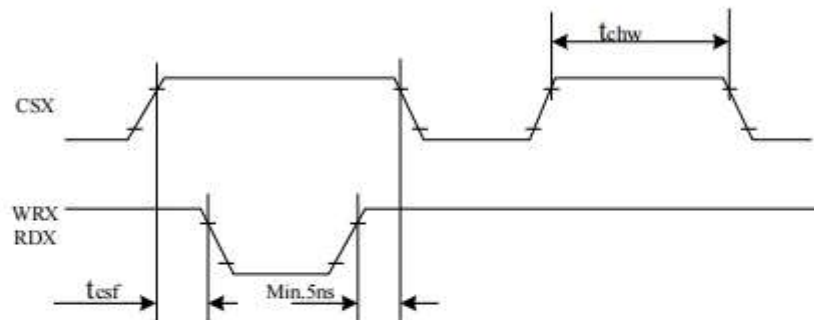
Note: T_a = -30 to 70 °C, I_{OVCC}=1.65V to 3.3V, V_{CI}=2.5V to 3.3V, V_{SS}=0V

Figure91.



CSX timings :

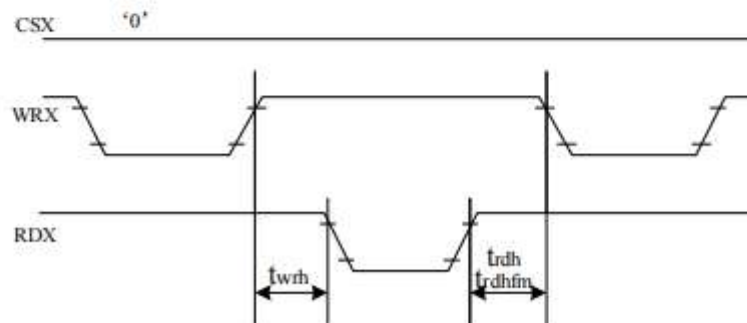
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

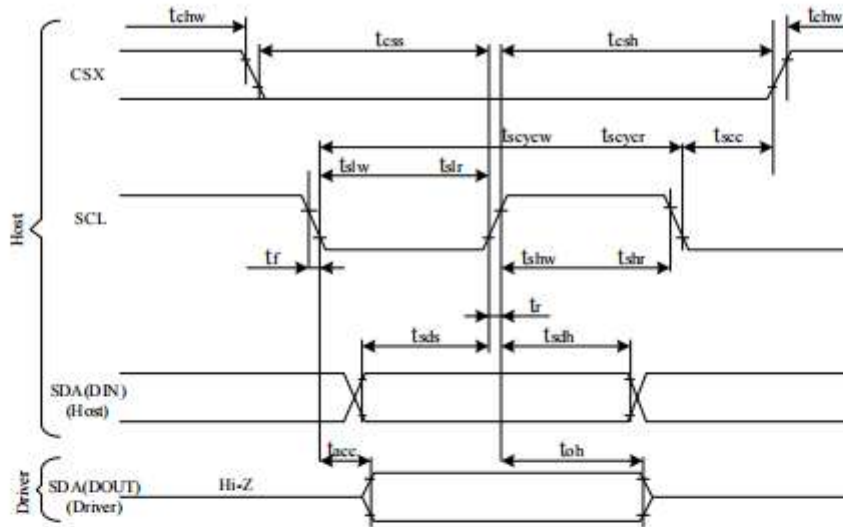
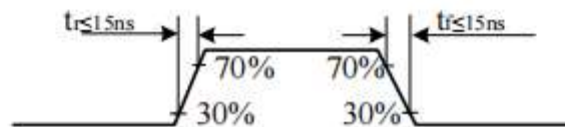


Table 47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Output)	tacc	Access time (Read)	10	-	ns	
CSX	tsec	SCL-CSX	10	-	ns	
	tchwh	CSX "H" Pulse Width	10	-	ns	
	tess	CSX-SCL Time	20	-	ns	
	tesh		40	-	ns	

Note: $T_a = 25^\circ\text{C}$, $IOVCC = 1.65\text{V to } 3.3\text{V}$, $VCI = 2.5\text{V to } 3.3\text{V}$, $VSSA = VSSC = 0\text{V}$

Figure98.



6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

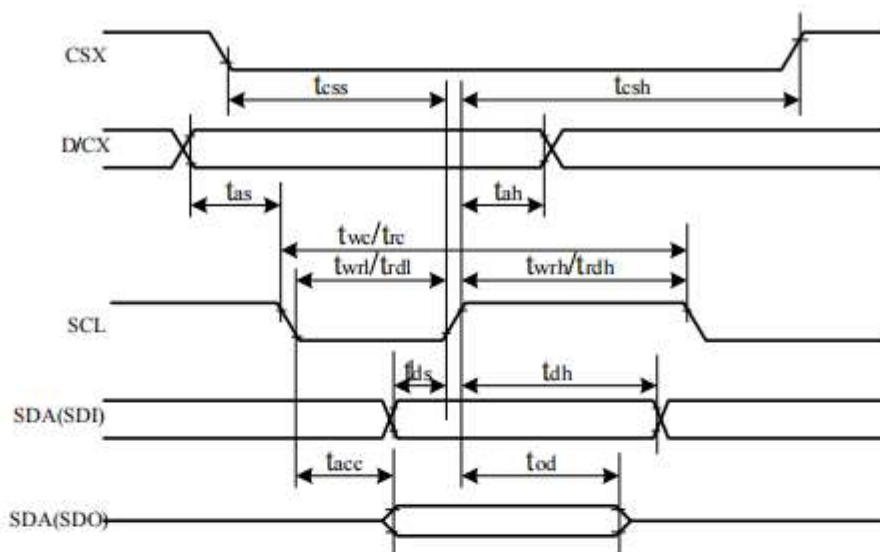
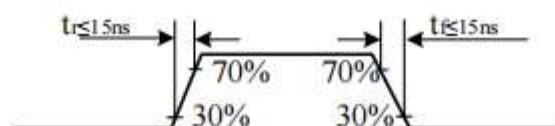


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tesh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: $T_a = 25\text{ }^{\circ}\text{C}$, $IOVCC=1.65V$ to $3.3V$, $VCI=2.5V$ to $3.3V$, $AGND=VSS=0V$

Figure99.



6.4 Parallel 18/16/6-bit RGB Interface Timing Characteristics

Figure100.

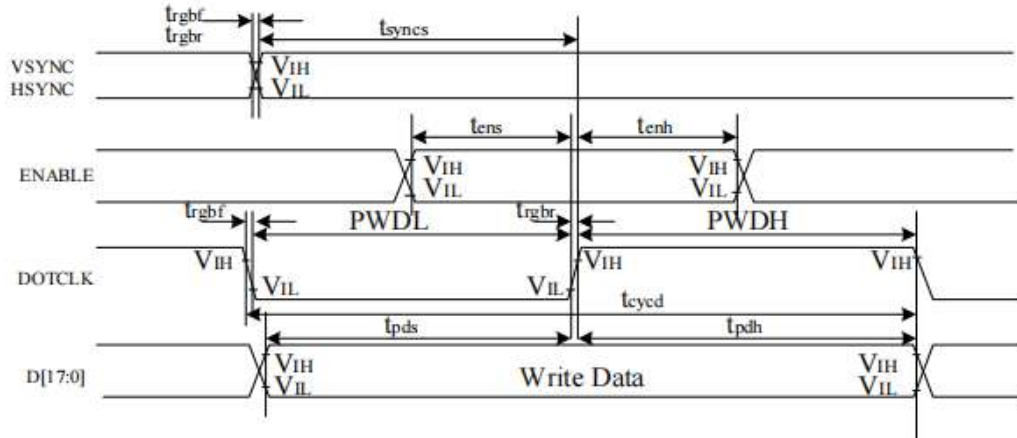
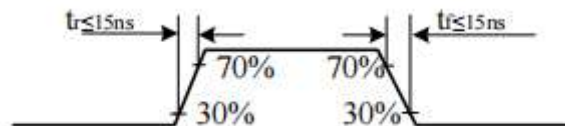


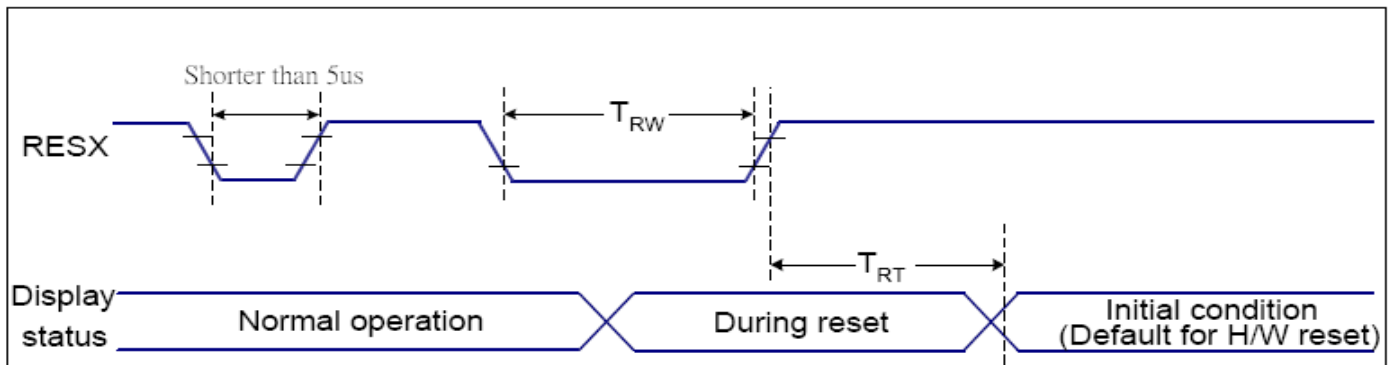
Table49.

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PDDL	DOTCLK low-level period	15	-	ns	
	tcyed	DOTCLK cycle time	100	-	ns	
	trgbf, trgbr	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PDDL	DOTCLK low-level pulse period	15	-	ns	
	tcyed	DOTCLK cycle time	100	-	ns	
	trgbf, trgbr	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70°C , $IOVCC = 1.65\text{V}$ to 3.3V , $VCI = 2.5\text{V}$ to 3.3V , $AGND = VSS = 0\text{V}$



6.5 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, $T_a = -30 \sim 70^\circ\text{C}$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

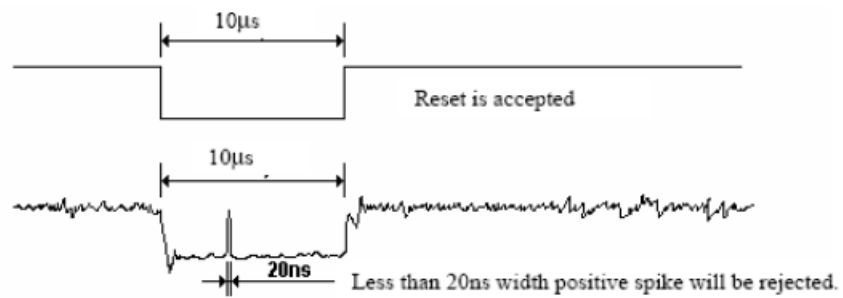
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

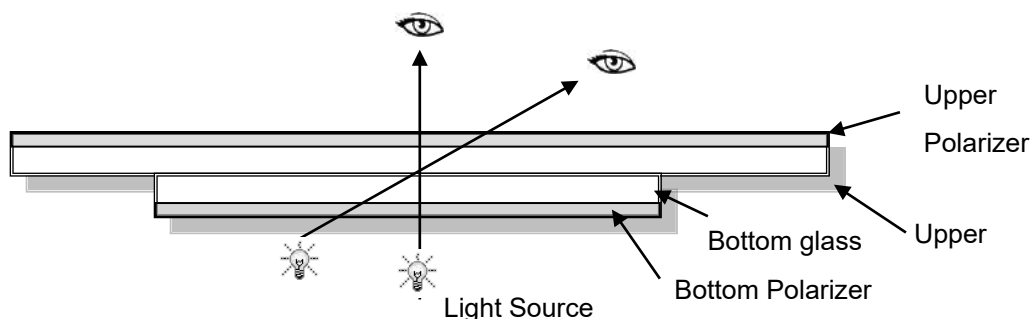
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

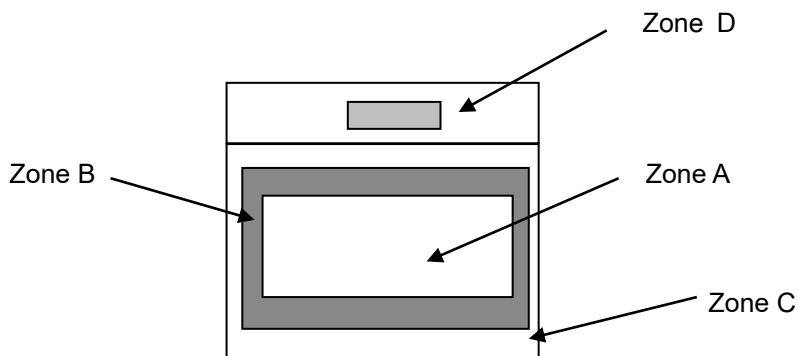
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

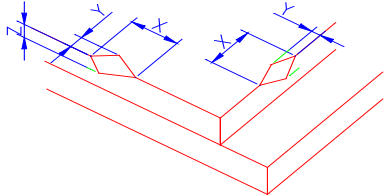
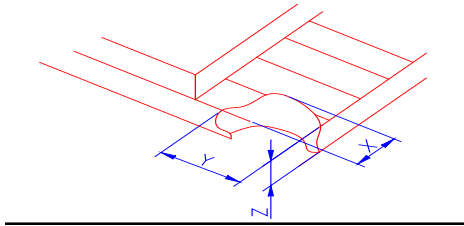
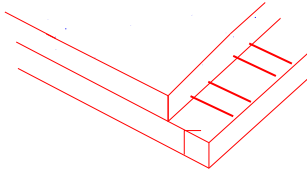
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc...	Major
2	Missing	Missing components and etc...	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc...	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

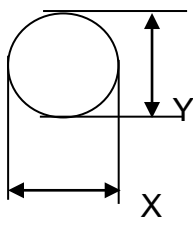
7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)
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1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

2.0

Spot defect



$\Phi=(X+Y)/2$

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 6\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 6\text{mm}$)		
$\Phi > 0.4$	0		

② Dim spot (light leakage、dent、dark spot, etc)

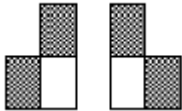
Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 6\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 6\text{mm}$)		
$\Phi > 0.4$	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.5$	2(distance $\geq 6\text{mm}$)		
$\Phi > 0.5$	0		

④ Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.4$	3(distance $\geq 6\text{mm}$)		
$\Phi > 0.4$	0		

3.0	LCD Pixel defect	<table> <tr> <th>Item</th><th>Zone A</th><th>Acceptable Qty</th></tr> <tr> <td rowspan="3">Bright dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td rowspan="3">Dark dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>Distance</td><td> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td>5mm</td></tr> <tr> <td colspan="2">Total bright and dark dot</td><td>$N \leq 4$</td></tr> </table> Note: A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture:   2 dot adjacent   2 dot adjacent (vertical) 2 dot adjacent (slant)	Item	Zone A	Acceptable Qty	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qty																							
Bright dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Dark dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	Width(mm)	Length(m m)	Acceptable Qty		
				A	B	C
		$\Phi\leq0.03$	Ignore	Ignore		Ignore
		$0.03<W\leq0.04$	$L\leq3.0$	$N\leq2$		
		$0.04<W\leq0.05$	$L\leq2.0$	$N\leq1$		
		$W>0.05$	Define as spot defect			
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite				
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.				
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.				

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C, 96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HRS	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10°C, 30 min ↔ +60°C, 30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330, 5points/panel Air: ±8KV, 5times; Contact: ±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition)	
Box Drop Test	1 Corner 3 Edges 6 faces, 80 _{cm} (MEDIUM BOX)	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water (Resistance > 10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

10. Packing

----TBD-----