

http://www.orientdisplay.com

SPECIFICATION FOR LCD MODULE

MODULE NO: AFU12801024G-19.0-EG01V0 REVISION NO: 01

Customer's Approval:

	SIGNATURE	DATE
PREPARED BY (RD ENGINEER)	HCL	2010-01-07
CHECKED BY	VITO H	2010-01-07
APPROVED BY	VITO H	2010-01-07

Contents

1. Handling Precautions	4
2. General Description	5
2.1 Display Characteristics	6
3. Functional Block Diagram	11
I/F PCB Interface:.	11
Mating Type	11
4. Absolute Maximum Ratings	12
4.1 Absolute Ratings of TFT LCD Module	12
4.2 Absolute Ratings of Backlight Unit	12
4.3 Absolute Ratings of Environment	12
5. Electrical characteristics	14
5.1 TFT LCD Module	14
5.2 Backlight Unit	16
6. Signal Characteristic	17
6.1 Pixel Format Image	17
6.2 The Input Data Format	18
6.4 Interface Timing	20
6.5 Power ON/OFF Sequence	23
7. Connector & Pin Assignment	24
7.1 TFT LCD Module	24
7.2 Backlight Unit	25
8. Reliability Test	26
9. Mechanical Characteristi c	28

Record of Revision

Version & Date Page		Page	Old Description	New Description	Remark	
00	2009/10/07	All	First Edition for Customer			
01	2010/1/7	All	Final version			

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the Cold Cathode Fluorescent Lamp (CCFL) reflector edge. Instead, press at the far ends of the CCFL reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold Cathode Fluorescent Lamp (CCFL) in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

AFU12801024G-19.0-EG01V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD panel, a driver circuit, and a backlight system. The screen format is intended to support the SXGA (1280(H) x 1024(V)) screen and 16.7M colors (RGB 6-bits + HiFRC data). All input signals are 2 -channel LVDS interface compatible. Inverter card of backlight is not included.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 $^\circ\!\!C$ $\,$ condition:

ltems	Unit	Specifications
Screen Diagonal	[mm]	482.6 (19.0")
Active Area	[mm]	376.32 (H) x 301.06 (V)
Pixels H x V		1280(x3) x 1024
Pixel Pitch	[mm]	0.294 (per one triad) x 0.294
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance	[cd/m ²]	450 (center, Typ) @ 7.5mA
Contrast Ratio		1000 : 1 (Тур)
Optical Response Time	[msec]	5 ms(Typ, on/off)
Nominal Input Voltage VDD	[Volt]	+5.0 V
Power Consumption	[Watt]	26.71 W (Typ) (PDD= 5.5 W, @Lamp=7.5mA)
Weight	[Grams]	2400 (TYP)
Physical Size (H x V x D)	[mm]	396 (H) x 324 (V) x 18.5 (D) (Typ)
Electrical Interface		Dual channel LVDS
Surface Treatment		Hard-coating (3H), Non-Glare treatment
Support Color		16.7M colors (RGB 6-bit data + HiFRC data)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		KOHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 $\,^\circ\!\mathbb{C}\,$ (Room Temperature):

ltem	Unit	Cond	itions	Min.	Тур.	Max.	Note			
		Horizontal CR = 10	(Right) (Left)	75 75	85 85	-				
		Vertical CR = 10	(Up) (Down)	70 70	80 80	-				
	[degree]	Horizontal CR = 5	(Up) (Down)	75 75	85 85	-	1			
		Vertical CR = 5	(Up) (Down)	75 75	85 85	-				
Luminance Uniformity	[%]	9 Points		75	80	-	2, 3			
Optical Response Time		R is ing		-	3.6	5.7	4, 6			
	[msec]	Falling		-	1.4	2.3				
		Rising + Falli	ng	-	5	8				
		Red x		0.617	0.647	0.677				
		Red y		0.310	0.340	0.370				
		Green x		0.258	0.288	0.318				
Color / Chromaticity		Green y		0.575	0.605	0.635	4			
(CIE)		Blue x		0.115	0.145	0.175	4			
		Blue y		0.041	0.071	0.101				
		White x		0.283	0.313	0.343				
		White y		0.299	0.329	0.359				
White Luminance (At CCFL= 7.5mA)	[cd/m ²]			360	450	-	4			
Contrast Ratio				600	1000	-	4			
Cross Talk (At 60Hz)	[%]			-	-	1.5	5			
Flicker	[dB]			-	-	-20	7			

Note 1: Definition of viewing angle, measured by ELDIM (EZContrast 88)

Viewing angle is the measurement of contrast ratio ≥ 10 , or ≥ 5 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2:9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance v alues by the minimum test point luminance. And measured by TOPCON SR-3



Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5: Definition of Cross Talk (CT) and measured by TOPCON SR-3 CT = | YB – YA | / YA \times 100 (%)

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



Note 6: Definition of response time, measured by WESTAR TRD-100A

The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 7: Subchecker Pattern



Method: Record dBV & DC value with (WESTAR)TRD-100



3. Functional Block Diagram

The following diagram shows the functional block of the 19.0 inches Color TFT-LCD Module:



I/F PCB Interface: FI-XB30SSL-HF15 / MSBKT2407P30HB Mating Type:

FI-X30HL (Locked Type)

FI-X30H (Unlocked Type)

4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 Absolute Ratings of TFT LCD Module

ltem	Symbol	Min.	Max.	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+6	[Volt]	Note 1, 2

4.2 Absolute Ratings of Backlight Unit

ltem	Symbol	Min.	Max.	Unit	Conditions
CCFL Current	ICFL	-	8.0	[mA] rms	Note 1, 2

4.3 Absolute Ratings of Environment

ltem	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	ТОР	0	+50	[°C]	
Operation Humidity	HOP 5 90 [%RH]		[%RH]	Noto 2	
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	90	[%RH]	

Note 1: With in Ta= 25 $^{\circ}$ C

Note 2: Permanent damage to the device may occur if exceed maximum values Note 3: For quality performance, please refer to Incoming Inspection Standard.



5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows:

Symbol	Parameter	Min	Тур	Max	Unit	Condition
VDD	Logic/LCD Drive Voltage	4.50	5.00	5.50	[Volt]	±10%
IDD	Input Current	-	1.10	1.31	[A]	VDD= 5.0V,All black Pattern, At 60Hz
IDD	Input Current	-	1.37	1.63	[A]	VDD= 5.0V,H- Stripe Pattern, At 75Hz Note1
PDD	VDD Power	-	5.50	6.55	[Watt]	VDD= 5.0V,All black Pattern, At 60Hz
PDD	VDD Power	-	6.85	8.15	[Watt]	VDD= 5.0V,H- Stripe Pattern, At 75Hz
IRush	Inrush Current	-	-	2.5	[A]	Note2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	VDD= 5.0V,All black Pattern, At 75Hz

Note 1: The H-Stripe pattern is defined as below :

	1	2	3	•	• •	1278	1279	1280	R →	Gray level = L255
1st Line	<mark>r</mark> g b	<mark>r</mark> g b	<mark>r</mark> g b			R G B	RGB	R G B	G→	Gray level = L255
									B→	Gray level = L255
	<mark>R</mark> G B	<mark>r</mark> g b	<mark>r</mark> g b	•	•••	R G B	R G B	R G B		Gray level = LO
•										
	•	•	•		•	•	•	•		
					-					
•	•	•	•		•	•	•	•		
	•	•	•		•	•	•	•		
•	R G B	RGB	R G B			R G B	RGB	RGB		
-				-						
	R G B	R G B	R G B	•	•••	R G B	R G B	R G B		
1024th Line										

Note 2: Measurement conditions:



Vin rising time

5.2 Backlight Unit

Parameter guideline for CCFL Inverter is under stable conditions at 25°C (Room Temperature):

Parameter	Min. °C	Тур.	Max. 🗆	Unit	Condition		
CCFL Operation Current(IRCFL)		7.5	8.0	[mA] rms	Note 2		
CCFL Frequency(FCFL)	40	60	80	[KHz]	Note 3,4		
CCFL Ignition Voltage(ViCFL, Ta= 0°C)		1200	1440	[Volt] rms	Noto F		
CCFL Ignition Voltage(ViCF, Ta= 25° C)		1000 1200 [[Volt] rms	NOLE 5		
CCFL Operation Voltage (VCFL)	-	707 (@ 7.5mA)	-	[Volt] rms	Note 6		
CCFL Power Consumption(PCFL)	-	21.21	-	[Watt]	Note 6		
CCFL Life Time(LTCFL)	50,000	-	-	[Hour]	Note 7		

Note 1: Typ. are OD recommended design points.

- *1 All of characteristics listed are measured under the condition using the test inverter.
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
- *4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
- Note 2: CCFL standard current is measured at 25 \pm 2°C.
- Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.
- Note 4: The frequency range will not affect to lamp life and reliability characteristics.
- Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,200 voltage. Lamp units need 1,200 voltage minimum for ignition.
- Note 6: The variance of CCFL power consumption is $\pm 10\%$. Calculator value for reference (ISCFL \times VCFL \times 4 = PCFL)
- Note 7: Definition of life: brightness becomes 50%. The typical life time of CCFL is on the condition at 7.5 mA lamp output current.

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

		1			2			12	279)	1280		
1st Line	R	G	В	R	G	В		R	G	В	R	G	В
		י י			۱ ۱				י י			•	
		•			•		1		•			•	
		•							•				
		•											
		•			•		,		•	•			
		•			, ,							•	
		•			۰ ۱		, ,				, ,		
1024th Line	R	G	В	R	G	В		R	G	В	R	G	В

6.2 The Input Data Format



Note1: Normally DE mode only. VS and HS on EVEN channel are not used. Note2: Please follow VESA.

Note3: 8-bit in

6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVD S is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

PIN #	SIGNAL NAME	DESCRIPTION
1	RxOIN0-	Negative LVDS differential data input (Odd data)
2	RxOIN0+	Positive LVDS differential data input (Odd data)
3	RxOIN1-	Negative LVDS differential data input (Odd data)
4	RxOIN1+	Positive LVDS differential data input (Odd data)
5	RxOIN2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
6	RxOIN2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
7	VSS	Power Ground
8	RxOCLKIN-	Negative LVDS differential clock input (Odd clock)
9	RxOCLKIN+	Positive LVDS differential clock input (Odd clock)
10	RxOIN3-	Negative LVDS differential data input (Od d data)
11	RxOIN3+	Positive LVDS differential data input (Od d data)
12	RxEIN0-	Negative LVDS differential data input (Ev en data)
13	RxEIN0+	Positive LVDS differential data input (Ev en data)
14	VSS	Power Ground
15	RxEIN1-	Negative LVDS differential data input (Ev en data)
16	RxEIN1+	Positive LVDS differential data input (Ev en data)
17	VSS	Power Ground
18	RxEIN2-	Negative LVDS differential data input (Ev en data)
19	RxEIN2+	Positive LVDS differential data input (Ev en data)
20	RxECLKIN-	Negative LVDS differential clock input (Ev en clock)
21	RxECLKIN+	Positive LVDS differential clock input (Ev en clock)
22	RxEIN3-	Negative LVDS differential data input (Ev en data)
23	RxEIN3+	Positive LVDS differential data input (Ev en data)
24	VSS	Power Ground
25	VSS	Power Ground
26	NC	Do not connect (for OD test)
27	VSS	Power Ground
28	VCC	+5.0V Power Supply
29	VCC	+5.0V Power Supply
30	VCC	+5.0V Power Supply

Note1: Start from left side



Note2: Input signals of odd and even clock shall be the same timing. Note3: Please follow VESA.

6.4 Interface Timing

6.4.1 Timing Characteristics

Signal	ltem	Symbol	Min	Тур	Max	Unit
Vertical Section	Period	Tv	1032	1066	1150	Th
	Active	Tdisp(v)	1024	1024	1024	Th
	Blanking	Tbp(v)+Tfp(v)+PWvs	8	42	126	Th

	Period	Th	780	844	2047	Tclk
Horizontal	Active	Tdisp(h)	640	640	640	Tclk
Section	Blanking	Tbp(h)+Tfp(h)+PWhs	140	204	-	Tclk
	Period	Tclk	22.2	18.52	14.81	ns
Clock	Frequency	Freq.	45	54	67.5	MHz
Frame Rate	Frequency	1/Tv	50	60	75	Hz

Note : DE mode only

6.4.2 Timing Diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power	Sea	uence	Timina
	Jug	actice	· · · · · · · · · · · · · · · · · · ·

Daramotor		Value	Unit	
Parameter	Min.	Тур.	Max.	Offic
T1	0.5	-	10	[ms]
T2	0	40	50	[ms]
Т3	300	-	-	[ms]
T4	300	-	-	[ms]
T5	0.5	16	50	[ms]
T6	-	-	-	[ms]
Т7	1000	-	-	[ms]

7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components .

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	JAE / STM
Type Part Number	FI-XB30SSL-HF15 / MSBKT2407P30HB
Mating Housing Part Number	I-X30HL

7.1.2 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	R xOIN0-	2	RxOIN0+
3	R xOIN1-	4	RxOIN1+
5	R xOIN2-	6	RxOIN2+
7	VSS	8	RxOCLKIN-
9	RxOCLKIN+	10	R xOIN3-
11	R xOIN3+	12	R xE INO-
13	R xE IN0+	14	VSS
15	R xE IN 1-	16	RxEIN1+
17	VSS	18	R xEIN2-
19	R xE IN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	R xE IN 3+	24	VSS
25	VSS	26	NC
27	VSS	28	VCC
29	VCC	30	VCC

7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Lamp Connector / Backlight lamp
Manufacturer	CVILUX / YEONHO
Type Part Number	CP0502SL090/35001HS-02L
Mating Type Part Number	CP0502P1ML0/ 35001 WR-02L

7.2.1 Signal for Lamp connector

	Connector No.	Pin No.	Input	Color	Function
Upper	CN1	1	Hot1	Pink	High Voltage
		2	Cold1	White	Low Voltage
	CN2	1	Hot2	blue	High Voltage
		2	Cold2	black	Low Voltage

	Connector No.	Pin No.	Input	Color	Function
Lower	CN3	1	Hot1	Pink	High Voltage
		2	Cold1	White	Low Voltage
	CN4	1	Hot2	blue	High Voltage
		2	Cold2	black	Low Voltage

8. Reliability Test

Environment test conditions are listed as following table.

ltems	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 5 0°C, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta=0°C, 300hours	
High Temperature Storage (HTS)	Ta=60°C, 300hours	
Low Temperature Storage (LTS)	Ta=- 20°C, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: $\pm X$, $\pm Y$, $\pm Z$ (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20 °C /30min, 60 °C/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: \pm 8KV, 150pF(330 Ω) 1sec, 9 points, 25 times/ point.	2
	Air Discharge: \pm 15KV, 150pF(330 Ω) 1sec 9 points, 25 times/ point.	2
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost Self-recoverable. No hardware failures.

9. Mechanical Characteristic



