SPECIFICATION
OF
LCD MODULE

MODULE NO: AFY240320A0-2.8N6NTN-R

Customer Approval:

☐ **Accept** ☐ **Reject**

FUTURE FOCUS	SIGNATURE	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

Sample Version	Doc. Version	DATE	DESCRIPTION	CHECKED BY
0001	A0	2013-03-26	First Release	

CONTENTS

NUMBER SYSTEM INTRODUCTION:

AFY240320A0-2.8N6NTN-R:

AF: Orient Display TFT;

Y: JAZZ TFT;

240320: Length * width pixel;

A0: Product Version;

2.8: Diagonal Dimension;

N: LCD Mode (N: TN; I: IPS; V: VA)

6: Viewing Direction (6-> 6:00; 12->12:00; Unavailable for IPS and VA);

N: Temperature Range (N: Normal; W: Wide);

T: Polarizer (T:Transmissive; F:Transflective);

N: Luminance (N: Normal <300 nit; M: Middle >=300 & <600 nit;
H: High >=600 nit);

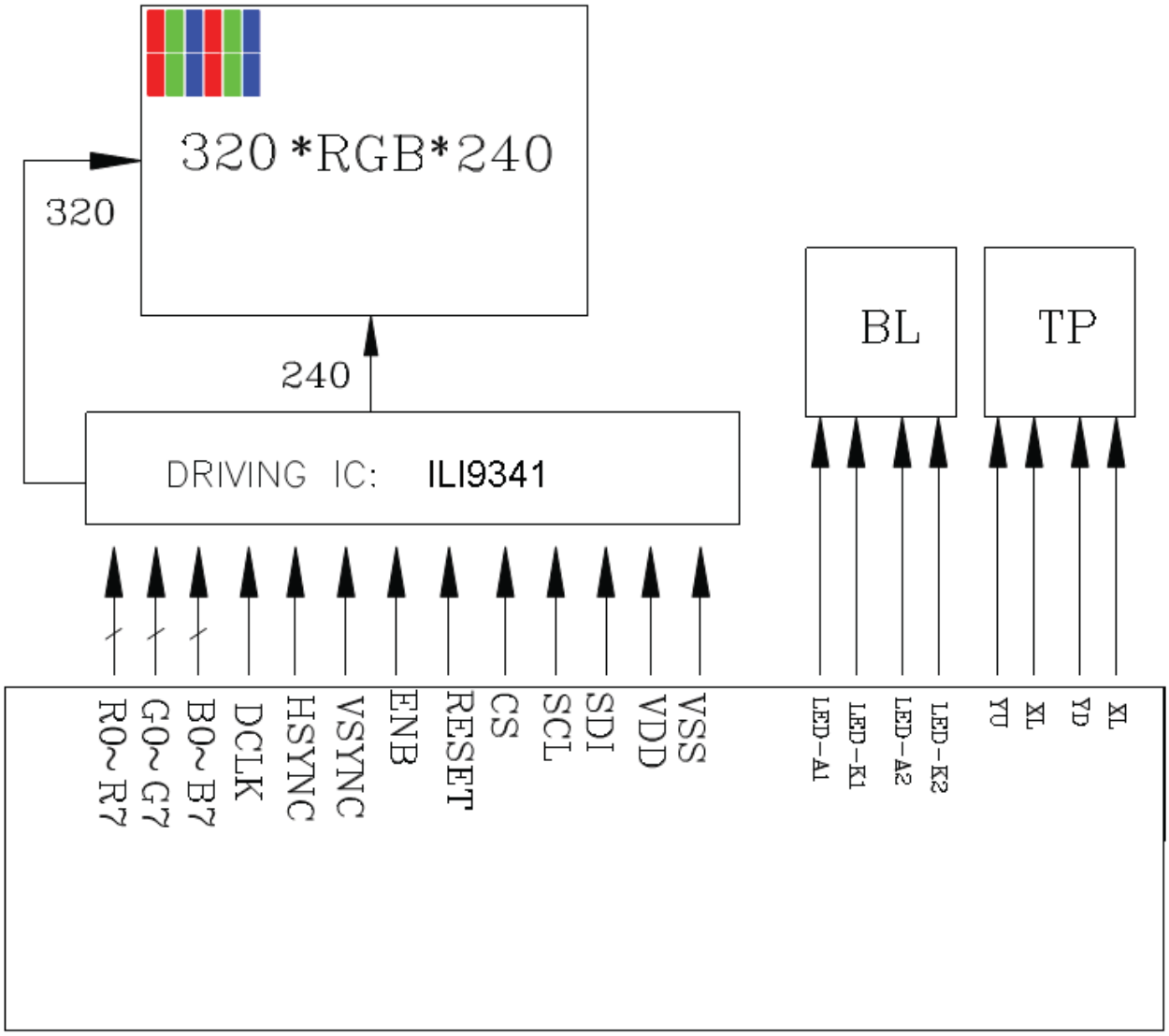
R: TP Option (R: Resistive TP; C: Capacitive TP; N: Without TP);

1. GENERAL SPECIFICATIONS

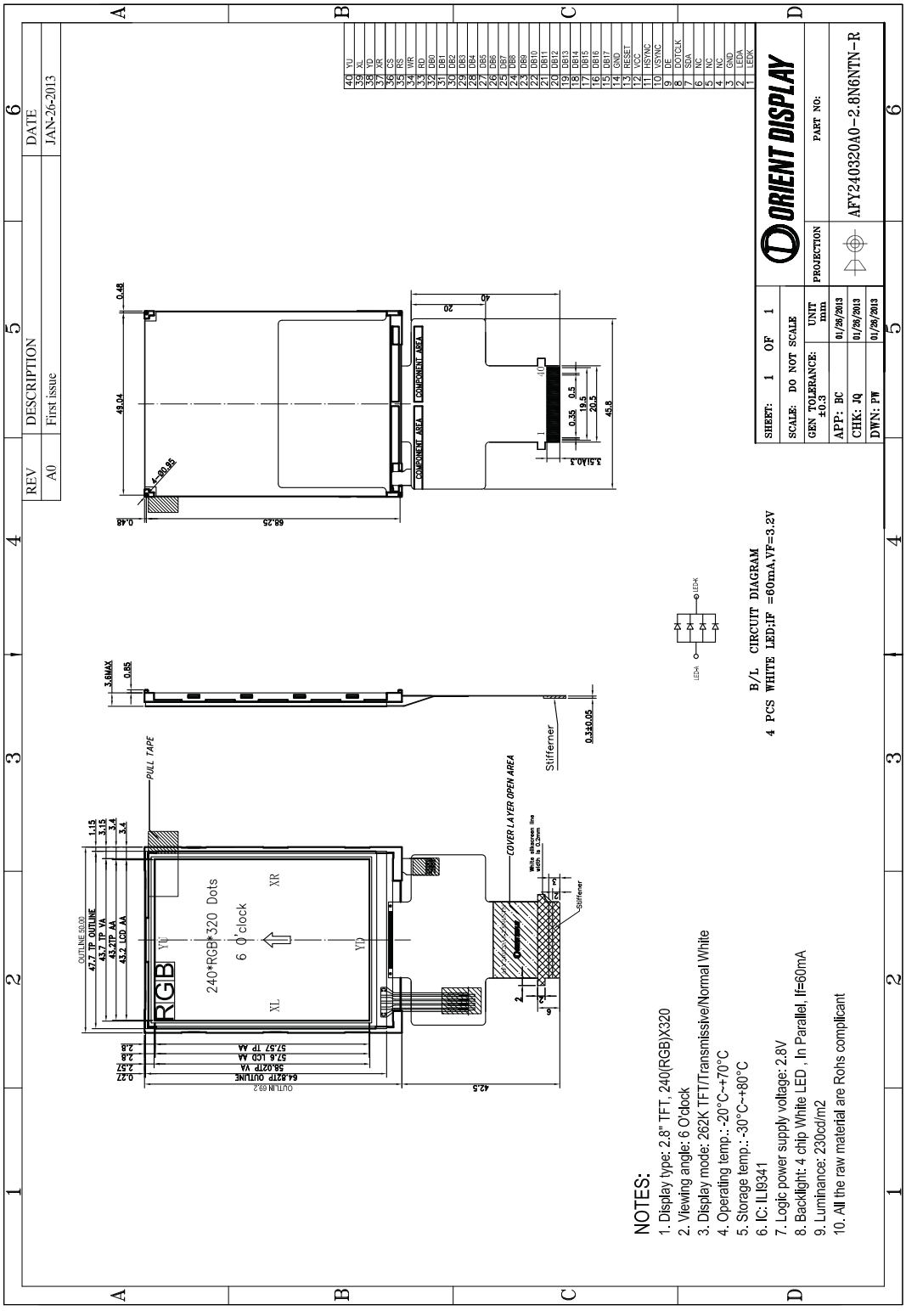
ITEM	SPECIFICATION	UNIT
OUTLINE DIMEMSIONS	50(W) X69.2 (H) X3.6 (D)	mm
DISPLAY SIZE	2.8	inch
DOT PITCH	0.18mmX0.18mm	mm
NUMBER OF DOTS	240*（RGB）*320	-
DRIVER IC	ILI9341	-
LCD TYPE	TFT(262K) TRANSMISSIVE	-
INTERFACE	MCU 18 BITS	
BACKLIGHT TYPE	LED White	-
VIEWING DIRECTION	6 O'clock	-
GRAY SCALE INVERSION DIRECTION	12 O'clock	

***See attached drawing for details.**

2. BLOCK DIAGRAM



3. DIMENSIONAL OUTLINE

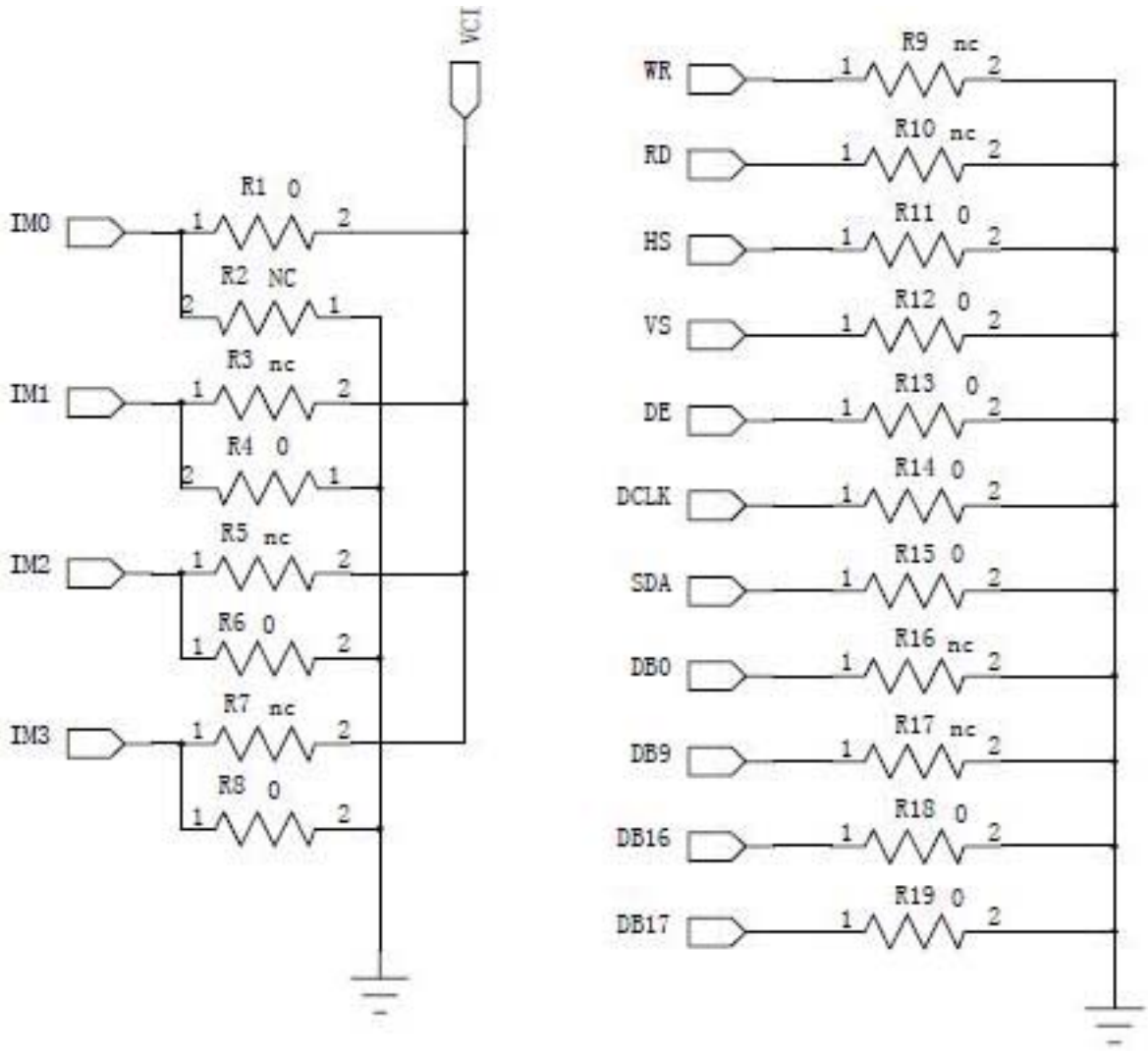


4. PIN DESCRIPTION

<table>
<tr><th>NO.</th><th>PIN NAME</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>LEDK</td><td>P</td><td>Power supply for LED (Cathode)</td></tr>
<tr><td>2</td><td>LEDA</td><td>P</td><td>Power supply for LED (Anode)</td></tr>
<tr><td>3</td><td>GND</td><td>P</td><td>Ground(0V)</td></tr>
<tr><td>4~6</td><td>NC</td><td>-</td><td>No connection</td></tr>
<tr><td>7</td><td>SDA</td><td>I/O</td><td>SPI Serial Data Input/output</td></tr>
<tr><td>8</td><td>DOTCLK</td><td>I</td><td>Pixel clock signal</td></tr>
<tr><td>9</td><td>DE</td><td>I</td><td>Data enable</td></tr>
<tr><td>10</td><td>VSYNC</td><td>I</td><td>Vertical synchronizing signal</td></tr>
<tr><td>11</td><td>HSYNC</td><td>I</td><td>Horizontal synchronizing signal</td></tr>
<tr><td>12</td><td>VCC</td><td>P</td><td>Power voltage</td></tr>
<tr><td>13</td><td>RESET</td><td>I</td><td>Reset signal</td></tr>
<tr><td>14</td><td>GND</td><td>P</td><td>Ground(0V)</td></tr>
<tr><td>15~32</td><td>DB17~DB0</td><td>I/O</td><td>Data bus
- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
</table>
Note: Does not support RGB interface</td></tr>
<tr><td>33</td><td>RD</td><td>I</td><td>Read signal, active at low in MCU mode;
In SPI mode, connect to GND</td></tr>
<tr><td>34</td><td>WR</td><td>I</td><td>Write Signal, active at low in MCU mode;
In SPI mode, SPI Serial Clock</td></tr>
<tr><td>35</td><td>RS</td><td>I</td><td>In MCU mode, Register select signal, low is selected data register; High is selected command register. In SPI mode, connect to GND</td></tr>
<tr><td>36</td><td>CS</td><td>I</td><td>Chip selection pin/ Serial port data enable signal</td></tr>
<tr><td>37</td><td>XR</td><td>-</td><td>TP: X right</td></tr>
<tr><td>38</td><td>YC</td><td>-</td><td>TP: Y bottom</td></tr>
<tr><td>39</td><td>XL</td><td>-</td><td>TP: X left</td></tr>
<tr><td>40</td><td>YU</td><td>-</td><td>TP: Y top</td></tr>
</table>

Note: 1: input, 0: output, P: Power

Note: 2: Default interface of this part is “80 MCU 16-bit bus interface I” ([IM3:IM0] =0001), and “HS”, “VS”, “DE”, “DCLK”, “SDA”, “DB16”, “DB17”, already are connected to GND via 0 ohm resistor on FPC. Refer to below circuit.



5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min	Max		
Power Supply for Pump	VCC	-0.3	4.5	V	
Operating temperature range	To	-20	70	Degree C	
Storage temperature range	Ts	-30	80	Degree C	
Logic input voltage range	VI	-0.3	VCC+0.3	V	
Logic input voltage range	VO	-0.3	VCC+0.3	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics

5.2 DC Characteristics

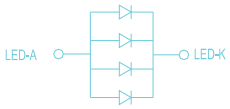
Item	Symbol	Values			Unit	Conditions
		Min	Typ	Max		
Low Level Input Voltage	Vil	GND	-	0.3xVCC	v	
High Level Input Voltage	Vih	0.7xVCC	-	VCC	uA	
High Level Output Voltage	Voh	VCC-0.4	-	VCC	ohm	
Low Level Output Voltage	Vol	GND	-	GND+0.4	uA	
Power Supply	VCC	2.5	2.8	3.3	V	
Input Leakage Current	Iil			±1.0	uA	
Pull High/Low Resistor	Rp	-	100K	-	ohm	

5.3 DC Backlight Unit

Item	Symbol	Min	Typ	Max	Unit	Remark
Average luminous Intensity	Iv		230		cd/m2	IF=60mA
Chromaticity Coordinates	X	0.234	0.284	0.334		IF=60mA
	Y	0.273	0.323	0.373		IF=60mA
Forward Voltage	VF		3.2	3.4	V	IF=60mA
Reverse Current	IR			50	μA	VR=5V,1LED
Luminous Tolerance	IV-M	80			%	(MIN/MAX)×100
Power Dissipation	Pd	192			mW	
Peak Forward Current	Ifp	100			uA	
Reverse Voltage	VR	5			V	

B/L CIRCUIT DIAGRAM

4 PCS WHITE LED;IF =60mA,VF=3.2V

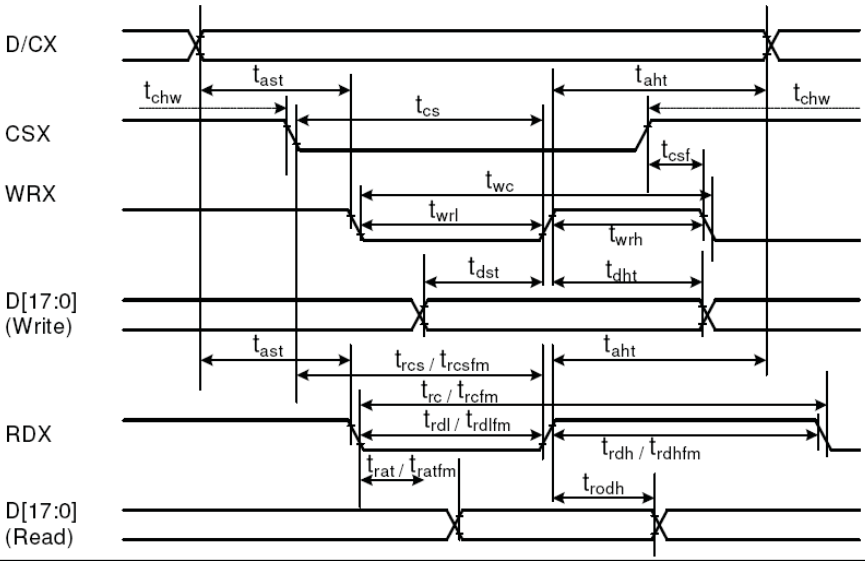


5.4 DC Touch Panel Unit

Item	Symbol	Min	Typ	Max	Unit	Remark
Transparency	-	80	-	-	%	JIS K-7105
Hardness Of Surface	-	-	3	-	H	150gf 45°
FPC Peeling Strength	-	5		-	N	Upward 90°
FPC Bending	-	-	3	-	cycle	R=1.0, 90°
Input Force	60	-		100	gf	-
Rated Voltage	V touch			3	V	DC
X-axis Resistance	Rx	150		500		FPC PIN
X-axis Resistance	Ry	300		850		
Linearity	-	-	±1.5	±2.0	%	-
Chattering	-	-	-	10	ms	-
Insulation Resistance	Ri	20	-	-	MΩ	-

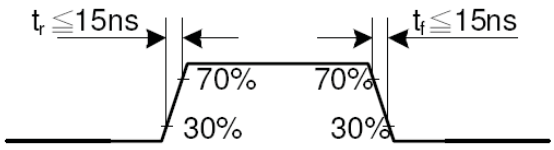
6. INPUT SIGNAL TIMING

6.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-I system)

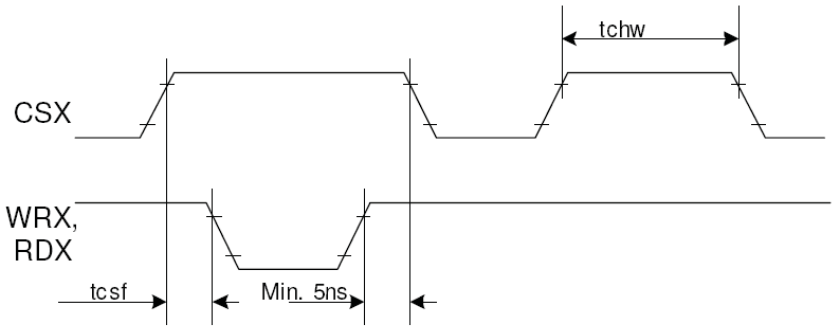


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

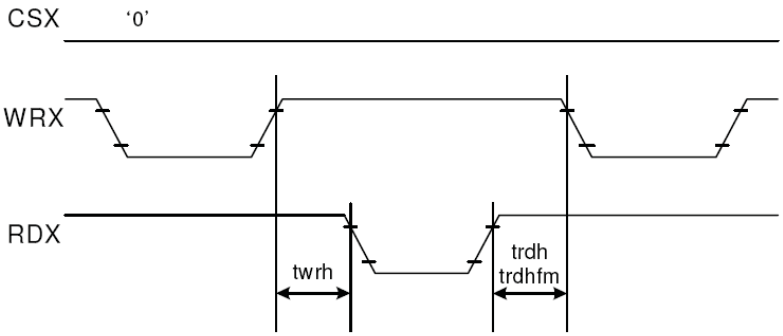


CSX timings :



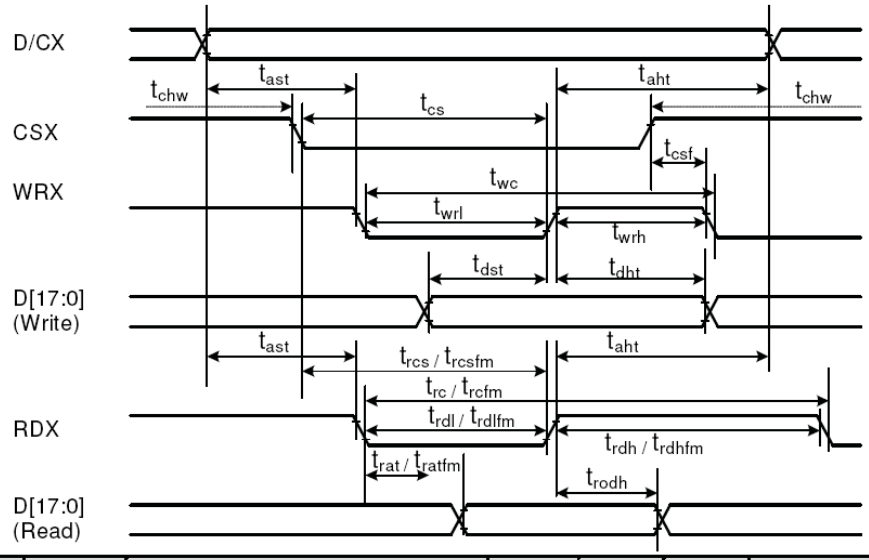
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



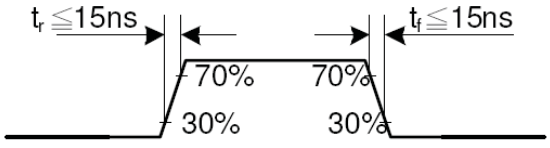
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-II system)

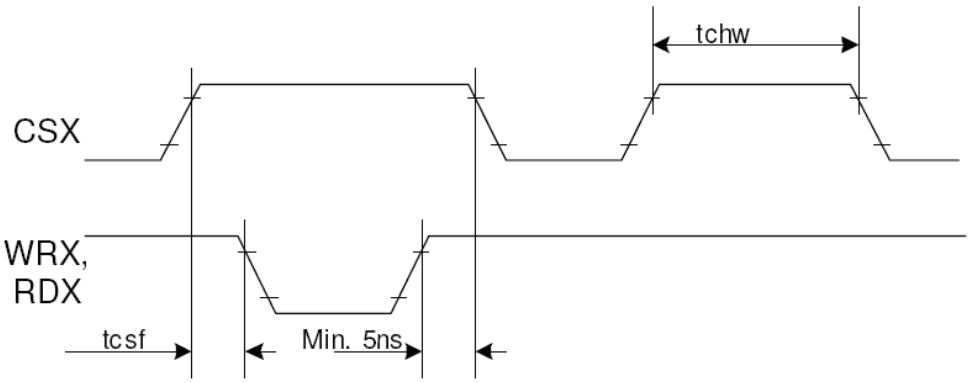


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

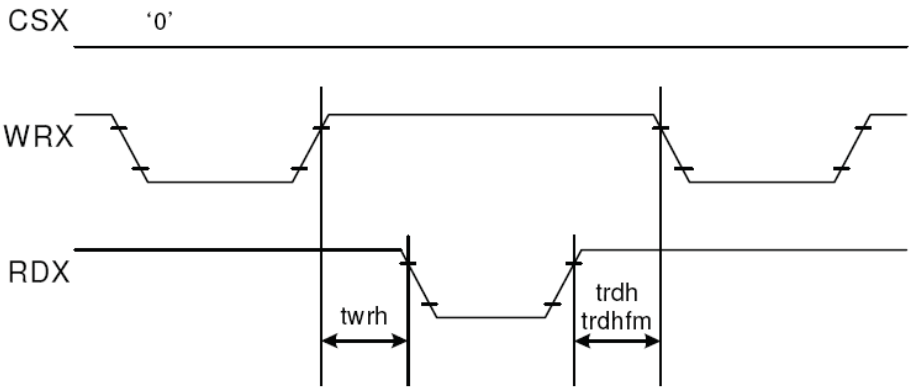


CSX timings：



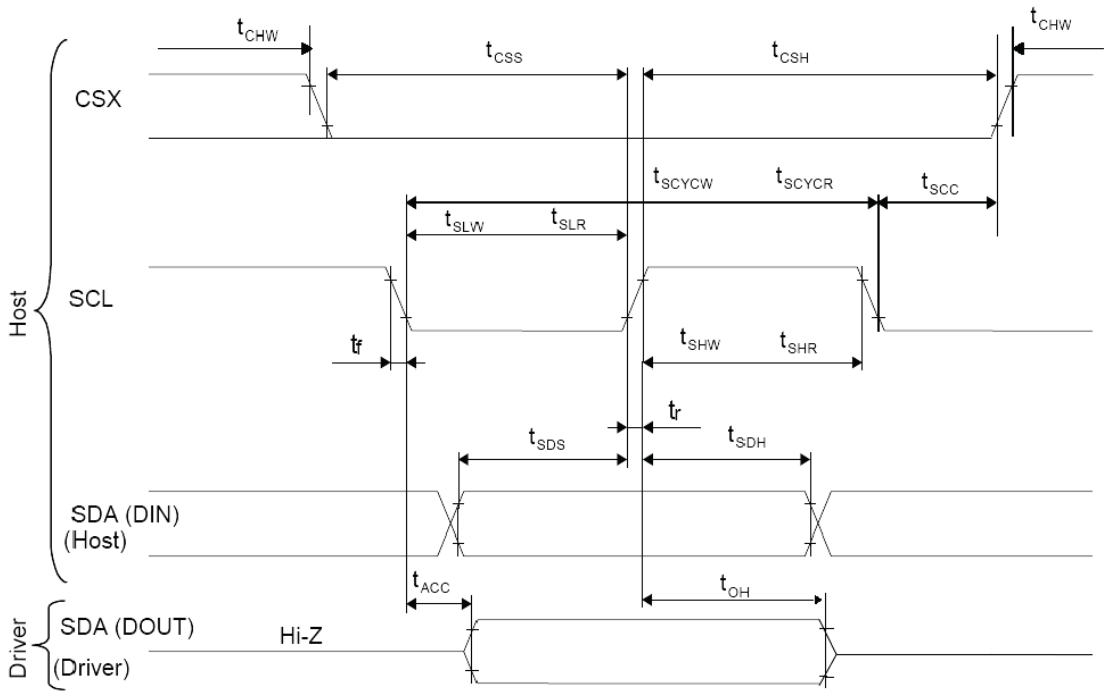
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



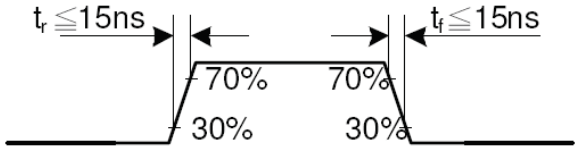
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.3 Display Serial Interface Timing Characteristics (3-line SPI system)

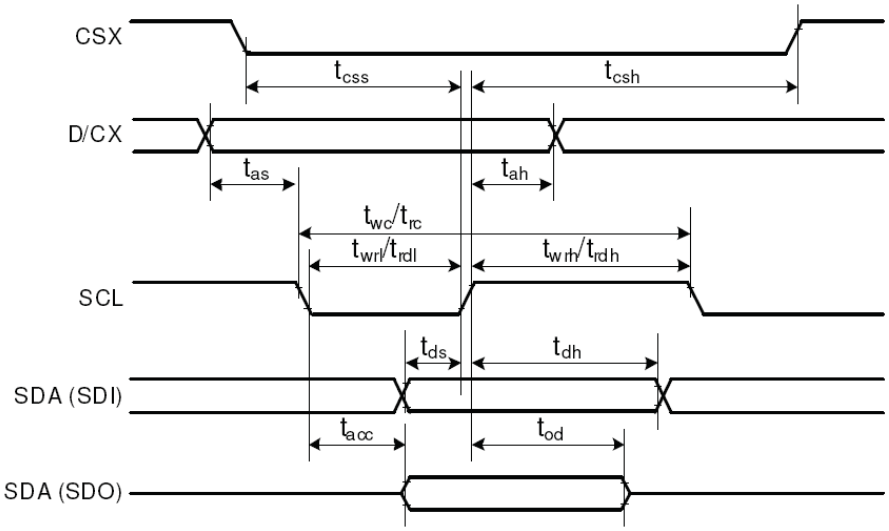


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width (Write)	40	-	ns	
	tslw	SCL “L” Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

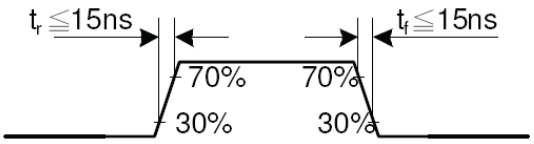


6.4 Display Serial Interface Timing Characteristics (4-line SPI system)

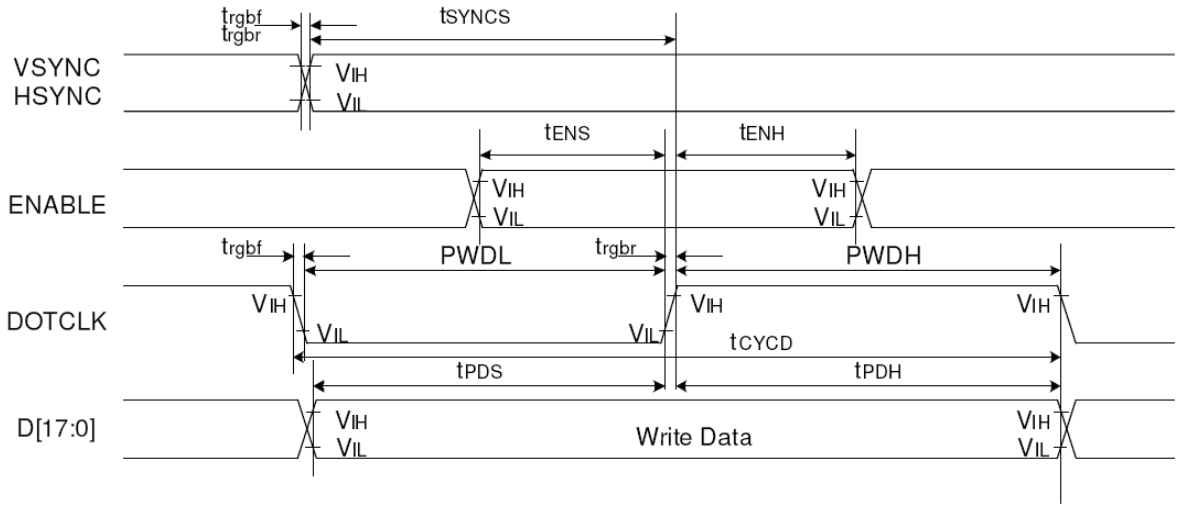


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

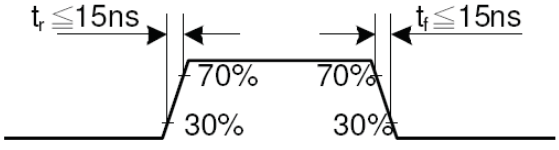


6.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



6.6 Controller Information

IC: ILI9341

Please download IC specification at http://www.orientdisplay.com/pdf/ILI9341.pdf

7. OPTICAL CHARACTERISTICS

Item		Symbol	Conditions	Specifications	Unit	Note
Transmittance		T%	Viewing normal angle $\theta_X = \theta_Y = 0°$	6.0	%	All left side data are based on CMO's following condition – 1.CG : NTSC 59% 2.LC : TN 3.Light Source : CMO LED BLU 4.Film : Nitto Linear Polarizer 5.Machine : DMS
Contrast Ratio		CR		300	--	
Response Time (by Quick)		Ton+ Toff		30	ms	
Viewing Angle	Hor.	θ_{X+}	Center CR>10	60	deg.	
		θ_{X-}		60		
	Ver.	θ_{Y+}		60		
		θ_{Y-}		50		
CF only Chromaticity	Red	X_R	Viewing normal angle $\theta_X = \theta_Y = 0°$	0.631	--	Under C light Simulation
		Y_R		0.316	--	
	Green	X_G		0.298	--	
		Y_G		0.566	--	
	Blue	X_B		0.138	--	
		Y_B		0.122	--	
	White	X_W		0.297	--	
		Y_W		0.327		

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

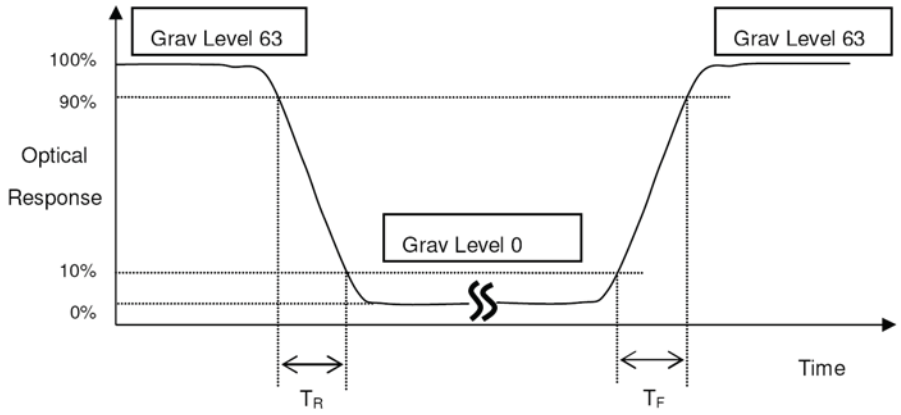
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

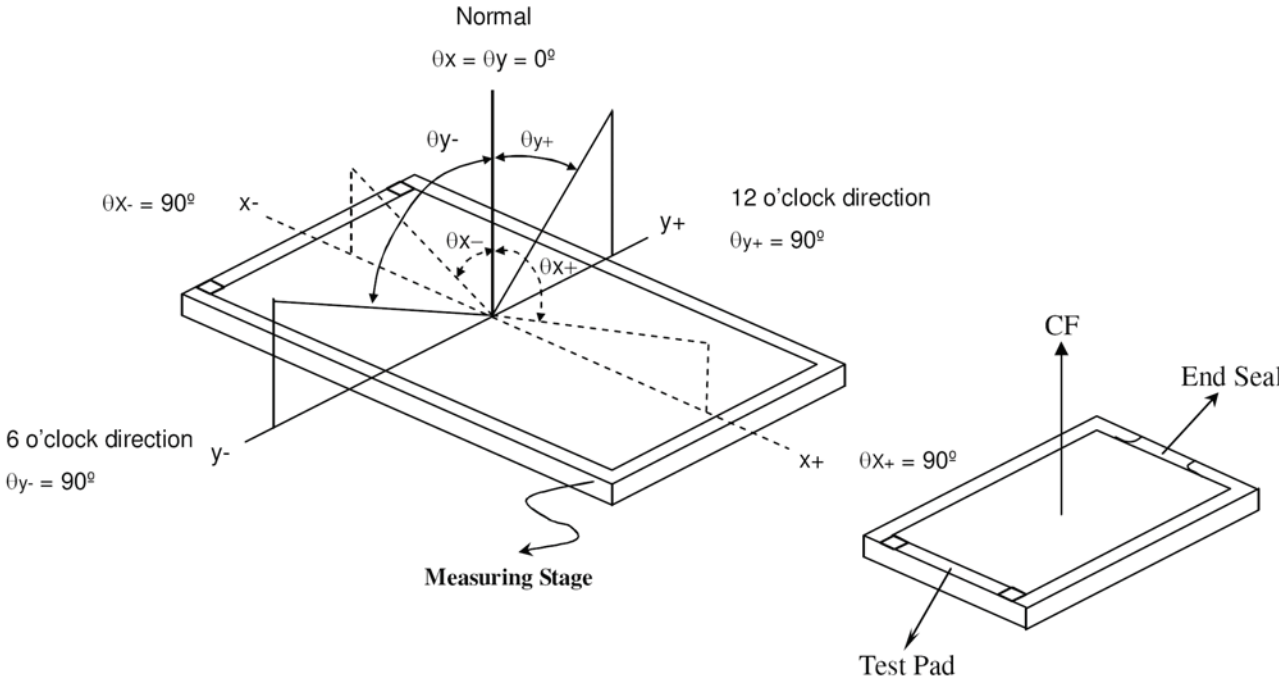
CR = CR (10)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (Ton, Toff):

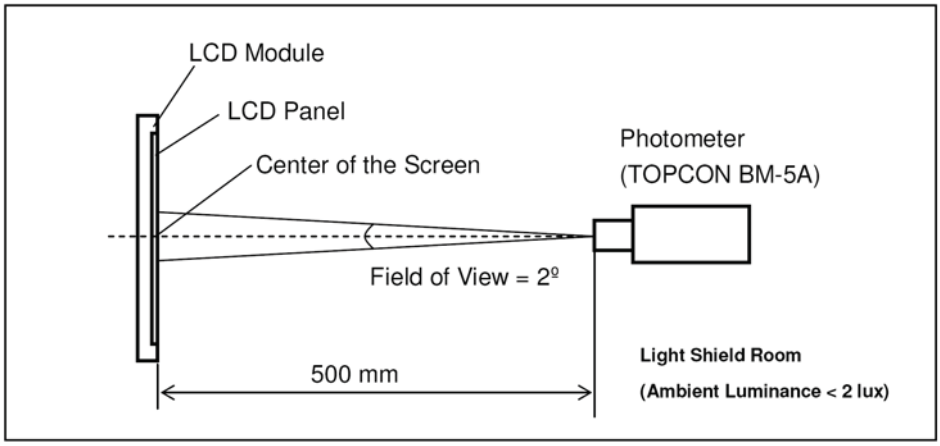


*Note(3) Definition of Viewing Angle

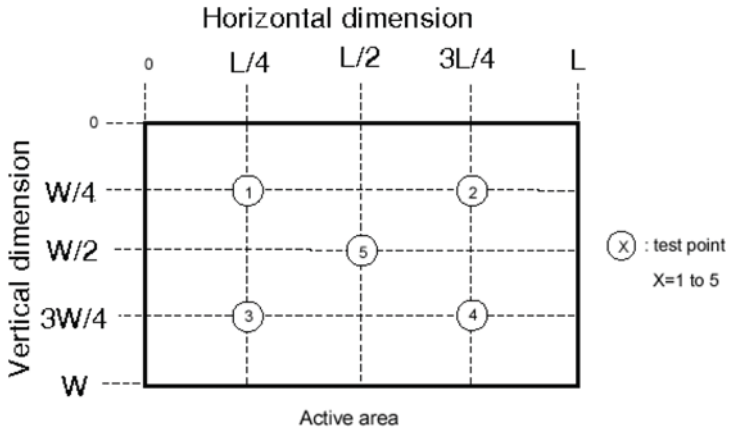


*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (5)



8. RELIABILITY

Please download details at http://www.orientdisplay.com/Reliability.html

9. SPECIFICATION OF QUALITY ASSURANCE

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10. GENERAL PRECAUTIONS

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11. LIMTIED WARRANTY

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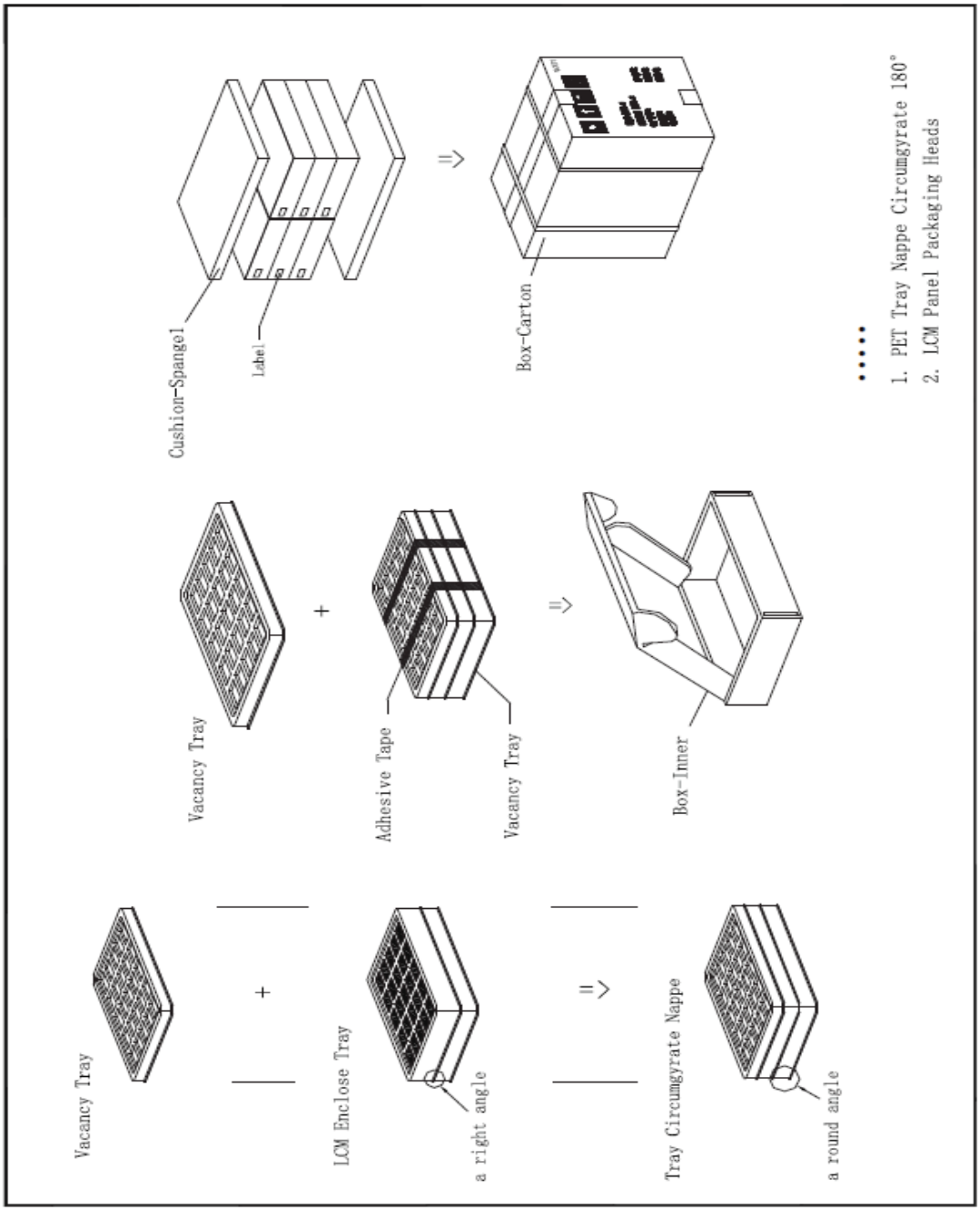
12. PACKAGE



Orient Display Corporation reserves the right to change this specification.