AG6202

HDMI1.4 to VGA Converter

Data Sheet

Official Version

V1.1

January, 2019

Revision History

Version	Date	Notes
1.0	2018/12/6	First release
1.1	2019/1/9	1) Update Features 2) Update Table1: PIN16 Description

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I. General Description

ALGOLTEK AG6202 is a high-performance, cost effective single-chip solution to implement HDMI1.4 high resolution video to VGA converter. With **ALGOLTEK**'s ultra-low power design, AG6202 is able to run stand-alone operation without external power source.

II. Features

- Video resolution support up to 1920x1200@60Hz
- Support Hot Plug Detection
- Crystal-free, an on-chip crystal integration
- Built-in 3.3V and 1.2V voltage regulators
- On-chip HDCP Engine which is compliant with HDCP 1.4 specification
- Integrated on-chip HDCP1.4 Keys
- 1.2V Core power and 3.3V I/O power
- 2KV ESD performance
- Operating temperature range: 0°C to +85°C

III. Device Information

Part Number	Package	Body Size
AG6202-MAQ	QFN-48	6x6 mm^2

IV. Application

- HDMI to VGA dongle
- Docking stations

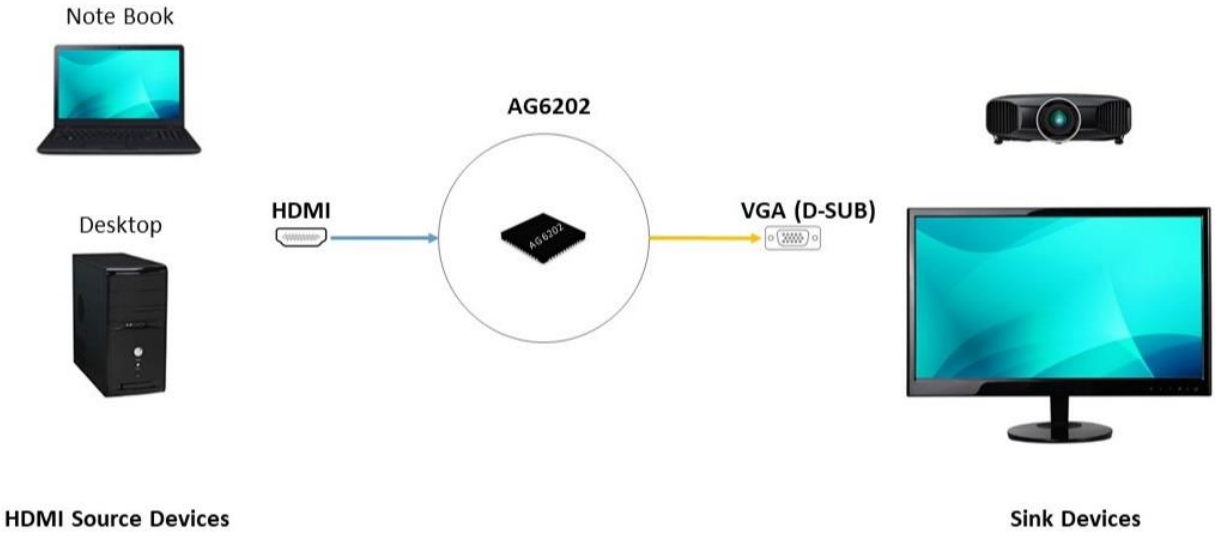


Figure 1 Application for HDMI to VGA Dongle

V. System Block Diagram

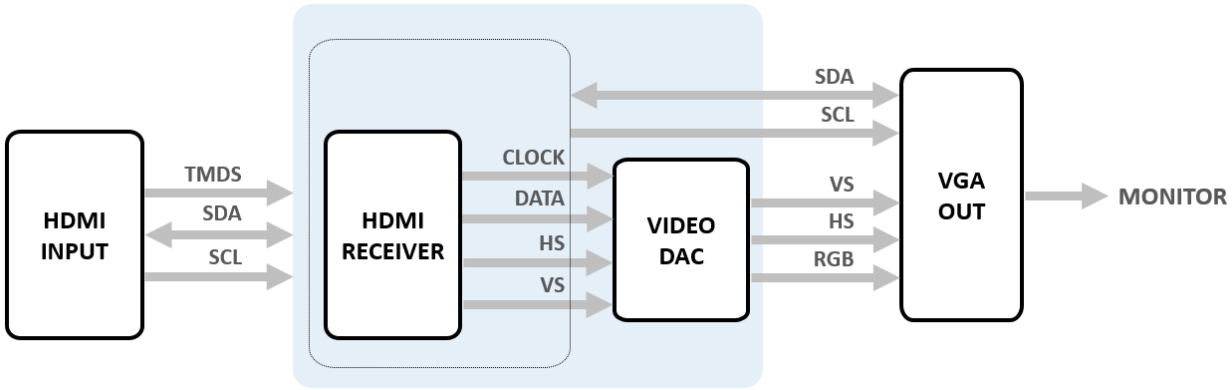


Figure 2 System Block Diagram

VI. Pin Definition and Functions

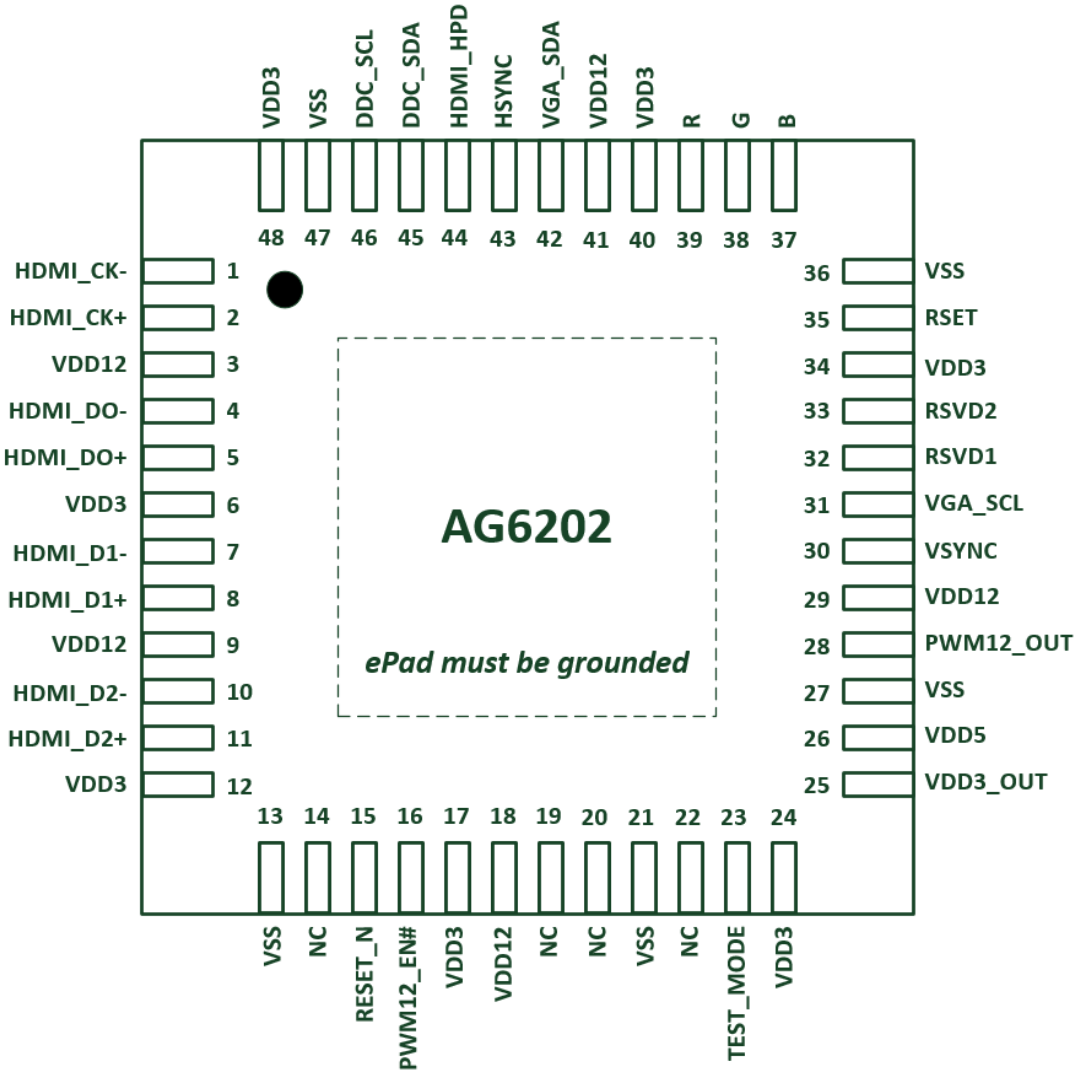


Figure 3 PIN Definition

Table 1 Pin Description

PIN NAME	PIN	TYPE	DESCRIPTION
POWER SUPPLY			
VDD5	26	Power	5V Power input
VDD3	6, 12, 17, 24, 34, 40, 48	Power	3.3V Power input
VDD12	3, 9, 18, 29, 41	Power	1.2V power input
VDD3_OUT	25	Power	On-chip 3.3V regulator power output
PWM12_OUT	28	Power	On-chip PWM 1.2V regulator power output
VSS	13, 21, 27, 36, 47, EPAD	Power	Ground
DIFFERENTIAL HIGH-SPEED IO			
HDMI_CK-	1	Input	HDMI RX clock channel negative
HDMI_CK+	2	Input	HDMI RX clock channel positive
HDMI_D0-	4	Input	HDMI RX data channel 0 negative
HDMI_D0+	5	Input	HDMI RX data channel 0 positive
HDMI_D1-	7	Input	HDMI RX data channel 1 negative
HDMI_D1+	8	Input	HDMI RX data channel 1 positive
HDMI_D2-	10	Input	HDMI RX data channel 2 negative
HDMI_D2+	11	Input	HDMI RX data channel 2 positive
DIGITAL IO			
RESET_N	15	Input	An available external Reset signal for system implementation. Active **LOW** reset signal to the device **Note**: On-chip POR reset is available and this pin ONLY reserved for system HOST adjust reset timing in any unexpected state case.
PWM12_EN#	16	Input	1.2V internal regulator control NC or L = enable (Connect this signal to GND or floating) H = disable (Connect this signal to VDD3)
TEST_MODE	23	Bidirectional	Factory test only Connect this signal to VDD3
VSYNC	30	Output	Vertical sync signal
VGA_SCL	31	Bidirectional	VGA I2C Clock

PIN NAME	PIN	TYPE	DESCRIPTION
RSVD1	32	Bidirectional	Reserved. Connect this signal to VSS
RSVD2	33	Bidirectional	Reserved. Connect this signal to VSS
VGA_SDA	42	Bidirectional	VGA I2C Data
HSYNC	43	Output	Horizontal sync signal
HDMI_HPD	44	Output	HDMI RX Hot-Plug Detect output
DDC_SDA	45	Bidirectional	DDC I2C Data for HDMI Port
DDC_SCL	46	Bidirectional	DDC I2C Clock for HDMI Port
ANALOG IO			
RSET	35	Input	Adjust voltage swing of R/G/B signals Default NC
B	37	Output	Blue channel output
G	38	Output	Green channel output
R	39	Output	Red channel output

VII. Specification

VII.1 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD5	5V supply voltage	-0.5	6.0	V
VDD3	3.3V supply voltage	-0.5	3.63	V
VDD12	1.2V supply voltage	-0.5	1.4	V
T_J	Junction Temperature	0	125	°C

Table 2 Absolute Maximum Rating

VII.2 Normal Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD5	5V supply voltage	4.5	5	5.5	V
VDD3	3.3V supply voltage	3.0	3.3	3.6	V
VDD12	1.2V supply voltage	1.16	1.2	1.32	V
I_{VDD5}*	Total current for 5V supply voltage		200		mA
θ_{JC}	Thermal Resistance (Junction to Case)		2		°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)		33		°C/W
T_A	Ambient Temperature	0	25	85	°C

***Test Conditions:** VDD5: 5.0V
Output resolution: 1080P@60Hz
3.3V and 1.2V internal regulator are enable

Table 3 Normal Operating Conditions

VII.3 DC Characteristics

Digital I/O Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	2.4			V
V_{OL}	Low-level Output Voltage			0.4	V
V_{IH}	High-level Input Voltage	2.0		5.5	V
V_{IL}	Low-level Input Voltage	-0.3		0.8	V
I_{LI}	Input leakage Current			±1	uA

Table 4 Digital I/O Characteristics

VGA DAC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
V_{MAX}	MAX Luminance Voltage (Input Data=FFh)	698	0.7	706.5	mV
V_{MIN}	MIN Luminance Voltage (Input Data=00h)	-0.4	0	0.3	mV
B_{DAC}	Resolution (Each DAC)			8	Bits
E_{OFF}	Offset Error	-0.025		0.043	%FS
E_{GAIN}	Gain Error	-0.29		0.93	%FS
INL	Integral Linearity Error	-1		1	LSB
DNL	Differential Linearity Error	-1		1	LSB
ANALOG OUTPUT					
I_{DAC}	Output Current	2		18.5	mA
E_{CHV}	Video Channel to Video Channel Mismatch (% of Max Luminance Voltage)		2	6	%
T_{Skew}	Video Channel to Video Channel Output Skew		1		ns
$E_{OV/UN}$	Overshoot/Undershoot	-1	0	1	%
$T_{R/F}$	Video Channel Rise/Fall Time	0.5	1	2	ns

Table 5 VGA DAC Characteristics

VII.4 AC Characteristics

HDMI Receiver AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_{DPS}	Intra-Pair Differential Input Skew			0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew			1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance			0.3	T_{bit}
F_{RXC}	TMDS Clock Frequency	25		200	MHz

Table 6 HDMI Receiver AC Characteristics

VIII.Package Outline

VIII.1 Marking

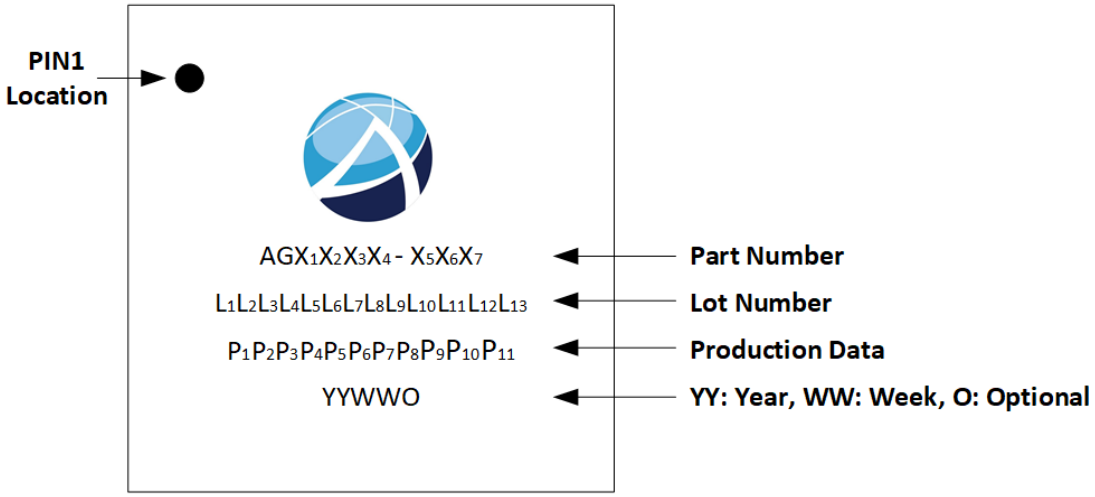
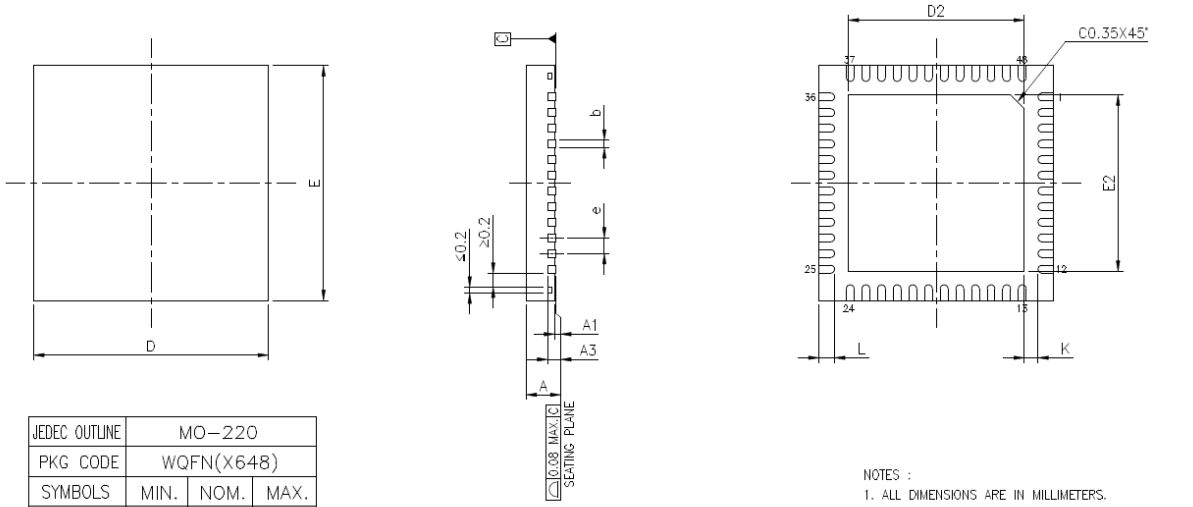


Figure 4 Marking

VIII.2 Package Dimension



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X648)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	VQFN	WQFN	UQFN	TQFN OPTION 1	TQFN OPTION 2
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
185X18* MIL	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	V	X	(W)VJJE-1	V	V	—	—	—

Figure 5 Package Dimension

IX. References

- HDMI Specification Version 1.4b
- VSIS™ Version 1, Rev. 2

X. Contact Information

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