AG6320

DP to HDMI/VGA Converter

Data Sheet

Official Version

V1.3

October, 2017

Revision History

Version	Date	Notes
0.1.0	2017/10/24	Preliminary
1.1.0	2018/10/15	Added another package
1.2	2019/01/23	Revised VGA resolution
1.3	2019/4/29	Update Table4: Add Tj / $\theta_{JC,}$ / θ_{JA}

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I. General Description

ALGOLTEK AG6320 is a single chip solution to implement DisplayPort to HDMI/VGA data converter. AG6320 is a single chip solution which transmits both the video and audio streams via single DisplayPort connector. Its DisplayPort 1.2 receiver supports configurable 1, 2 and 4 lanes @ 1.62Gbps, 2.7Gbps and 5.4Gbps input, and the HDMI supports up to 4K2K@30Hz output. Otherwise, the RGB triple-DAC supports up to 1200P@60Hz output. AG6320 Series also support the external SPI flash for the firmware upgrade for better compatibility and flexibility. It's a good fit for the applications of docking stations, extended display adaptors and dongles for the laptop PC, tablet and smartphone accessory markets..

II. Features

- Embedded 16 bit MCU
- EDID and MCCS pass-through supported
- Supports Hot Plug Detection
- External SPI flash supported for firmware upgrade
- Embedded HDCP 1.4 supported
- HDMI 1.4b TX supports 4K@30Hz output
- VGA supports 1920x1200p@60Hz output
- Simultaneously display via HDMI and VGA outputs
- 2KV ESD performance
- Down Spread Spectrum Clock (SSC) supported

III. Device Information

Part Number	Package	Body Size	Note
AG6320-MAQ	QFN-88	10x10 mm^2	/w I^2S audio output
AG6320-MBQ	QFN-88	10x10 mm^2	/w I^2S audio output /w USB DP_DM

IV. Application

- DP dongle

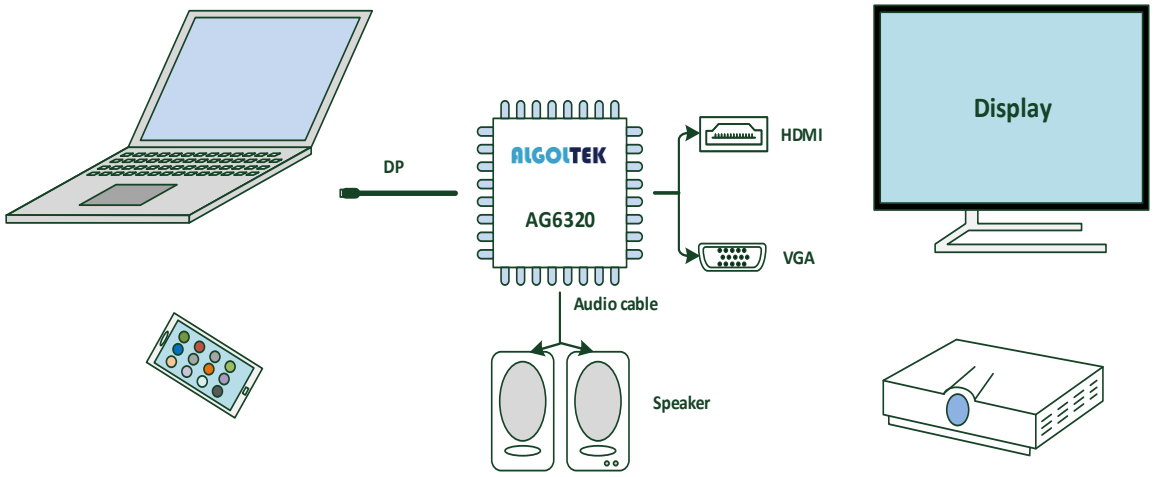


Figure 1 Application for DP to HDMI/VGA Dongle

V. System Block Diagram

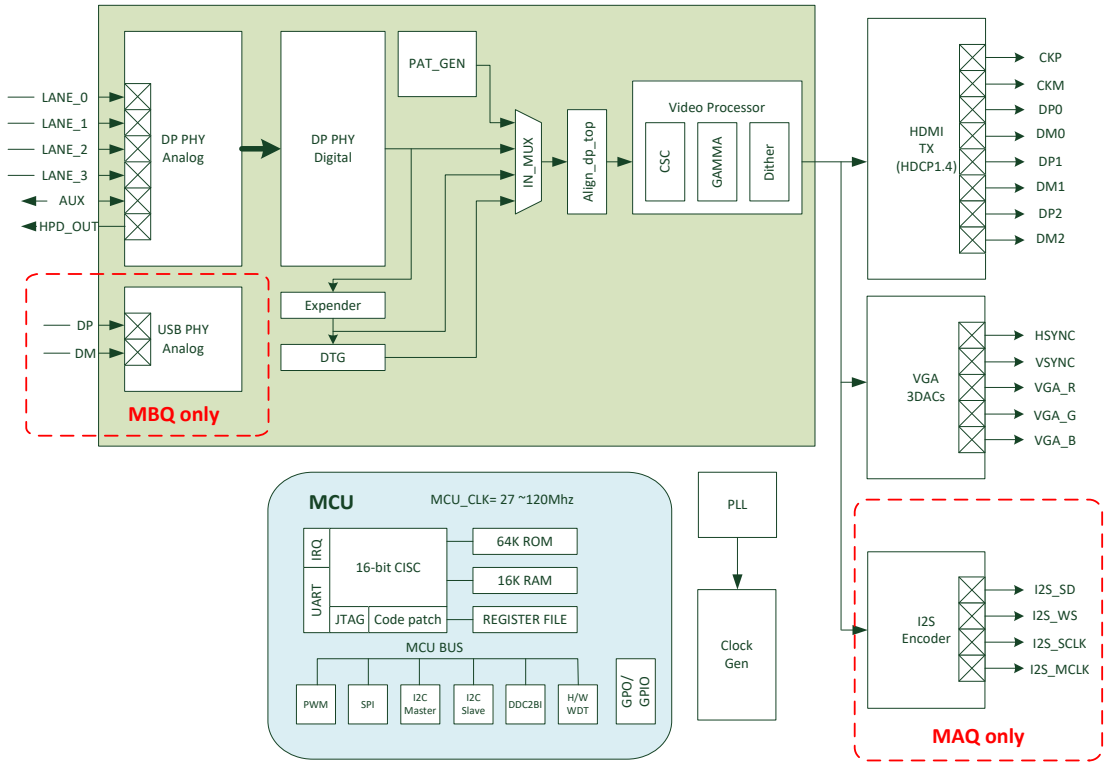


Figure 2 System Block Diagram

VI. Pin Mapping and Description

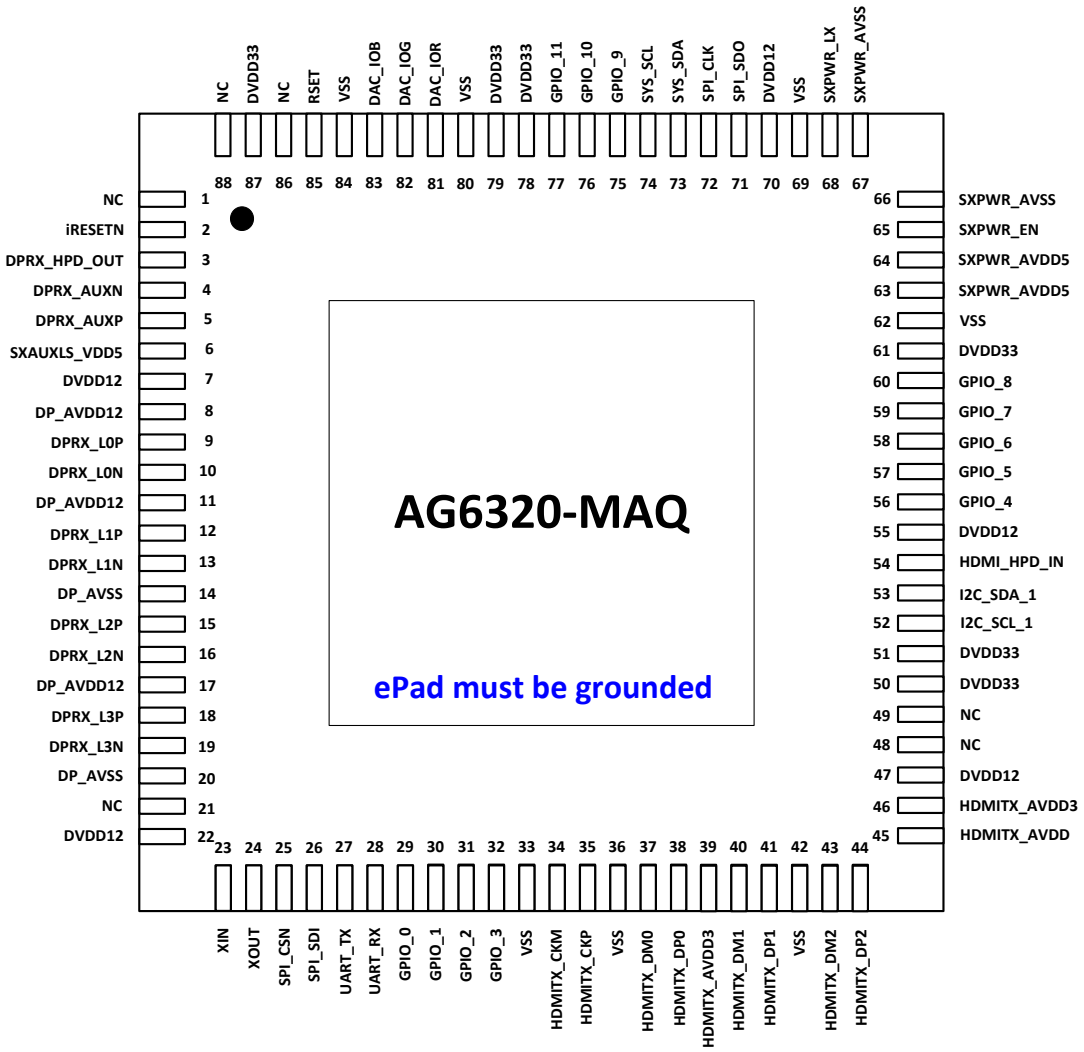


Figure 3 AG6320-MAQ PIN Mapping

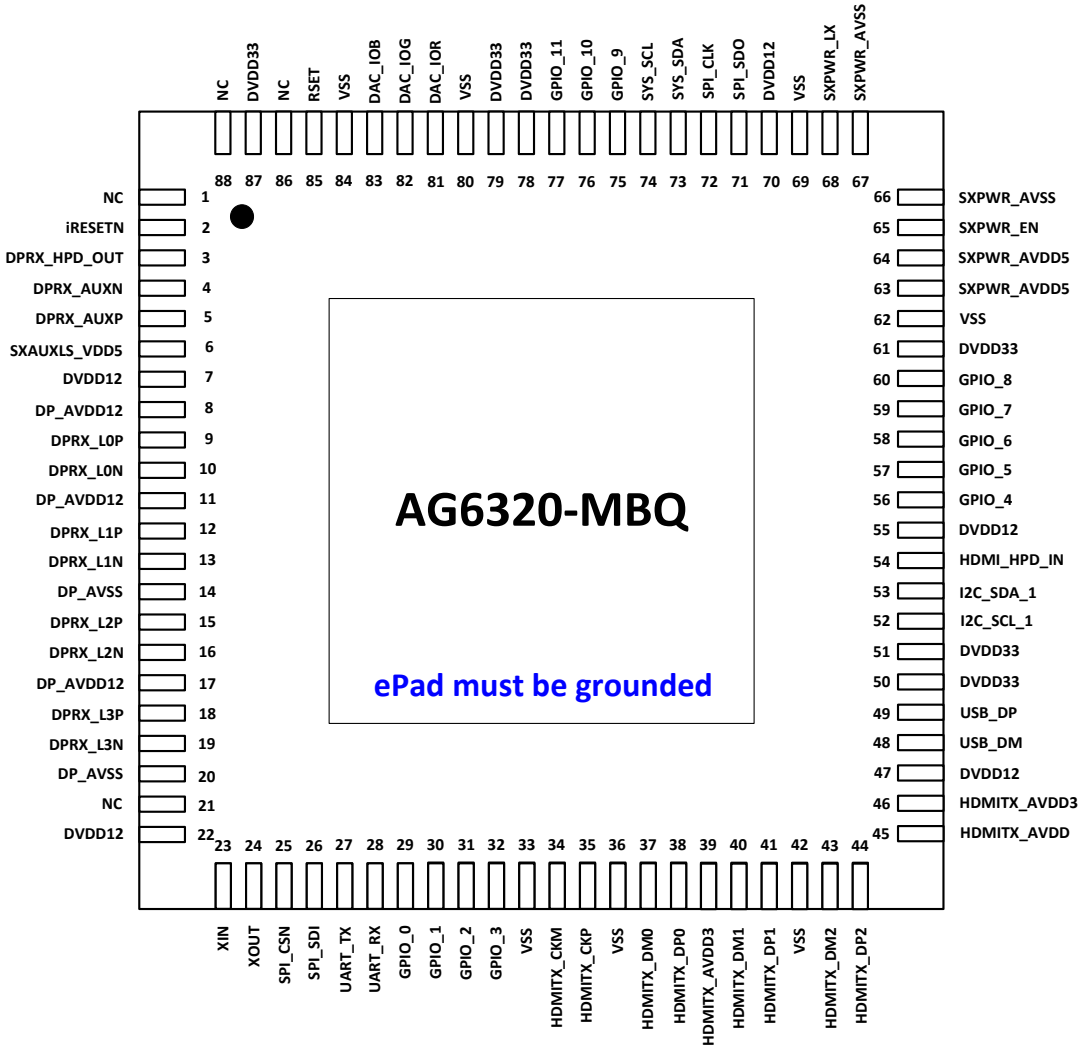
Pin Name	PIN NO.	Type	Description
POWER SUPPLY			
SXAUXLS_VDD5	6	Power	Analog 5V power input for AUX channel
DP_AVDD12	8, 11, 17	Power	Analog 1.2V power input for DP RX
DP_AVSS	14, 20	Power	Analog ground for DP RX

DVDD33	50, 51, 61 78, 79, 87	Power	Digital 3.3V I/O power input
DVDD12	7, 22, 47, 55, 70	Power	Digital 1.2V core power input
VSS	33, 36, 42, 62, 69, 80, 84	Power	Digital ground
HDMITX_AVDD	45	Power	Analog 1.2V power for HDMI TX
HDMITX_AVDD3	39, 46	Power	Analog 3.3V power for HDMI TX
SXPWR_AVDD5	63, 64	Power	5.0V power input. Input voltage range: 3.0V ~ 5.5V
SXPWR_AVSS	66, 67	Power	Analog ground.
SXPWR_LX	68	Power	NC
DIFFERENTIAL HIGH-SPEED IO			
DPRX_L0P	9	Input	DP RX lane0 positive
DPRX_L0N	10	Input	DP RX lane0 negative
DPRX_L1P	12	Input	DP RX lane1 positive
DPRX_L1N	13	Input	DP RX lane1 negative
DPRX_L2P	15	Input	DP RX lane2 positive
DPRX_L2N	16	Input	DP RX lane2 negative
DPRX_L3P	18	Input	DP RX lane3 positive
DPRX_L3N	19	Input	DP RX lane3 negative
HDMITX_CKM	34	Output	HDMI TX clock channel negative
HDMITX_CKP	35	Output	HDMI TX clock channel positive
HDMITX_DM0	37	Output	HDMI TX data channel 0 negative
HDMITX_DP0	38	Output	HDMI TX data channel 0 positive
HDMITX_DM1	40	Output	HDMI TX data channel 1 negative
HDMITX_DP1	41	Output	HDMI TX data channel 1 positive
HDMITX_DM2	43	Output	HDMI TX data channel 2 negative
HDMITX_DP2	44	Output	HDMI TX data channel 2 positive
DPRX_AUXN	4	Bidirectional	DisplayPort AUX channel N
DPRX_AUXP	5	Bidirectional	DisplayPort AUX channel P
Digital IO			
iRESETN	2	Input	H/W Reset signal, active low. Need connect

			to Resistor and Capacitor on board.
DPRX_HPD_OUT	3	Output	DP RX Hot Plug Detect
XIN	23	Input	Crystal oscillator clock input
XOUT	24	Output	Crystal oscillator clock output
SPI_CSN	25	Output	SPI chip select.
SPI_SDI	26	Input	SPI data input
UART_TX	27	Output	UART TX
UART_RX	28	Input	UART RX
I2S_WS	29	Output	I2S Left Right Clock
I2S_SD	30	Output	I2S Serial Audio Data Output
I2S_SCLK	31	Output	I2S Continuous Serial Clock
I2S_AUMCLK	32	Output	I2S System Clock
I2C_SCL_1	52	Bidirectional	HDMI I2C SCL
I2C_SDA_1	53	Bidirectional	HDMI I2C SDA
HDMI_HPD_IN	54	Input	HDMI cable detection
GPIO_2	56	Bidirectional	General Purpose I/O
GPIO_3	57	Bidirectional	General Purpose I/O
VGA_DETN	58	Input	VGA cable detection
I2C_SDA_0	59	Bidirectional	VGA I2C SDA
I2C_SCL_0	60	Bidirectional	VGA I2C SCL
SXPWR_EN	65	Input	Pull down to ground
SPI_SDO	71	Output	SPI data output.
SPI_CLK	72	Output	SPI clock.
HSYNC	73	Output	Horizontal sync signal to monitor
VSYNC	74	Output	Vertical sync signal to monitor
CEC	75	Input	HDMI CEC
GPIO_0	76	Bidirectional	General Purpose I/O
GPIO_1	77	Bidirectional	General Purpose I/O
Analog IO			
DAC_IOR	81	Output	VGA red channel output Pull down to ground by an 75Ω resistor
DAC_IOG	82	Output	VGA green channel output Pull down to ground by an 75Ω resistor
DAC_IOB	83	Output	VGA blue channel output Pull down to ground by an 75Ω resistor

RSET	85	Input	VGA full-scale current control resistor Pull down to ground by an 4.7KΩ resistor

Table 1 AG6320-MAQ PIN Description



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HDMITX_DM2	43	Output	HDMI TX data channel 2 negative
HDMITX_DP2	44	Output	HDMI TX data channel 2 positive
USB_DM	48	Bidirectional	USB Type-C D-
USB_DP	49	Bidirectional	USB Type-C D+
DPRX_AUXN	4	Bidirectional	DisplayPort AUX channel N
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iRESETN	2	Input	H/W Reset signal, active low. Need connect to Resistor and Capacitor on board.

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RSET	85	Input	VGA full-scale current control resistor

			Pull down to ground by an 4.7KΩ resistor

Table 2 AG6320-MBQ PIN Description

VII. Specification

i. Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDD5	5V Power Input	-0.5	5.5	V
VDD33/AVDD33	3.3V supply voltage	-0.5	3.63	V
VDD/AVDD	1.2V supply voltage	-0.5	1.32	V

Table 3 Absolute Maximum Rating

ii. DC Characteristics/Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
VDD5	5V Power Input	4.5	5	5.5	V
VDD33	Digital I/O supply voltage	3	3.3	3.6	V
VDD	Digital core supply voltage	1.16	1.2		V
AVDD3	Analog I/O supply voltage	3	3.3	3.6	V
AVDD	Analog core supply voltage	1.16	1.2		V
$I_{VDD33+AVDD3}$	3.3V I/O Supply Current (4K2K/30Hz)		80		mA
$I_{VDD+AVDD}$	1.2V Core supply Current (4K2K/30Hz)		380		mA
V_{OH}	Output High Voltage	2.4			V
V_{OL}	Output Low Voltage			0.4	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{LI}	Input leakage Cur.			±1	uA
θ_{JC}	Thermal Resistance(Junction to Case)		0.8		°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)		19		°C/W

T_J	Junction Temperature	0		125	°C
T_A	Ambient Temperature	0		70	°C

Table 4 Digital I/O Specification

iii. AC Characteristics

DisplayPort Main Link AC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
UI_HBR2	Unit interval for HBR2(5.4-Gbps/lane)		185		ps
UI_HBR	Unit interval for HBR(2.7-Gbps/lane)		370		ps
UI_RBR	Unit interval for RBR(1.62-Gbps/lane)		617		ps
Down_Spread_Amp.	Link clock down-spreading	0		0.5	%
Down_Spread_Frequency	Link clock down-spreading frequency	30		33	kHz
$T_{RX\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Max time between the jitter median and max. deviation from the median at Rx package pins for HBR (2.7-Gbps)			0.265	UI
$T_{RX\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Max. time between the jitter median and max. deviation from the median at Rx package pins for RBR (1.62-Gbps)			0.39	UI
$V_{RX\text{-}DC\text{-}CM}$	RX DC Common Mode Voltage	0		2	V
$I_{RX\text{-}SHORT}$	RX Short Circuit Current Limit			50	mA

Table 5 DisplayPort Input Timing

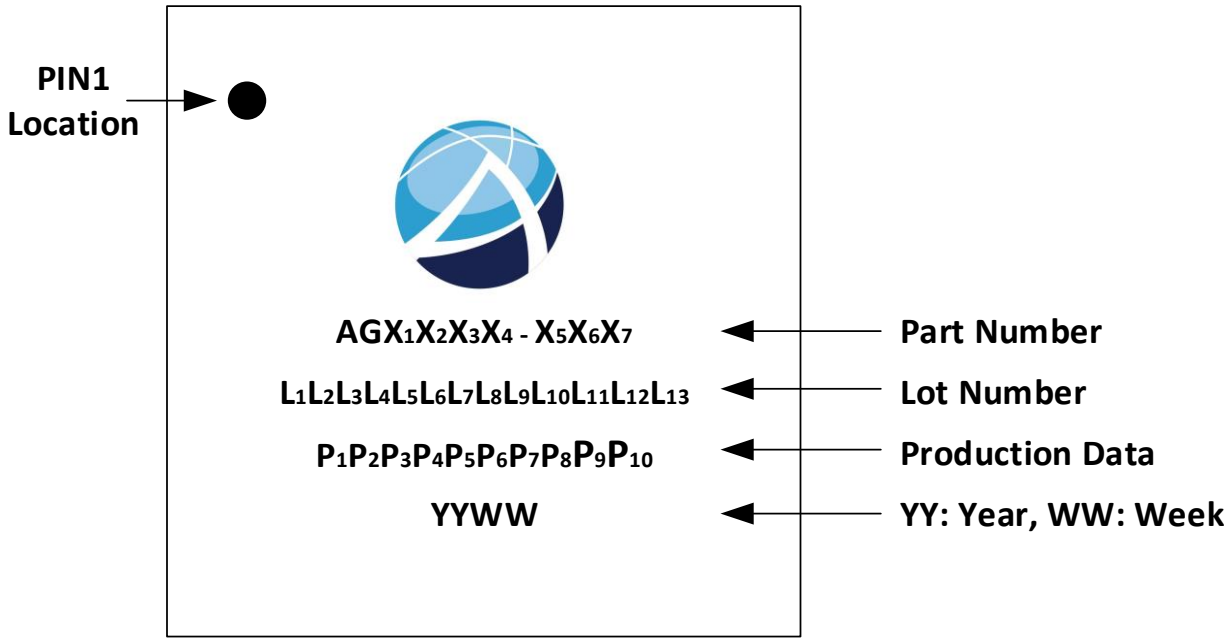
DisplayPort AUX-CH AC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
UIMAN	AUX (Manchester transaction) unit interval	0.4	0.5	0.6	us
Pre-charge Pulses	Number of pre-charge pulses	10		16	
$T_{AUX-BUS-PEAK}$	AUX CH bus park time	10			ns
$T_{cycle-to-cycle\ jitter}$	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI
$V_{AUX-DIFFp-p\ RX}$	AUX peak-to-peak voltage at a transmitting device when receiving	0.29		1.38	V
$V_{AUX-DIFFp-p\ RX}$	AUX peak-to-peak voltage at a receiving device when receiving	0.27		1.36	V
$V_{AUX\_TERM\_R}$	AUX CH termination DC resistance		100		Ω
$V_{AUX\_DC\_CM}$	AUX DC common mode voltage	0		2.0	V
$V_{AUX\_TURN\_CM}$	AUX turn around common mode voltage			0.3	V
I_{AUX_SHORT}	AUX short circuit current			90	mA
C_{AUX}	AUX AC coupling	75		200	nF

Table 6 DisplayPort AUX Channel I/O Specification

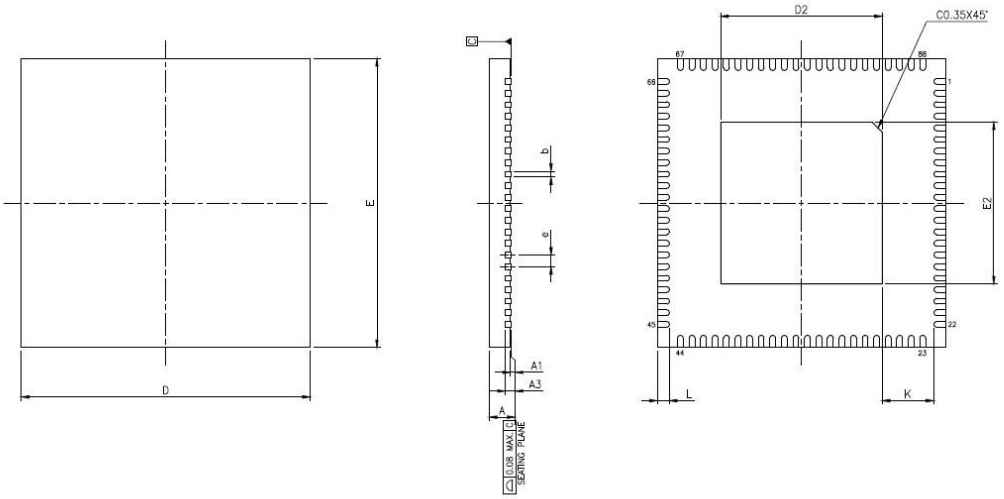
VIII. Packing and Marking Specification

- **Marking**



- **Package Dimension**

AG6320: QFN-88L 10x10mm



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(XA88)		
SYMBOLS	MIN.	NOM.	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	10.00 BSC		
E	10.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			b			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
276X27* MIL	6.75	6.80	6.85	6.75	6.80	6.85	0.15	0.20	0.25	V	X	(W)VNNE-1

Figure 5 AG6320 Package Dimension

IX. References

- DisplayPort™ Standard 1.2b Specification
- HDMI 1.4b Specification

X. Contact Information

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