



AG7111

3 to 1 HDMI/DVI/DisplayPort Dual-mode Switch

付S 18027661972 Q:1540182856

Data Sheet V1.0

Change History

Version	Date	Notes
1.0	2016/12/22	First Release

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Features

- Single voltage supply 3.15V ~ 5.5V
- Support both AC coupled and DC coupled inputs
- Support HDMI, DVI and DisplayPort input
- Compatible to HDMI 1.4b specification
- Compatible to DisplayPort Dual-Mode Standard version 1.1
- Maximum TMDS throughput up to 3.4Gbps per lane (Total 10.2 Gbps)
- Maximum pixel clock rate up to 340MHz
- Support 4K2K@30Hz resolution
- Support Deep Color
- RC embedded to leave out external crystal
- 5V to 3.3V/1.2V regulator embedded
- Integrated 50 ohm termination resistors at each high speed signal input
- Support 3 GPOs for port enable LED indicators
- Support GPI to select between Auto or MCU mode (Refer to AG7110 application note)
- Automatic HDMI plug-in detection
- Built-in port activate circuits for switching between source devices without the external MCU
- Support external MCU interface for remote controller application
- Suspend mode implemented for power saving

- Implement auto equalization design for supporting cables with different lengths
- Implement signal extension design to support long cables
- Advanced design to enhance noise immunity for cascade application

Process and Packaging

- 48-pin LQFP-EP/QFN 7X7mm package size
- Extended commercial temperature range (0°C to +70°C)

Applications

- Projectors
- A/V receivers
- Set-Top boxes
- Game consoles
- Televisions/Monitors
- Media Centers
- PCs/Notebooks

General Description

The Algotek AG7111 chip is a digital video interface (DVI) or high-definition multimedia interface (HDMI) or DisplayPort dual-mode switch which allows up to 3 DisplayPort or DVI or HDMI ports to be switched to a single display sink device. The maximum bandwidth is 3.4Gbps per lane and provides Deep Color supporting. Its low power operation allows no external power source required in most applications. AG7111 is available in a space-saving, 48-pin LQFP and QFN package and operates over the extended 0°C to +70°C temperature range.

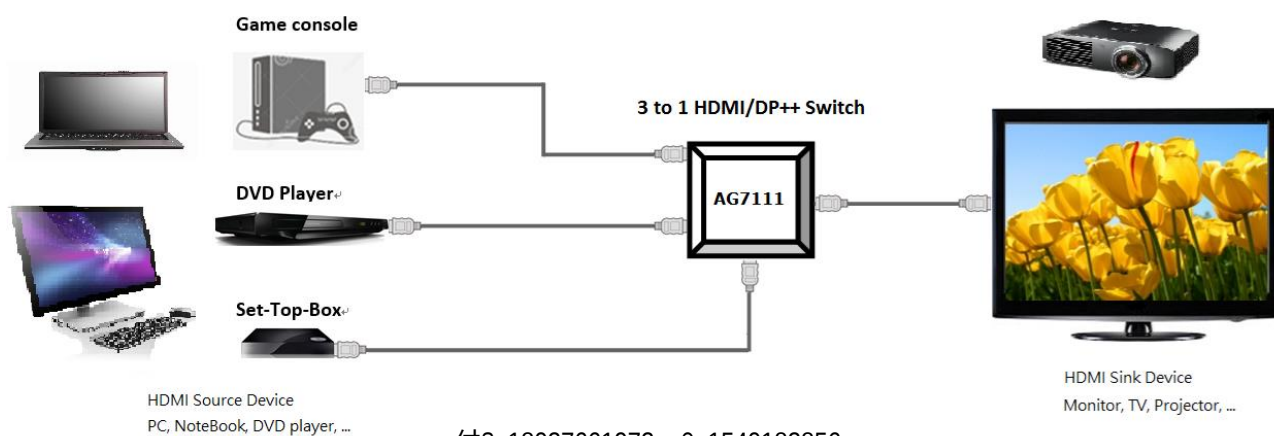


Figure 1 Application for 3 to 1 HDMI/DP++ Switch

1. System Block and Functional Description

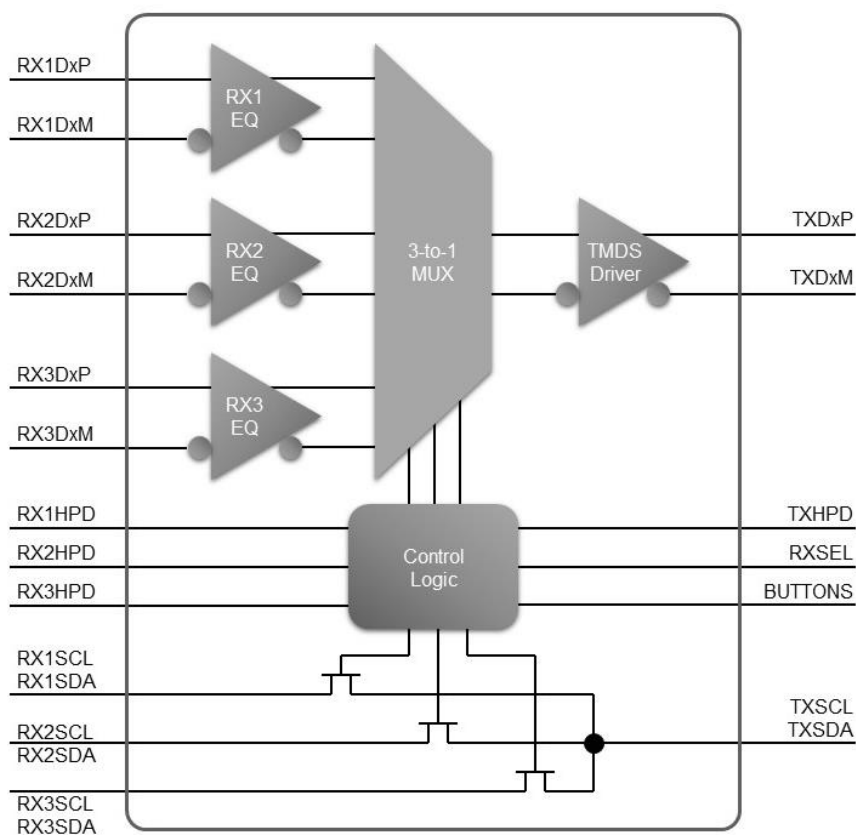


Figure 2 System Block Diagram

PIN Assignment

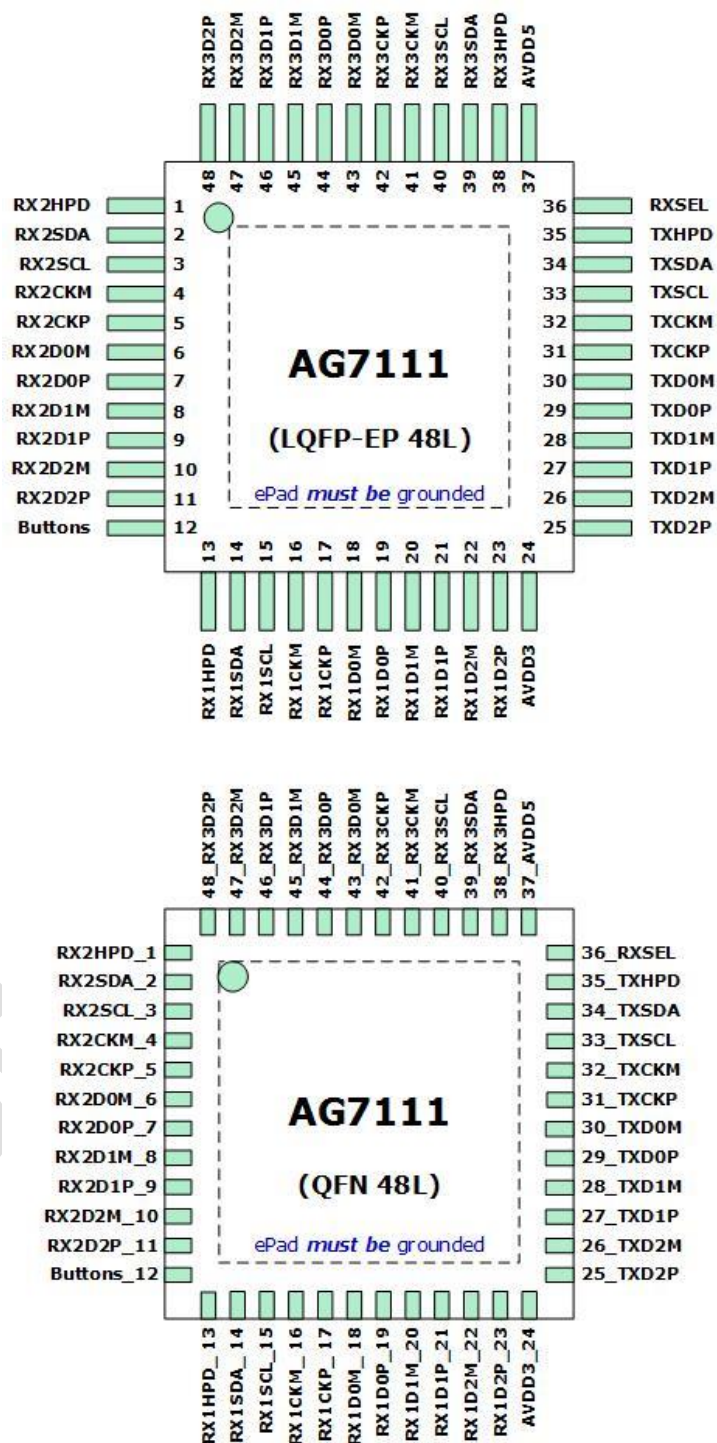


Figure 3 PIN Assignment

PIN Description

Pin#	Pin name	Type	Description
1	RX2HPD	Output	Port 2 Hot Plug detector output
2	RX2SDA	Bidirectional	Port 2 DDC Data
3	RX2SCL	Bidirectional	Port 2 DDC Clock
4	RX2CKM	Input	Port2 Clock TMDS negative input
5	RX2CKP	Input	Port2 Clock TMDS positive input
6	RX2D0M	Input	Port2 Data TMDS negative input
7	RX2D0P	Input	Port2 Data TMDS positive input
8	RX2D1M	Input	Port2 Data TMDS negative input
9	RX2D1P	Input	Port2 Data TMDS positive input
10	RX2D2M	Input	Port2 Data TMDS negative input
11	RX2D2P	Input	Port2 Data TMDS positive input
12	BUTTONS	Input	1) RX EQ select 2) Port switch without the external MCU
13	RX1HPD	Output	Port 1 Hot Plug detector output
14	RX1SDA	Bidirectional	Port 1 DDC Data
15	RX1SCL	Bidirectional	Port 1 DDC Clock
16	RX1CKM	Input	Port1 Clock TMDS negative input
17	RX1CKP	Input	Port1 Clock TMDS positive input
18	RX1D0M	Input	Port1 Data TMDS negative input
19	RX1D0P	Input	Port1 Data TMDS positive input
20	RX1D1M	Input	Port1 Data TMDS negative input
21	RX1D1P	Input	Port1 Data TMDS positive input
22	RX1D2M	Input	Port1 Data TMDS negative input
23	RX1D2P	Input	Port1 Data TMDS positive input
24	AVDD3	Power	VDD 3V
25	TXD2P	Output	Data TMDS positive output
26	TXD2M	Output	Data TMDS negative output
27	TXD1P	Output	Data TMDS positive output
28	TXD1M	Output	Data TMDS negative output
29	TXD0P	Output	Data TMDS positive output
30	TXD0M	Output	Data TMDS negative output

Pin#	Pin name	Type	Description
31	TXCKP	Output	Clock TMDS positive output
32	TXCKM	Output	Clock TMDS negative output
33	TXSCL	Bidirectional	Output Port DDC Clock
34	TXSDA	Bidirectional	Output Port DDC Data
35	TXHPD	Input	Output Port Hot Plug detector
36	RXSEL	Input	RX Input Port select by the external MCU
37	AVDD5	Power	VDD 5V
38	RX3HPD	Output	Port 3 Hot Plug detector output
39	RX3SDA	Bidirectional	Port 3 DDC Data
40	RX3SCL	Bidirectional	Port 3 DDC Clock
41	RX3CKM	Input	Port3 Clock TMDS negative input
42	RX3CKP	Input	Port3 Clock TMDS positive input
43	RX3D0M	Input	Port3 Data TMDS negative input
44	RX3D0P	Input	Port3 Data TMDS positive input
45	RX3D1M	Input	Port3 Data TMDS negative input
46	RX3D1P	Input	Port3 Data TMDS positive input
47	RX3D2M	Input	Port3 Data TMDS negative input
48	RX3D2P	Input	Port3 Data TMDS positive input
	ePad	Ground	Ground

Table 1 Describes the IP related IO ports

2. Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
AVDD5	5V Power Input	-0.3	6	V
ESD	HBM (JESD22-A114-B)	±8KV		
	MM (JESD22-A115-C)	±400V		
	CDM (JESD22-C101-C)	±500V		
Latch-up	LU (JESD78)	±200mA		

Table 2 Absolute Maximum Rating

Normal Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
AVDD5	5V Power Input	3.15	5	5.5	V
Ta	Ambient Temperature	0	25	70	°C
Icc*	Normal Operation Supply Current		85		mA

Test Condition:

 $V_{IH}=V_{DD}$, $V_{IL}=V_{DD}-0.4V$, $V_{ICM}=3.1V$, $R_T=50\Omega$, $V_{DD}=3.3V$

Data input: 1.485Gbps HDMI data pattern

Clock input: 148.5MHz clock

Table 3 Normal Operating Conditions

I/O Specification

Parameter		Test Conditions	Min	Typ.	Max	Unit
Status pin: TXHPD(input), RXHPD(output)						
V_{IH}	LVTTL input High-level voltage		2		5.3	V
V_{IL}	LVTTL input Low-level voltage		0		0.8	V
V_{OH}	LVTTL High-level output voltage	$I_{OH} = -8\text{ mA}$	2.4		5.3	V
V_{OL}	LVTTL Low-level output voltage	$I_{OL} = 8\text{ mA}$	0		0.4	V
Differential: RXCK/D0~D2,TXCK/D0~D2						
V_L	TMDS –VL	$\leq 165\text{MHz}$	2.7		2.9	V
V_L	TMDS –VL	$> 165\text{MHz}$	2.6		2.9	V
V_{off}	TMDS –VOFF		AVCC-10mV		AVCC+10mV	V
R_T	Input termination resistance		45	50	55	Ω

Table 4 I/O Specification

3. Packing and Marking Specification

Marking

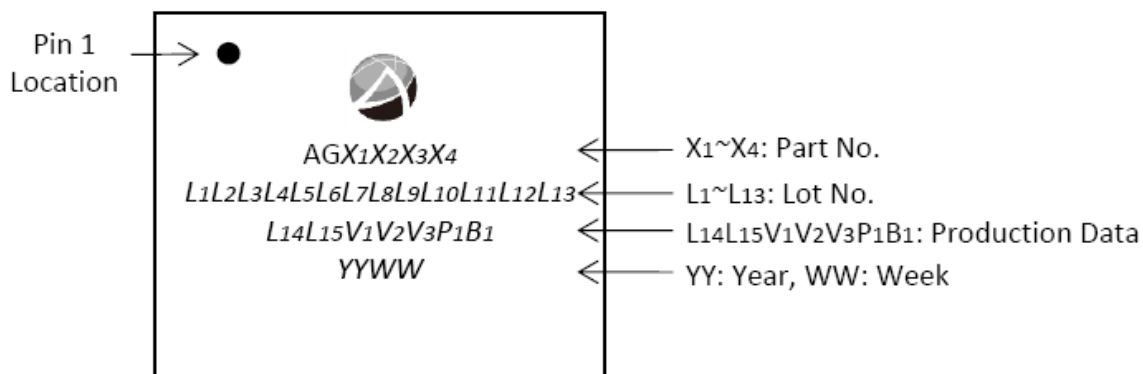
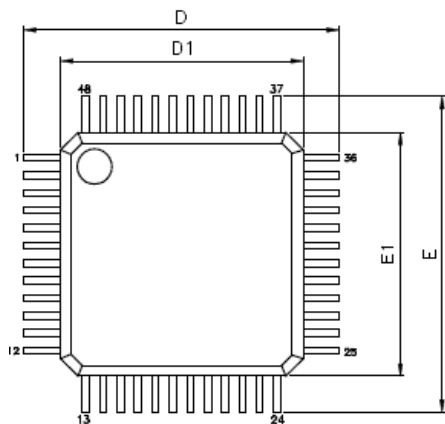


Figure 4 Marking

Package Drawing

LQFP-EP 48L

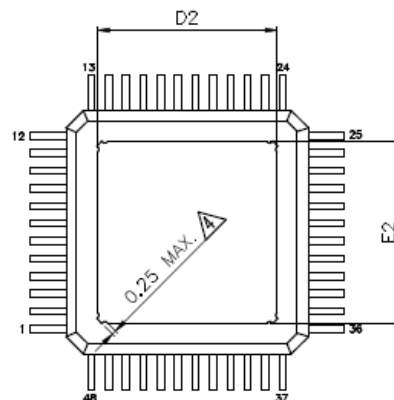
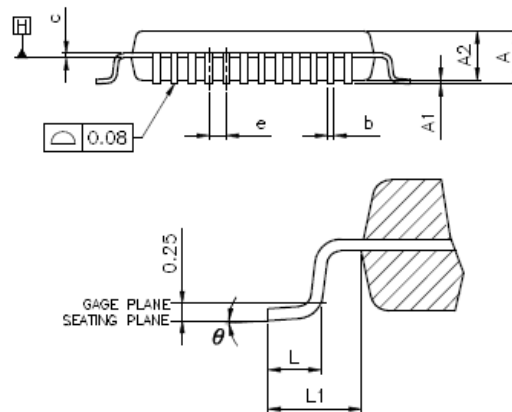


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
205X20E	4.31	5.21	4.31	5.21



THERMALLY ENHANCED VARIATIONS ONLY

NOTES:

1.JEDEC OUTLINE :

MS-026 BBC

MS-026 BBC-HD(THERMALLY ENHANCED VARIATIONS ONLY)

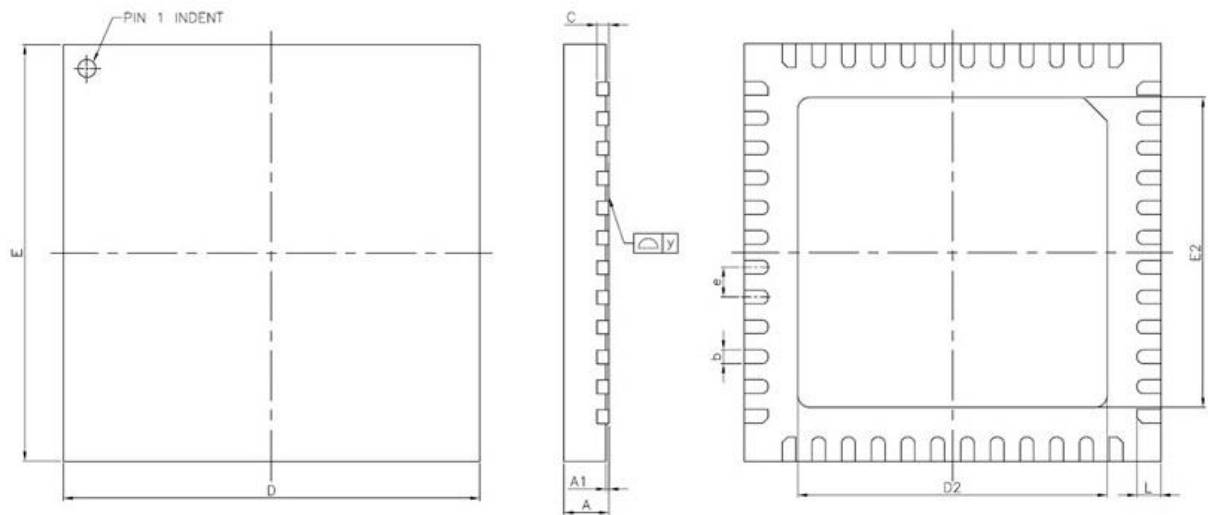
2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

Figure 5 LQFP-EP 48L Package Drawing

QFN 48L



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
C	—	0.20 REF.	—
D	6.925	7.00	7.075
D2	5.15	5.20	5.25
E	6.925	7.00	7.075
E2	5.15	5.20	5.25
e	—	0.50	—
L	0.30	0.40	0.50
y	0.00	—	0.075

NOTE:
1. THE TERMINAL #1 IDENTIFIER
IS A LASER MARKED FEATURE

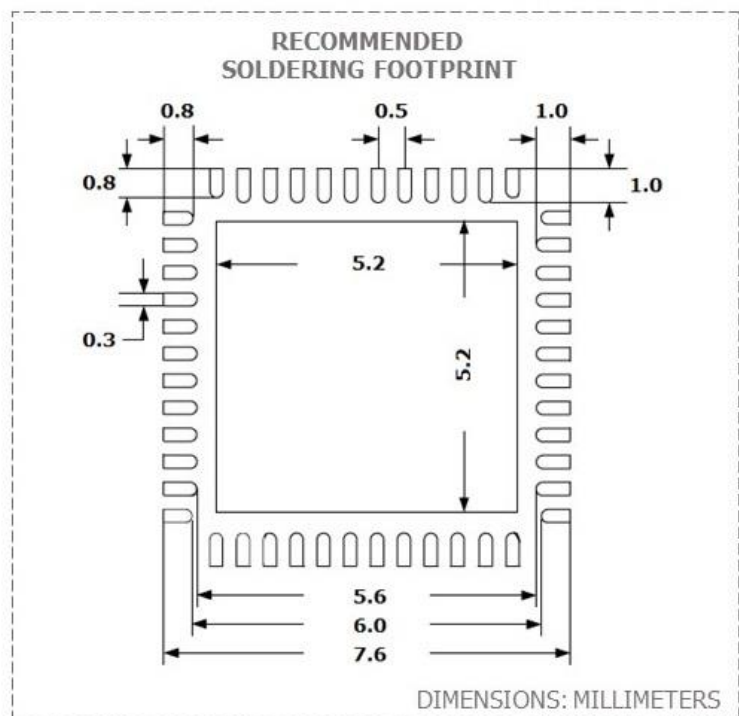


Figure 6 QFN 48L Package Drawing

4. References

HDMI 1.4b Specification

VESA DisplayPort Dual-Model Standard Version 1.1

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