



AG7120

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HDMI/DVI Re-Driver

Data Sheet V1.2

Change History

Version	Date	Notes
1.0	2016/5	First Release
1.1	2016/6/27	1) Update Figure 3 PIN Assignment 2) Add Electrical Characteristics
1.2	2017/2/10	1) Update Features 2) Update 2. Electrical Characteristics

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Features

- Single voltage supply 3.15V~ 5.5V
- Support both AC coupled and DC coupled inputs
- Support HDMI and DVI input
- Compatible to HDMI 1.4b specification
- Maximum TMDS throughput up to 3.4Gbps per lane (Total 10.2Gbps)
- Maximum pixel clock rate up to 340MHz
- Support 4K2K@30Hz resolution
- Support Deep Color
- RC embedded to leave out external crystal
- 5V to 3.3V/1.2V regulator embedded
- Integrated 50 ohm termination resistors at high speed signal input
- Implement auto equalization design for supporting cables with different lengths

- Implement signal extension design to support long cables

Process and Packaging

- 24-pin QFN 4X4mm package size
- Extended commercial temperature range (0 °C to +70°C)

Applications

- Long Cable
- HDMI/DVI Cable Extender
- HDMI/DVI Active Cable Assemblies
- Projectors
- High-Definition Displays

General Description

The Algotek AG7120 chip is a digital video interface (DVI) or high-definition multimedia interface (HDMI) re-driver which automatically compensates HDMI/DVI cable loss. The maximum bandwidth is 3.4Gbps per lane and provides Deep Color supporting. Its low power operation allows no external power source required. AG7120 is available in a space-saving, 24-pin QFN package and operates over the extended 0°C to +70°C temperature range.

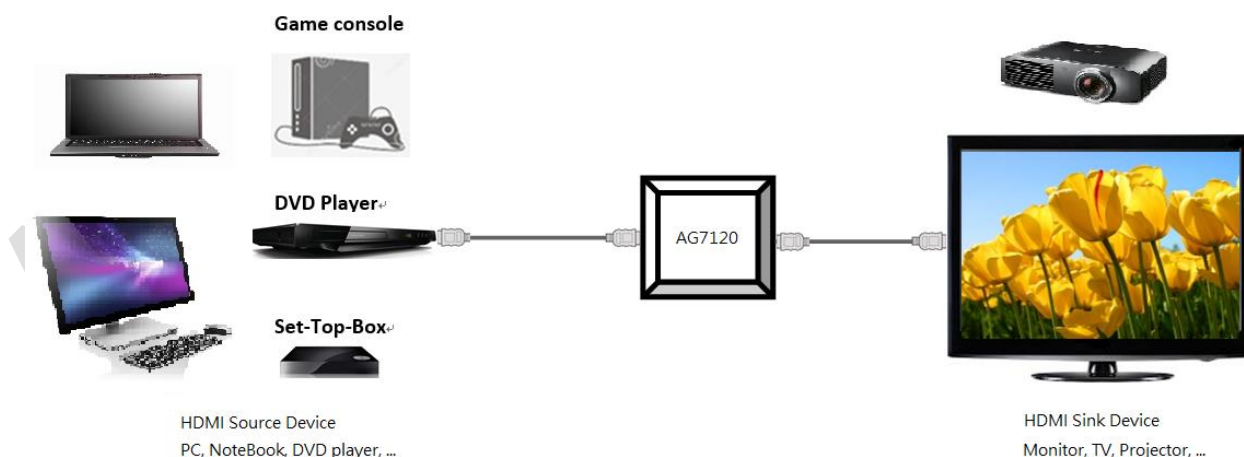


Figure 1 Application for HDMI/DVI re-driver

1. System Block and Functional Description

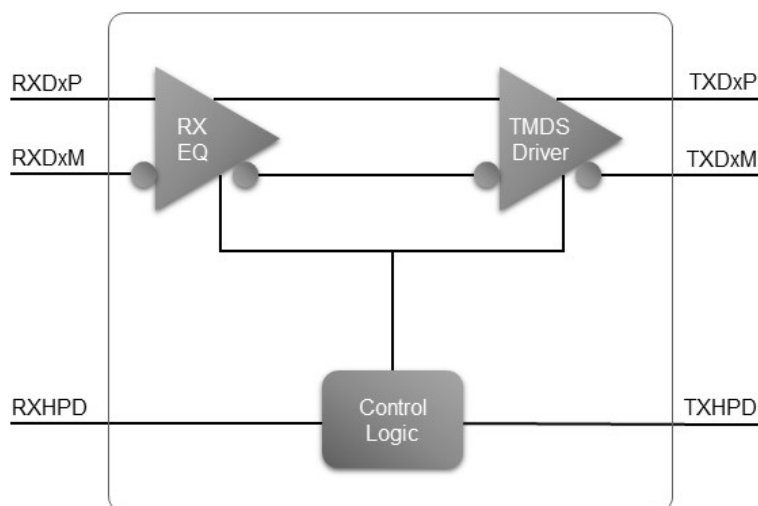


Figure 2 System Block Diagram

PIN Assignment

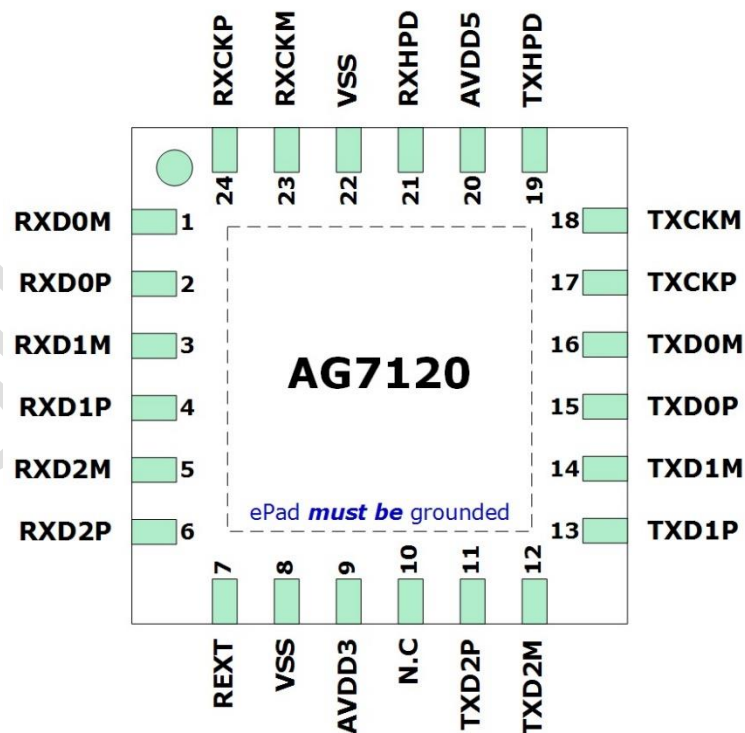


Figure 3 PIN Assignment

PIN Description

Pin	Pin name	Type	Description
1	RXD0M	Input	Data TMDS negative input
2	RXD0P	Input	Data TMDS positive input
3	RXD1M	Input	Data TMDS negative input
4	RXD1P	Input	Data TMDS positive input
5	RXD2M	Input	Data TMDS negative input
6	RXD2P	Input	Data TMDS positive input
7	REXT	Input	External Resistor
8	AVSS	Ground	Ground
9	AVDD3	Power	VDD 3V
10	N.C	N.C	No Connect
11	TXD2P	Output	Data TMDS positive output
12	TXD2M	Output	Data TMDS negative output
13	TXD1P	Output	Data TMDS positive output
14	TXD1M	Output	Data TMDS negative output
15	TXD0P	Output	Data TMDS positive output
16	TXD0M	Output	Data TMDS negative output
17	TXCKP	Output	Clock TMDS positive output
18	TXCKM	Output	Clock TMDS negative output
19	TXHPD	Input	Output Port Hot Plug detector
20	AVDD5	Power	VDD 5V
21	RXHPD	Output	Input Port Hot Plug detector
22	AVSS	Ground	Ground
23	RXCKM	Input	Clock TMDS negative input
24	RXCKP	Input	Clock TMDS positive input
	ePad	Ground	Ground

Table 1 describes the IP related IO ports.

2. Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
AVDD5	5V Power Input	-0.3	6	V
ESD	HBM (JESD22-A114-B)	±8KV		
	MM (JESD22-A115-C)	±400V		
	CDM (JESD22-C101-C)	±500V		
Latch-up	LU (JESD78)	±200mA		

Table 2 Absolute Maximum Rating

Normal Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
AVDD5	5V Power Input	3.15	5	5.5	V
Ta	Ambient Temperature	0	25	70	°C
I _{cc} *	Normal Operation Supply Current		80		mA

Test Condition:

V_{IH}=V_{DD}, V_{IL}=V_{DD}-0.4V, V_{ICM}=3.1V, R_T=50Ω, V_{DD}=3.3V

Data input: 1.485Gbps HDMI data pattern

Clock input: 148.5MHz clock

Table 3 Normal Operating Conditions

I/O Specification

Parameter		Test Conditions	Min	Typ.	Max	Unit
Status pin: TXHPD(input), RXHPD(output)						
V _{IH}	LVTTTL input High-level voltage		2		5.3	V
V _{IL}	LVTTTL input Low-level voltage		0		0.8	V
V _{OH}	LVTTTL High-level output voltage	I _{OH} = -8 mA	2.4		5.3	V
V _{OL}	LVTTTL Low-level output voltage	I _{OL} = 8 mA	0		0.4	V

Table 4 I/O Specification

DC Electrical Characteristics

Parameter		Test Conditions	Min	Typ.	Max	Unit
TXCKP/N, TXD0P/N, TXD1P/N, TXD2P/N						
V _{OFF}	Single-ended off output voltage	AVCC = 3.3V	AVCC - 0.01		AVCC + 0.01	V
V _{SWING}	Single-ended output swing voltage	AVCC= 3.3V, R _T = 50 Ω	0.4		0.6	V
V _{OL}	Single-ended low level output voltage	AVCC= 3.3V, TMDS clock frequency > 165MHz,	AVCC - 0.7		AVCC - 0.4	V
RXCKP/N, RXD0P/N, RXD1P/N, RXD2P/N						
V _{TERM}	TMDS Termination Voltage	AVCC= 3.3V	3.125		3.475	V
V _{ICM}	Input Common Mode Voltage Level	AVCC= 3.3V	AVCC - 0.4		AVCC - 0.0375	V
RT						
R _T	Input Termination Resistance		45	50	55	Ω

Table 5 DC Electrical Characteristics

AC Electrical Characteristics

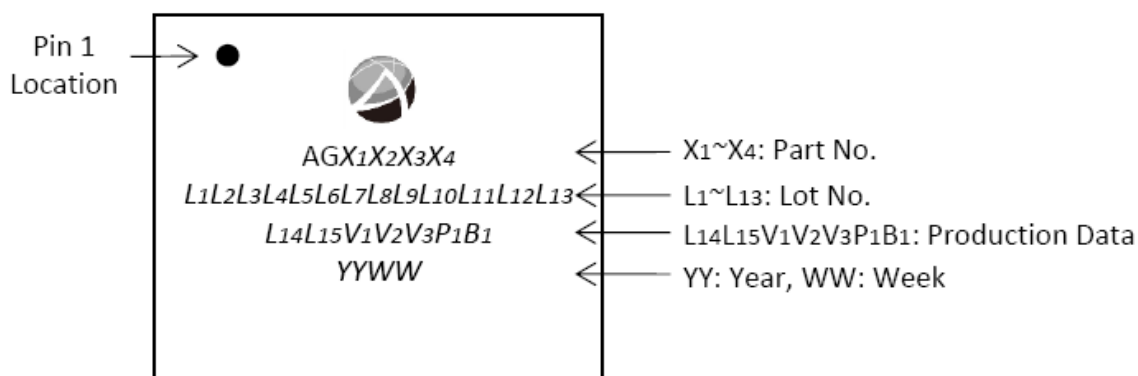
Parameter	Test Conditions	Min	Typ.	Max	Unit
TXCK, TXD0, TXD1, TXD2, RXCK, RXD0, RXD1, RXD2					
FCLK	Pixel Clock (1/10th of the differential data rate)	-	-	340	MHz
DR	Maximum Data Rate per Channel	-	-	3.4	Gbps
TXCKP/N, TXD0P/N, TXD1P/N, TXD2P/N					
V _{OD}	Differential output voltage (peak-to-peak).	AVCC= 3.3V, R _T = 50 Ω	0.8	1.2	V
t _R	Differential clock and data output rise and fall time	20% ~ 80% of VOD	75		ps
t _F		80% ~ 20% of VOD	75		ps
t _{SK-intra}	Intra-pair output skew			0.15Tbit	ps
t _{SK-inter}	Inter-pair differential skew			0.2Tcharacter	ps
t _{TXCK-duty}	TMDS clock duty cycle	40	50	60	%
t _{TXCK-jitter}	TMDS differential output clock jitter	TMDS clock frequency > 165MHz,		0.25Tbit	ps

Parameter	Test Conditions	Min	Typ.	Max	Unit
RXCKP/N, RXD0P/N, RXD1P/N, RXD2P/N					
VID	Differential input voltage (p-p)	VICM=3.3V	0.15	1.56	V
t _{SK-intra-i}	Intra-pair input skew	TMDS clock frequency > 165MHz,		112ps +0.15Tbit	ps

Table 6 AC Electrical Characteristics

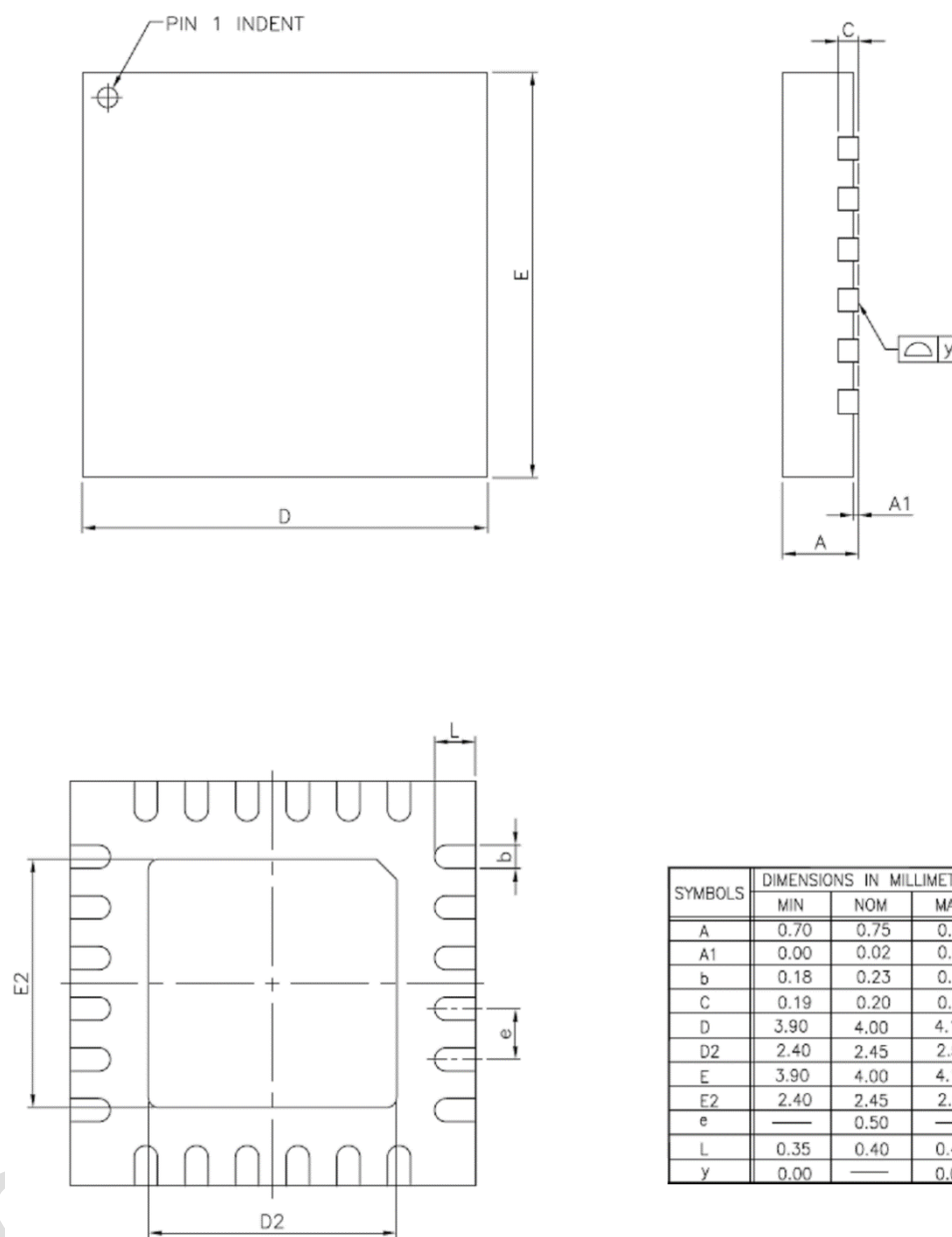
3. Packing and Marking Specification

Marking





Package Dimension



4. References

HDMI 1.4b Specification