



AG7220

HDMI2.0 Re-Driver Controller

www.angerei.com TEL:18520874087 QQ:1659747718

Data Sheet

Official Version

V1.0

October, 2017



Revision History

Version	Date	Notes
1.0	2017/10/24	Official release.

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I. General Description

ALGOLTEK AG7220 is a single chip solution to serve as High-Definition Multimedia Interface (HDMI) re-driver which maintaining high band data on thinner or longer HDMI cable with HDMI2.0 devices. The maximum bandwidth is 6Gbps per lane which can support video performance up to 4K2K@60Hz resolution. With **ALGOLTEK**'s advanced green designs, AG7220 can support features without external power supplies. Compare to the traditional passive cable, with AG7220, HDMI cable makers can provide the thinner or longer HDMI2.0 cables with the equal video performance.

II. Features

- Compatible to HDMI 2.0 specification
- Support HDMI and DVI inputs
- Support both AC coupled and DC coupled inputs
- Maximum TMDS throughput up to 6Gbps per lane (Total 18Gbps)
- Support 4K2K@60Hz resolution
- Support RGB 4:4:4 / YCbCr 4:4:4 / YCbCr 4:2:2 / YCbCr 4:2:0
- Support Deep Color
- Wide-range receiver equalization ratio: 7.5dB ~ 20dB @ 6Gbps
- Programmable receiver equalization for supporting cables with different lengths
- Pin selectable output swing and pre-emphasis control
- Built-in 3.3V LDO and 1.2V LDO
- Integrated 50ohm termination resistors
- Single voltage supply: 3.8V ~ 5.5V
- ESD protection: HBM 8KV, MM 300V

III. Device Information

Part Number	Package	Body Size
AG7220	32QFN	4x4 mm ²

IV. Application

- Sink devices with HDMI2.0 interface
- HDMI / DVI Cable Extender
- HDMI / DVI active Cable

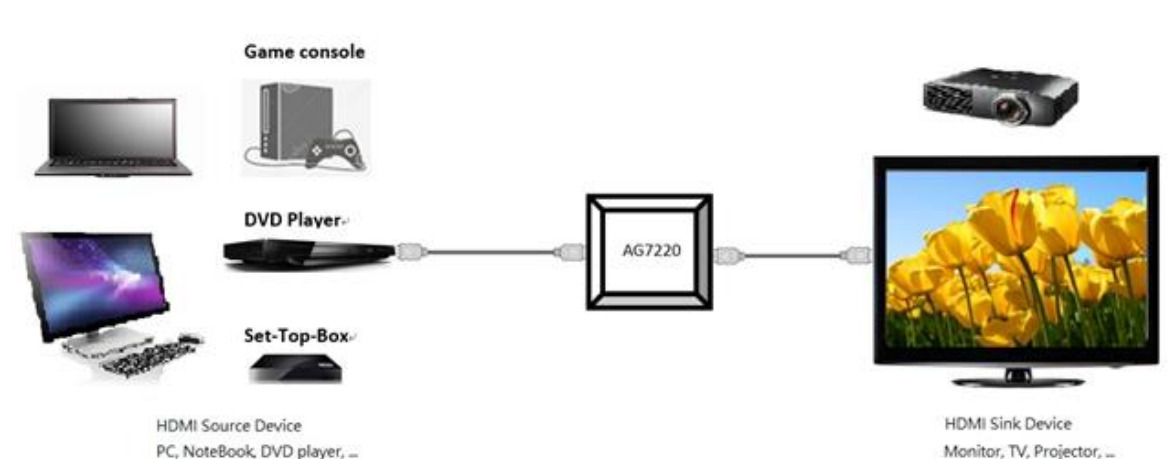
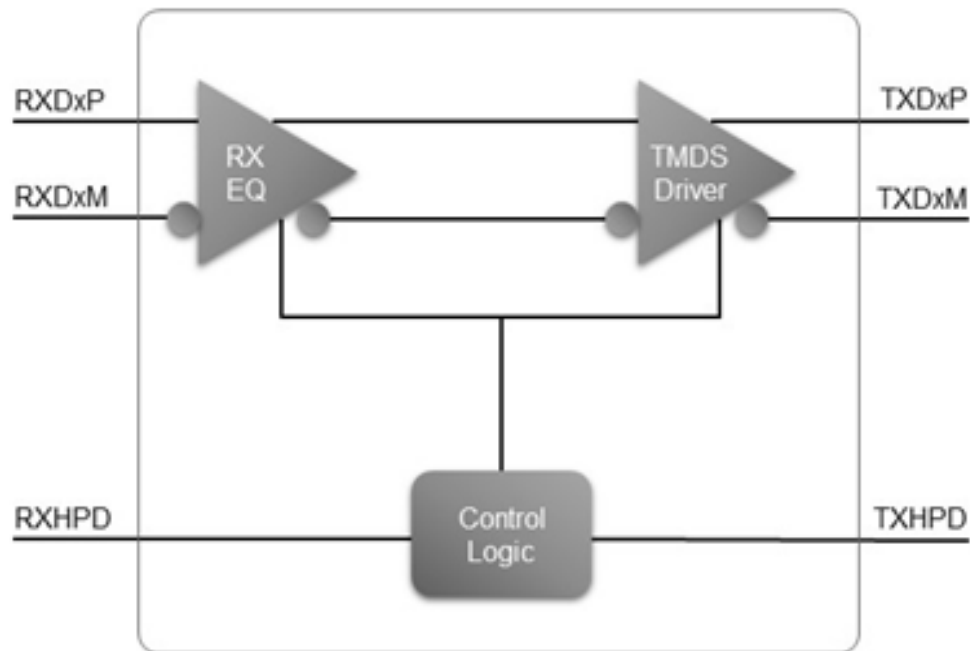


Figure 1 Applications for HDMI Re-driver

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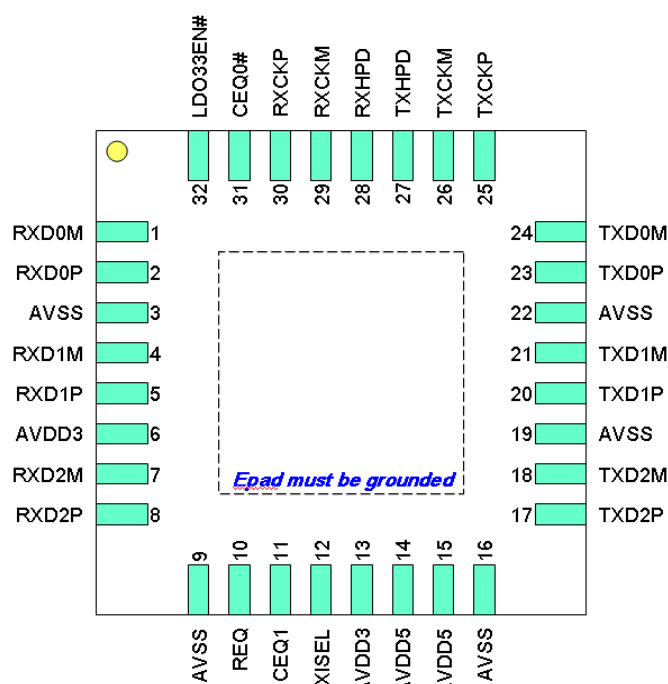
V. System Block Diagram



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Figure 2 System Block Diagram

VI. Pin Definition and Function



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Figure 3 PIN Definition

Table 1 Pin Description

Pin name	Pin	Type	Description
POWER SUPPLY			
AVDD5	14, 15	Power	VDD 5V Input
AVDD3	6, 13	Power	VDD 3.3V (generated from internal 3.3V LDO)
AVSS	3, 9, 16, 19 22, <i>Epad</i>	Ground	Ground
DIFFERENTIAL HIGH-SPEED IO			
RXCKM / P	29, 30	Input	TMDS clock input from player
RXD0M / P	1, 2	Input	TMDS data input from player
RXD1M / P	4, 5	Input	TMDS data input from player
RXD2M / P	7, 8	Input	TMDS data input from player
TXD2P / M	17, 18	Output	TMDS data output to monitor

TXD1P / M	20, 21	Output	TMDS data output to monitor
TXD0P / M	23, 24	Output	TMDS data output to monitor
TXCKP / M	25, 26	Output	TMDS clock output to monitor
HOT PLUG DETECTOR PINS			
TXHPD	27	Input	Hot Plug Detection input from monitor
RXHPD	28	Output	Hot Plug Detection output to player
CONTROL PINS			
LDO33EN#	32	Input	Selection to enable/disable internal 3.3V LDO LOW : enable internal 3.3V LDO (Default) HIGH (AVDD3): disable internal 3.3V LDO Internal pull LOW
CEQ0#	31	Input	Reserved for vendor usage Internal pull LOW
CEQ1	11	Input	RX equalization ratio selection (Check Pin10 REQ) Internal pull HIGH (AVDD5)
REQ	10	Input	RX equalization ratio @ 6Gbps CEQ1 = LOW : REQ = floating: 7.5dB REQ = 75Kohm (+- 5%) to ground: 10dB REQ = 10Kohm (+- 5%) to ground: 12.5dB REQ = 27Kohm (+- 5%) to ground: 15dB CEQ1 = HIGH (Default): REQ = 10Kohm (+- 5%) to ground: 17.5dB REQ = 27Kohm (+- 5%) to ground: 20dB Internal pull HIGH (AVDD5)
TXISEL	12	Input	TX output current selection LOW : TX output differential swing = 950mV without pre-emphasis HIGH : TX output differential swing = 1200mV with 2dB pre-emphasis (Default) Internal pull HIGH (AVDD3) ◆ <i>Larger output swing is recommended if there is an extra cable between AG7220 and Sink device.</i>



VII. Specification

i. Absolute Maximum Ratings

		MIN	MAX	Unit
Supply Voltage Range	AVDD5	-0.5	6	V
Storage Temperature		-60	150	°C

ii. ESD Ratings

		Value	Unit
Electrostatic Discharge	Human-body mode (HBM)	8000	V
	Machine mode (MM)	300	V
	Charged-device mode (CDM)		V

iii. Recommended Operation Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
AVDD5	5V Power Input	3.8		5.5	V
Ta	Ambient Temperature	-40		85	°C
Icc*	Normal Operation Supply Current		110		mA

***Test Condition:**

VIH = 3.3V, VIL = 2.9V, VICM = 3.1V

Data input: 1.485Gbps HDMI data pattern

Clock input: 148.5MHz clock

**iv. Electrical Characteristics**

Parameter	Test Conditions	Min	Typ.	Max	Unit
TXCKP/M, TXD0P/M, TXD1P/M, TXD2P/M					
V_{OFF}	Single-ended off output voltage	AVCC = 3.3V	AVCC - 0.01	AVCC + 0.01	V
V_{SWING}	Single-ended output swing voltage	AVCC = 3.3V, $R_T = 50\ \Omega$	0.4	0.6	V
V_{OD}	Differential output voltage	AVCC = 3.3V, $R_T = 50\ \Omega$	0.8	1.2	V
$t_{TXCK-duty}$	TMDS clock duty cycle		40	60	%
$t_{TXCK-jitter}$	TMDS differential output clock jitter			0.25	T_{bit}

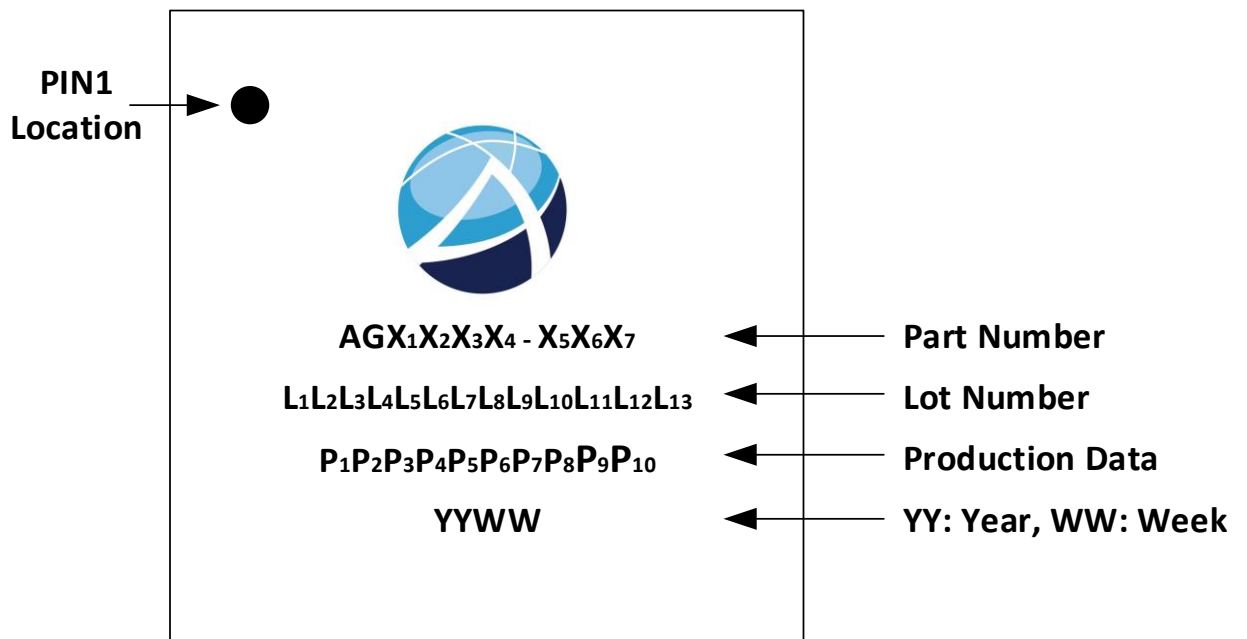
Parameter	Test Conditions	Min	Typ.	Max	Unit
RXCKP/M, RXD0P/M, RXD1P/M, RXD2P/M					
V_{TERM}	TMDS termination voltage	AVCC = 3.3V	3.125	3.475	V
V_{ICM}	Input common mode voltage level	AVCC = 3.3V	AVCC - 0.8	AVCC + 0.01	V
V_{ID}	Differential input voltage (peak-to-peak)	$V_{ICM} = 3.1V$	0.1	1.6	V
$R_{T, diff}$	Input differential termination resistance		90	110	Ω
$R_{T, cm}$	Input common mode termination resistance		30		Ω

Parameter	Test Conditions	Min	Typ.	Max	Unit
TXCK, TXD0, TXD1, TXD2, RXCK, RXD0, RXD1, RXD2					
D_R	Maximum data rate per channel			6	Gbps



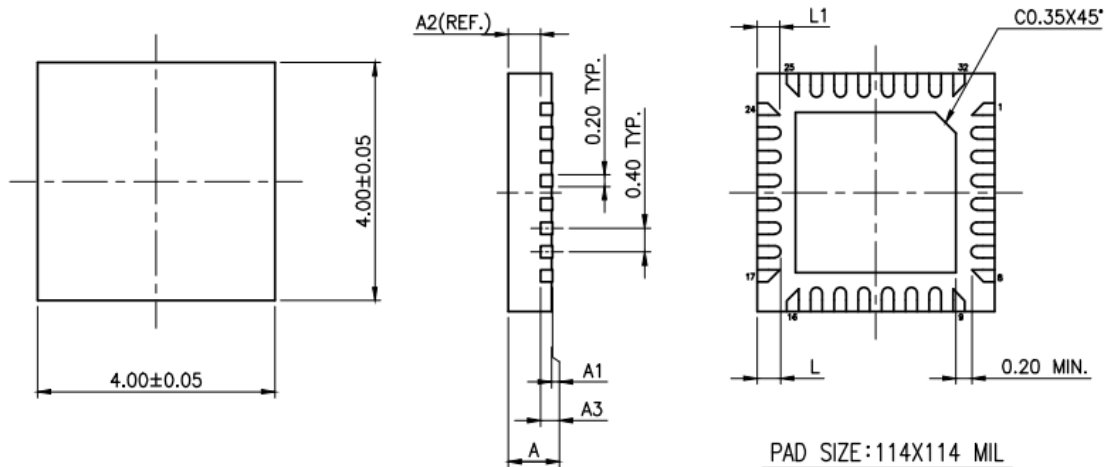
VIII. Package Outline

i. Marking





ii. Package Dimension



SYMBOLS	WQFN(X432)	VQFN(Y432)	UQFN(W432)
A1	0.02±0.02	0.02±0.02	0.02±0.02
A2	0.55	0.65	0.40
A3	0.203±0.008	0.203±0.008	0.150±0.007
A	0.75±0.035	0.85±0.035	0.55±0.025

PAD SIZE	L	L1	WQFN	VQFN	UQFN
114X11* MIL	0.40±0.05	0.382±0.05	V	V	—

NOTES:

1. CONTROLLED DIM. : mm
2. PLATING MATERIAL :
2-1 PURE TIN 300 ~ 800 MICRO INCH.
2-2 PPF(Ni/Pd/Au).
3. L/F MATERIAL : A194 FH.
4. CUTTING BURR : 0.030mm UNLESS OTHER SPECIFIC NOTE.
5. LEAD BEND : 3° MAX.
6. INTERLEAD FLASH : 0.075mm MAX.
7. MOLD FLASH : 0.120mm MAX.
8. OFF-CENTER(PACKAGE'S ϕ AND L/F'S ϕ) : 0.025mm MAX.
9. WARPING FACTOR : 2 mil/INCH MAX.
10. LEAD COPLANARITY : 0.05mm MAX. CPK > 1.33.
11. ALL SURFACE : MATTE FINISH Ra 0.8 ~ 1.2 μ m.
12. MOLDING COMPOUND : EME-G700 OR EQUIVALENCE.

IX. Contact Information



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