ALGOLTEK

安格科技股份有限公司

www.angerei.com QQ1659747718 TEL 18520874087

Datasheet

of

AG9321-MBQ

(USB-C to HDMI/VGA with PD 3.0)

Revision 0.9.2

2020/5/9

Confidential

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  - On-chip 1 MΩ resistors for AUX
  - Up to 4096x2160/30Hz resolution
  - Down spread spectrum clocking
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  - HDMI 1.4b compliance
  - Up to 4096x2160p/30Hz resolution
  - Linear PCM with sample rate of 32 kHz, 44.1 kHz and 48 kHz
- HDCP 1.4 compliance with pre-loaded key
- Dual Quick Charge™ 3.0 ports.
- On-chip USB 2.0 FS PHY for Billboard and firmware upgrade
- Embedded 16-bit CISC with 16 KB SRAM
- Integrated 128 KB flash
- Communication interfaces
  - One UART interface
  - Two I^2C interfaces, one in master/slave mode and one in master mode.
- 4-ch, 10-bit ADC for voltage monitoring
- Deep color
  - RGB/YUV (4:4:4) – 10 bits per color
  - YUV (4:2:2) – 10 bits per color
  - Color space conversion – YUV to RGB and RGB to YUV
- Operating characteristic
  - 1.2V core power and 3.3V I/O power
  - Temperature range: 0°C to 70°C
  - ESD HBM 1 kV
- Package
  - QFN-64L 8x8x0.75 mm^3

Application

- Docking station
- Laptop accessory

Series	Part Number
AG9320	AG9321-MBQ

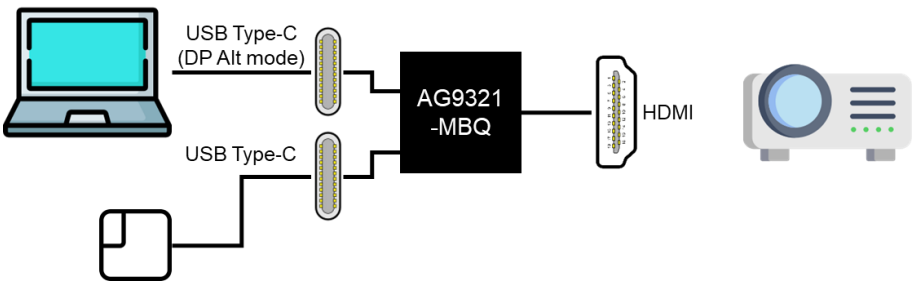


Figure 1. Application illustration

II. GENERAL DESCRIPTION

ALGOLTEK AG9321-MBQ provides a single-chip solution of USB Type-C (DisplayPort Alternate) to HDMI converter with Power Delivery. AG9321-MBQ supports dual USB Type-C receptacles with on-chip R_p/R_d resistors and is compliant with USB Power Delivery Specification 3.0. AG9321-MBQ also supports Quick Charge™ 3.0 for battery charging.

The DisplayPort receiver is compliant with DisplayPort 1.2 specification and supports up to 4096x2160/30Hz resolution with configurable 1, 2 or 4 lanes configuration at 5.4(HBR2), 2,7(HBR), and 1.62(RBR) Gbps per lane. The HDMI transmitter is compliant with HDMI 1.4 and supports up to 4096x2160/30Hz resolution. Copy protection is provided by encryption with HDCP 1.4 and factory pre-loaded HDCP key.

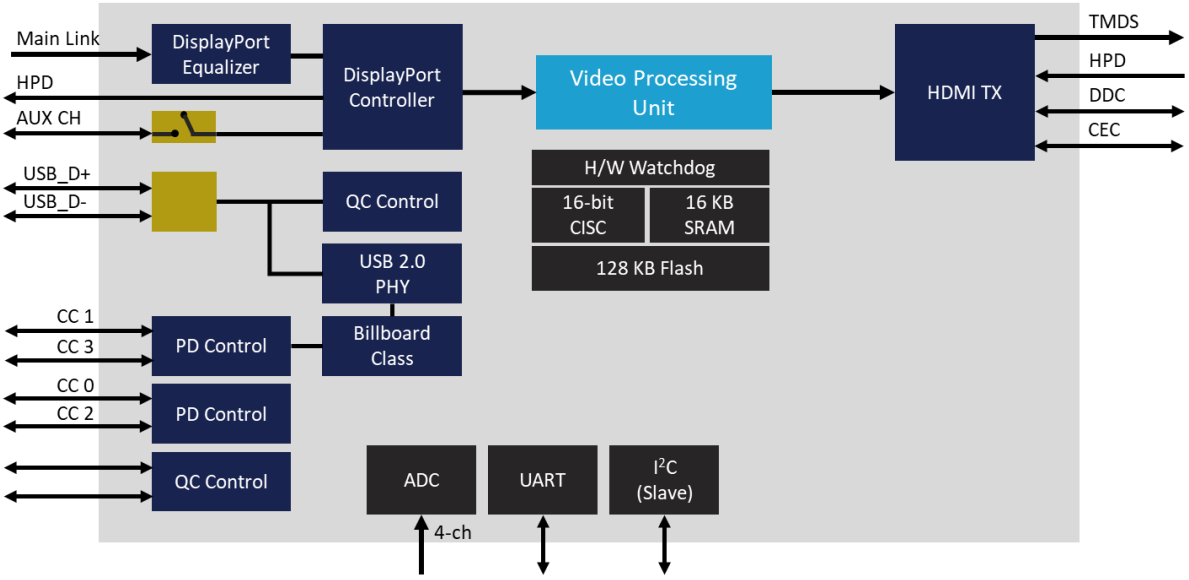


Figure 2. System block diagram

III. FUNCTIONAL DESCRIPTION

A. USB Type-C interface

AG9321-MBQ supports 4 Configuration Channels (CC) and integrates complete R_p and R_d resistors of CC for two USB Type-C receptacles. USB Type-C interfaces are compliant with USB Power Delivery Specification Revision 3.0.

1. DisplayPort Alternate mode

One of the USB Type-C interface uses USB Power Delivery Structured Vendor Defined Messages (Structured VDMs) to enable DisplayPort Alternate Mode and supports USB Billboard function if required.

When USB Type-C receptacle behaves as a DisplayPort Sink, pin assignment C, D and E are detected for the USB Type-C connector pins A2-A3, A8, A10-A11 and B2-B3, B8, B10-B11.

Table 1. Type-C receptacle pin assignment – normal plug orientation

Pin Assignment		C	D	E
Receptacle Pin Number	A2-A3	Main Link 3	USB TX	Main Link 1
	A10-A11	Main Link 1	Main Link 1	Main Link 3
	B2-B3	Main Link 0	Main Link 0	Main Link 2
	B10-B11	Main Link 2	USB RX	Main Link 0
	A8	AUX CH N	AUX CH N	AUX CH P
	B8	AUX CH P	AUX CH P	AUX CH N

Table 2. Type-C receptacle pin assignment – flipped plug orientation

Pin Assignment		C	D	E
Receptacle Pin Number	A2-A3	Main Link 0	Main Link 0	Main Link 2
	A10-A11	Main Link 2	USB RX	Main Link 0
	B2-B3	Main Link 3	USB TX	Main Link 1
	B11-B10	Main Link 1	Main Link 1	Main Link 3
	A8	AUX CH P	AUX CH P	AUX CH N
	B8	AUX CH N	AUX CH N	AUX CH P

The video data rate changes depending on the configuration.

2. Power Delivery

AG93210MBQ supports Dual Role Power. The USB PD power mode can be configured for the following four modes: from power sink to power source, from power source to power sink, power sink only and power source only.

B. DisplayPort receiver

The DisplayPort receiver is compliant with DisplayPort Specification Revision 1.2 and consists of a Main link, an auxiliary channel (AUX CH), and a Hot-Plug Detect (HPD) signal.

- Main Link—Main Link is a unidirectional, high-bandwidth channel that transports video and audio over 1, 2, or 4 lanes at 5.4(HBR2), 2,7(HBR), and 1.62(RBR) Gbps per lane. The clock is embedded in 8b/10b encoded serial data.

Table 3. DisplayPort Main Link throughput

	Raw Bit Rate	Throughput
1 lane	1.62, 2.7, 5.4 Gbps	1.296, 2.16, 4.32 Gbps
2 lanes	3.24, 5.4, 10.8 Gbps	2.592, 4.32, 8.64 Gbps
4 lanes	6.48, 10.8, 21.6 Gbps	5.184, 8.64, 17.28 Gbps

- AUX CH—The AUX CH is 1 Mbps half-duplex bidirectional channel used for link management and device control. AUX CH is used to transports EDID as well.
- HPD—The HPD signal serves as an interrupt request to detect its presence.

The DisplayPort receiver supports VESA or CEA resolution up to 4096x2160/30Hz, color depth up to 30 bits and down Spread Spectrum Clocking (SSC). Copy protection is provided by decryption with HDCP 1.3 and DPCP.

For supporting USB Type-C (DisplayPort Alternate mode) pin assignment C, D and E, the DisplayPort receiver provides data lane swap capability.

C. High Definition Multimedia Interface (HDMI) transmitter

The HDMI transmitter is compliant with HDMI 1.4b Specification and consists of three color channels accompanied by a single clock channel. Based on TMDS encoding, the HDMI protocol allows each color channel to transfer individual RGB colors, audio data and auxiliary data between source and sink devices. TMDS encoding is based on 8b/10b algorithm. The maximum clock rate is 297 MHz and the maximum total throughput is 7.128 Gbps (2.376 Gbps/channel).

The HDMI transmitter supports VESA or CEA resolution up to 4096x2160/30Hz, color depth up to 30 bits and

IEC 60985 L-PCM with sample rate of 32 kHz, 44.1 kHz and 48 kHz. Copy protection is provided by encryption with HDCP 1.4 and factory pre-loaded key.

D. USB 2.0 Full Speed PHY

AG9321 provides on-chip USB 2.0 Full Speed PHY for supporting Billboard function and firmware upgrade via USB.

E. Universal Asynchronous Receiver Transmitters (UART)

The UART interface provides asynchronous communication and full-duplex communication mode. System firmware can be upgraded through this UART interface.

F. Inter-Integrated Circuit (I^2C) interface

The Inter-Integrated Circuit (I^2C) interface is 2-wire, bidirectional serial bus which supports the standard (up to 100 kHz) and fast (up to 400 kHz) modes.

AG9321-MBQ provides up to three I^2C bus interfaces. One I^2C bus operates in slave mode for receiving system configuration and two I^2C buses operate in master mode for Display Data Channel, DDC, of HDMI connector and of VGA (D-sub) connector. System firmware can be upgraded through I^2C master (DDC of HDMI) or I^2C slave interface.

G. Analog-to-Digital Converter (ADC)

One 10-bit analog-to-digital converter is embedded and shares up to 5 external channels, performing conversions in scan mode, which automatic conversion is performed on a selected group of analog inputs. An interrupt is generated when the converted voltage is outside the programmed thresholds.

H. Video processing unit

The video processing unit performs three functionalities: color space conversion, gamma control and dithering. Color space conversion performs YUV to RGB or RGB to YUV color space transformation, gamma control performs the gamma compensation and dithering performs the noise reduction.

The video processing supports bypass mode to disable these functionalities. The data output of DisplayPort receiver will pass through the video processing unit directly.

I. QuickCharge™ controller

Two Quick charge controllers are embedded for supporting Qualcomm® QuickCharge™ QC3.0 protocol. When QC 3.0 is activated, the voltage can be set via this protocol from 3.6 V to 12 V in steps of 200 mV.

AG9321 integrates two QC 3.0 controllers. One is supported on USB_D+/D-, and the other is supported on GPIO9 and GPIO10.

IV. PINOUTS AND PIN DESCRIPTION

A. Pin Diagram

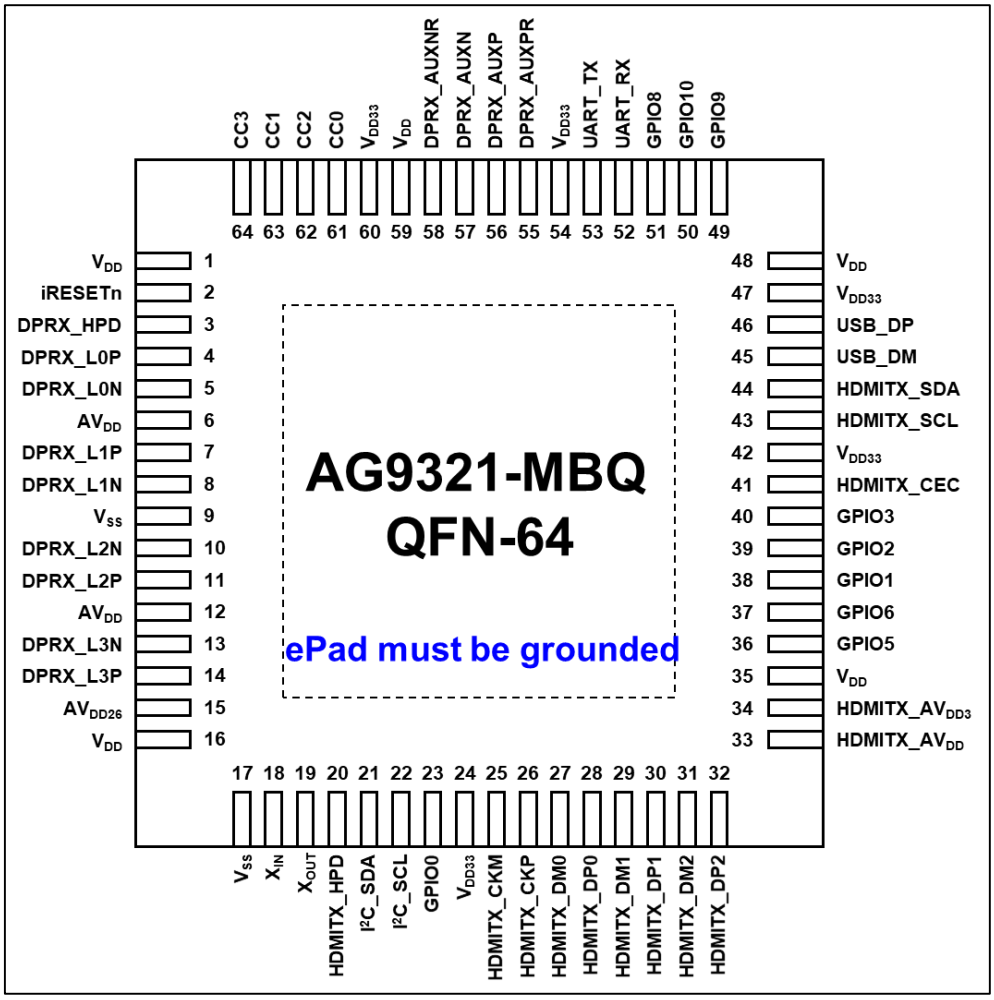


Figure 3. QFN-64 Pinout

B. Pin Description

Table 4. Pin description

QFN64	Pin Name	Type	Description
1	V_{DD}	P	1.2V power supply for core
2	iRESETn	I	System reset, active low. External resistor and capacitor are required.
3	DPRX_HPD	O	DisplayPort RX Hot-Plug Detect (HPD)
4	DPRX_L0P	I	DisplayPort RX Lane 0+
5	DPRX_L0N	I	DisplayPort RX Lane 0-
6	AV_{DD}	P	1.2V analog power supply for DisplayPort RX
7	DPRX_L1P	I	DisplayPort RX Lane 1+
8	DPRX_L1N	I	DisplayPort RX Lane 1-
9	V_{SS}	P	Ground pin for system
10	DPRX_L2N	I	DisplayPort RX Lane 2-
11	DPRX_L2P	I	DisplayPort RX Lane 2+
12	AV_{DD}	P	1.2V analog power supply for DisplayPort RX
13	DPRX_L3N	I	DisplayPort RX Lane 3-
14	DPRX_L3P	I	DisplayPort RX Lane 3+
15	AV_{DD26}	P	2.6V analog power output for decoupling capacitor
16	V_{DD}	P	1.2V power supply for core
17	V_{SS}	P	Ground pin for system
18	X_{IN}	I	Crystal oscillator clock input
19	X_{OUT}	O	Crystal oscillator clock output
20	GPIO4	I/O	General Purpose I/O
	HDMITX_HPD	I	HDMI TX Hot-Plug Detect (HPD)
21	I^2C_SDA	I/O	I^2C (master) serial data
22	I^2C_SCL	I/O	I^2C (master) serial clock
23	GPIO0	I/O	General Purpose I/O
24	V_{DD33}	P	3.3V power supply for I/O ports
25	HDMITX_CKM	O	HDMI TX negative clock output
26	HDMITX_CKP	O	HDMI TX positive clock output
27	HDMITX_DM0	O	HDMI TX channel 0 negative data output
28	HDMITX_DP0	O	HDMI TX channel 0 positive data output
29	HDMITX_DM1	O	HDMI TX channel 1 negative data output
30	HDMITX_DP1	O	HDMI TX channel 1 positive data output
31	HDMITX_DM2	O	HDMI TX channel 2 negative data output
32	HDMITX_DP2	O	HDMI TX channel 2 positive data output
33	HDMITX_AV_{DD}	P	1.2V analog power supply for HDMI TX

QFN64	Pin Name	Type	Description
34	HDMITX_AV$_{DD3}$	P	3.3V analog power supply for HDMI TX
35	V$_{DD}$	P	1.2V power supply for core
36	GPIO5	I/O	General Purpose I/O
37	GPIO6	I/O	General Purpose I/O
	I²C_SCL	I/O	I²C (slave) serial clock
38	GPIO1	I/O	General Purpose I/O
	ADC_CH3	I	ADC channel 3
39	GPIO2	I/O	General Purpose I/O
	ADC_CH2	I	ADC channel 2
	I²C_SCL	I/O	I²C (slave) serial clock
40	GPIO3	I/O	General Purpose I/O
	ADC_CH1	I	ADC channel 1
	I²C_SDA	I/O	I²C (slave) serial data
41	HDMITX_CEC	I	HDMI TX CEC input
	ADC_CH0	I	ADC channel 0
42	V$_{DD33}$	P	3.3V power supply for I/O ports
43	HDMITX_SCL	I/O	I²C (master) serial clock for DDC of HDMI TX
	I²C_SCL	I/O	I²C (slave) serial clock
44	HDMITX_SDA	I/O	I²C (master) serial data for DDC of HDMI TX
	I²C_SDA	I/O	I²C (slave) serial data
45	USB_DM	I/O	USB differential signal D- (UFP), Quick Charge™ 3.0 enabled
46	USB_DP	I/O	USB differential signal D+ (UFP), Quick Charge™ 3.0 enabled
47	V$_{DD33}$	P	3.3V power supply for I/O ports
48	V$_{DD}$	P	1.2V power supply for core
49	GPIO9	I/O	General Purpose I/O
	QC1_DP	I/O	D+ terminal of Quick Charge™ 3.0
50	GPIO10	I/O	General Purpose I/O
	QC1_DM	I/O	D- terminal of Quick Charge™ 3.0
51	GPIO8	I/O	General Purpose I/O
52	UART_RX	I	UART data receiver
53	UART_TX	O	UART data transmitter
54	V$_{DD33}$	P	3.3V power supply for I/O ports
55	DPRX_AUXPR	I/O	AUX positive channel with 1 MΩ resistor
56	DPRX_AUXP	I/O	DisplayPort auxiliary channel +
57	DPRX_AUXN	I/O	DisplayPort auxiliary channel -
58	DPRX_AUXPR	I/O	AUX negative channel with 1 MΩ resistor

QFN64	Pin Name	Type	Description
59	V_{DD}	P	1.2V power supply for core
60	V_{DD33}	P	3.3V power supply for I/O ports
61	CC0	I/O	USB-C Configuration Channel, CC0
62	CC2	I/O	USB-C Configuration Channel, CC2
63	CC1	I/O	USB-C Configuration Channel, CC1
64	CC3	I/O	USB-C Configuration Channel, CC3

V. ELECTRICAL CHARACTERISTICS

A. Absolute Maximum Ratings

Table 5. Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD33}-V_{SS}	3.3V supply voltage for I/O	-0.5	3.63	V
V_{DD}-V_{SS}	1.2V supply voltage for system	-0.5	1.32	V
AV_{DD33}-V_{SS}	3.3V supply voltage for analog circuit	-0.5	3.63	V
AV_{DD}-V_{SS}	1.2V supply voltage for analog circuit	-0.5	1.32	V
HDMITX_AV_{DD3}-V_{SS}	3.3V supply voltage for HDMI TX	-0.5	3.63	V
HDMITX_AV_{DD}-V_{SS}	1.2V supply voltage for HDMI TX	-0.5	1.32	V
V_{IN}	Input voltage on any other pin	V_{SS}-0.5	V_{DD33}	V
$\|V_{DD}-AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	0	50	mV
$\|V_{DDX}-V_{DD}\|$	Variations between different power pins	0	50	mV
$\|V_{SSX}-V_{SS}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	0	50	mV

Table 6. Current characteristics

Symbol	Parameter	Max	Unit
ΣI_{VDD33}	Total current into sum of all 3.3V power lines		mA
ΣI_{VDD}	Total current into sum of all 1.2V power lines		mA
ΣI_{VSS}	Total current out of sum of all ground lines		mA

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

Table 7. Thermal characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Ambient temperature	0	70	°C
T_J	Junction temperature	0	85	°C
T_{ST}	Storage temperature	-65	150	°C

Table 8. Package thermal characteristics

Symbol	Parameter	Value	Unit
θ_{JC}	Thermal resistance junction-case, QFN-64	2.0	°C/W
θ_{JA}	Thermal resistance junction-ambient, QFN-64	29	°C/W

Table 9. ESD characteristics

Symbol	Ratings	Conditions	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C conforming to JESD22-A114-B	1C	1.0	kV

$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25°C conforming to JESD22-C101-C	III	500	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25°C conforming to JESD22-A115-C	B	250	V

Table 10. Electrical sensitivities

Symbol	Ratings	Conditions	Class	Max	Unit
LU	Static latch-up class	T_A = 25°C conforming to JESD78	I level A	200	mA

B. Operating Conditions

1. General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient temperature	0	25	70	°C
V_{DD33}	Supply voltage for I/O	3.0	3.3	3.6	V
V_{DD}	Supply voltage for system	1.16	1.23	1.32	V
AV_{DD33}	Supply voltage for analog circuit	3.0	3.3	3.6	V
AV_{DD}	Supply voltage for analog circuit	1.16	1.23	1.32	V
HDMITX_AV_{DD3}	Supply voltage for HDMI TX (3.3V)	3.0	3.3	3.6	V
HDMITX_AV_{DD}	Supply voltage for HDMI TX (1.2V)	1.16	1.2	1.32	V

2. I/O port characteristics

Table 12. I/O static characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	2.4		5.5	V
V_{OL}	Output Low Voltage	0		0.4	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{LI}	Input leakage current			±1	μA

C. DisplayPort Characteristics

Table 13. DisplayPort Main Link AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
UI_HBR2	Unit interval for HBR2 (5.4 Gbps/lane)		185		ps
UI_HBR	Unit interval for HBR (2.7 Gbps/lane)		370		ps

UI_RBR	Unit interval for RBR (1.62 Gbps/lane)		617		ps
Down_Spread_Amp.	Link clock down-spreading	0		0.5	%
Down_Spread_Frequency	Link clock down-spreading frequency	30		33	kHz
$T_{RX-MEDIAN-to-MAX-JITTER}$	Max time between the jitter median and max. deviation from the median at Rx package pins for HBR (2.7-Gbps)			0.265	UI
$T_{RX-MEDIAN-to-MAX-JITTER}$	Max. time between the jitter median and max. deviation from the median at Rx package pins for RBR (1.62-Gbps)			0.39	UI
$V_{RX-DC-CM}$	RX DC Common Mode Voltage	0		2	V
$I_{RX-SHORT}$	RX Short Circuit Current Limit			50	mA

Table 14. DisplayPort AUX-CH AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
UI_{MAN}	AUX (Manchester transaction) unit interval	0.4	0.5	0.6	μs
Pre-charge Pulses	Number of pre-charge pulses	10		16	-
$T_{AUX-BUS-PARK}$	AUX CH bus park time	10			ns
$T_{cycle-to-cycle\ jitter}$	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI
$V_{AUX-DIFFp-p}$	AUX peak-to-peak voltage at a receiving device	0.27		1.36	V
R_{AUX_TERM}	AUX CH termination DC resistance		100		Ω
$V_{AUX\_DC\_CM}$	AUX DC common mode voltage	0		2.0	V
$V_{AUX\_TURN\_CM}$	AUX turn around common mode voltage			0.3	V
I_{AUX_SHORT}	AUX short circuit current			90	mA
C_{AUX}	AUX AC coupling	75		200	nF

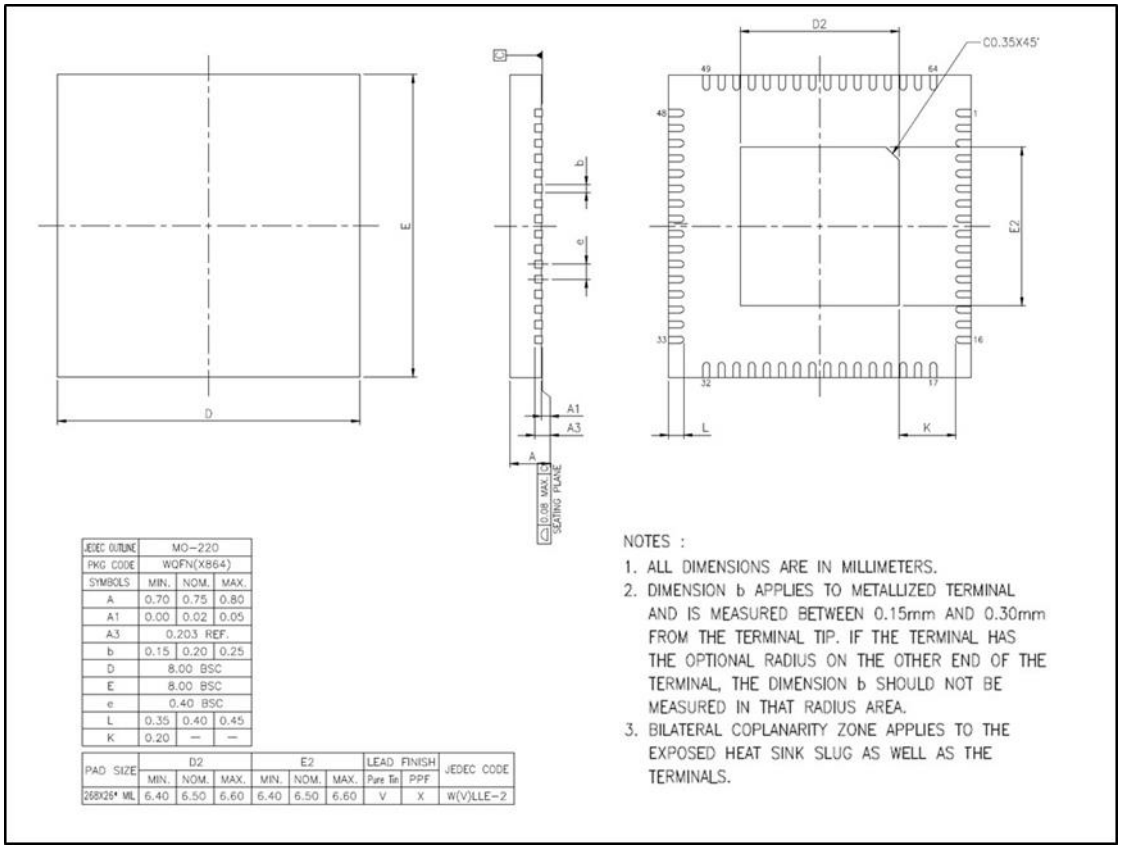
VI. TERMS AND ABBREVIATIONS

Table 15. Terms and Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
AUX	Auxiliary
CCIO	Configuration Channel Input/Output
CEA	Consumer Electronics Association
CISC	Complex Instruction Set Computing
CTA	Consumer Technology Association (Formerly CEA)
DDC	Display Data Channel
DPCP	DisplayPort Content Protection
DP	DisplayPort
EDID	Extended Display Identification Data
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I^2C	Inter-Integrated Circuit
I/O	Input/Output
LPCM	Linear Pulse Code Modulation
MCCS	Monitor Control Command Set
PHY	Port Physical Layer
PLL	Phase-Locked Loop
RAM	Random Access Memory
ROM	Read-Only Memory
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
THD+N	Total Harmonic Distortion +Noise
TMDS	Transition Minimized Differential Signaling
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VESA	Video Electronics Standards Association
VGA	Video Graphic Array

VII. PACKAGE INFORMATION

A. QFN-64L (8x8x0.75 mm^3, pitch 0.4 mm)



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X864)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
268X26* MIL	6.40	6.50	6.60	6.40	6.50	6.60	V	X	W(V)LLE-2

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 4. QFN-64 package outline

VIII. MARKING INFORMATION

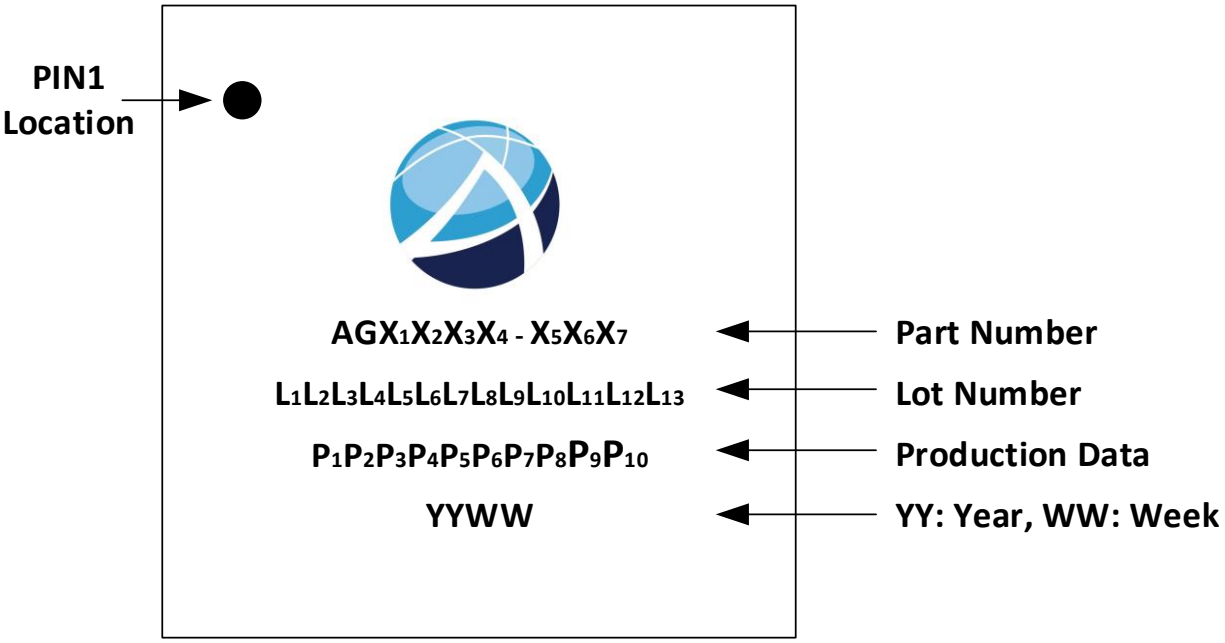


Figure 5. Marking information

IX. REVISION HISTORY

Table 16. Revision History

Date	Revision	Remark
2020/01/15	0.9	Preliminary