

**● General Description**

The AGM312M combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for load switch and battery protection applications.

**● Features**

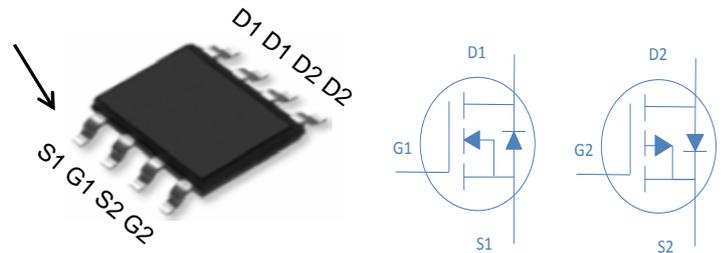
- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

**● Application**

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

**Product Summary**

BVDSS	RDSON	ID
30V	10mΩ	11A
-30V	28mΩ	-7.2A

**SOP-8 Pin Configuration**

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM312M	AGM312M	SOP-8	325mm	16mm	3000

**Table 1. Absolute Maximum Ratings (TA=25°C)**

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
$V_{DS}$	Drain-Source Voltage ( $V_{GS}=0V$ )	30	-30	V
$V_{GS}$	Gate-Source Voltage ( $V_{DS}=0V$ )	±20	±20	V
$I_D$	Drain Current-Continuous( $T_c=25^\circ C$ ) (Note 1)	11	-7.2	A
	Drain Current-Continuous( $T_c=100^\circ C$ )	6.5	-4.7	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	28	-19	A
$P_D$	Total Power Dissipation( $T_c=25^\circ C$ )	5	5	W
	Total Power Dissipation( $T_A=100^\circ C$ )	0.2	0.2	W
EAS	Avalanche energy (Note 3)	25	25	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	-55 To 150	°C

**Table 2. Thermal Characteristic**

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	24	°C/W

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
<b>PARAMETER</b>	<b>CONDITIONS</b>	<b>SYMBOL</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNIT</b>
<b>Static</b> <sup>(Note 4)</sup>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.2	1.5	2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 30V, V_{GS} = 0V$	$I_{DSS}$	--	--	1	$\mu A$
	$V_{DS} = 24V, T_C = 125^\circ\text{C}$		--	--	10	
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$	$R_{DS(on)}$	--	10	14	m $\Omega$
	$V_{GS} = 4.5V, I_D = 6A$		--	14	21	
Forward Transconductance	$V_{DS} = 5V, I_D = 6A$	$g_{fs}$	--	8.0	--	S
<b>Dynamic</b> <sup>(Note 5)</sup>						
Total Gate Charge	$V_{DS} = 15V, I_D = 8A,$ $V_{GS} = 4.5V$	$Q_g$	--	12	--	nC
Gate-Source Charge		$Q_{gs}$	--	4	--	
Gate-Drain Charge		$Q_{gd}$	--	6.0	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	$C_{iss}$	--	800	--	$\mu\text{F}$
Output Capacitance		$C_{oss}$	--	75	--	
Reverse Transfer Capacitance		$C_{rss}$	--	90	--	
<b>Switching</b> <sup>(Note 6)</sup>						
Turn-On Delay Time	$V_{DD} = 15V, I_D = 2A,$ $R_{GEN} = 3.3\Omega$	$t_{d(on)}$	--	7.0	--	ns
Turn-On Rise Time		$t_r$	--	14	--	
Turn-Off Delay Time		$t_{d(off)}$	--	22	--	
Turn-Off Fall Time		$t_f$	--	8	--	

**Notes:**

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3.  $L = 0.1\text{mH}, I_{AS} = 17A, V_{DD} = 25V, R_G = 25\Omega,$  Starting  $T_J = 25^\circ\text{C}$
4. Pulse test:  $PW \leq 300\mu s,$  duty cycle  $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

**N- Channel Typical Electrical and Thermal Characteristics (Curves)**
**•Thermal resistance**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	$R_{thJC}$	-	-	34	$^{\circ}C/W$
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	180	$^{\circ}C/W$
Soldering temperature, wavesoldering for 10s	$T_{sold}$	-	-	265	$^{\circ}C$

**•Electronic Characteristics**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2		-2.5	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=-30V, V_{GS}=0V$			-1.0	$\mu A$
Gate- Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$		27	34	$m\Omega$
		$V_{GS}=-4.5V, I_D=-10A$		35	45	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-5A$		6		S
Source-drain voltage	$V_{SD}$	$I_S=-20A$			1.28	V

**•Electronic Characteristics**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	$C_{iss}$	f = 1MHz	-	850	-	pF
Output capacitance	$C_{oss}$		-	140	-	
Reverse transfer capacitance	$C_{rss}$		-	103	-	

**•Gate Charge characteristics( $T_a = 25^{\circ}C$ )**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	$Q_g$	$V_{DD}=25V$	-	13	-	nC
Gate - Source charge	$Q_{gs}$	$I_D=2A$	-	7	-	
Gate - Drain charge	$Q_{gd}$	$V_{GS}=10V$	-	2	-	

**•N Channel characteristics curve**

Fig.1 Power Dissipation

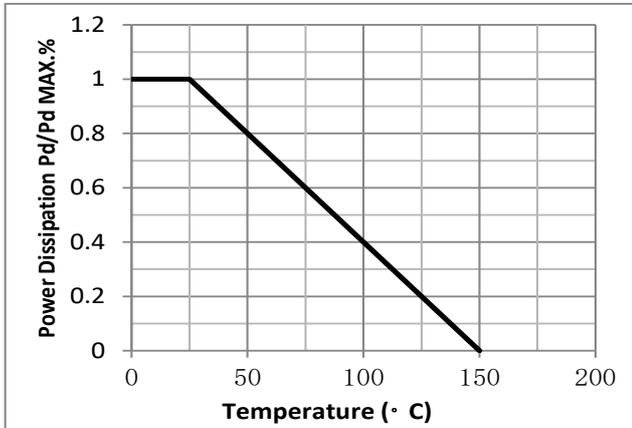


Fig.2 Typical output Characteristics

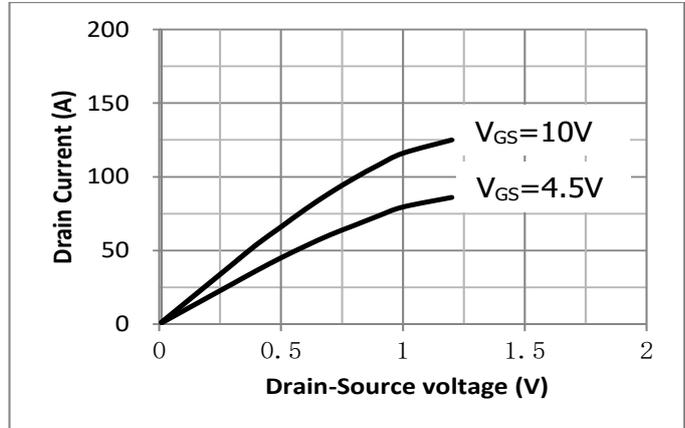


Fig.3 Threshold Voltage V.S Junction Temperature

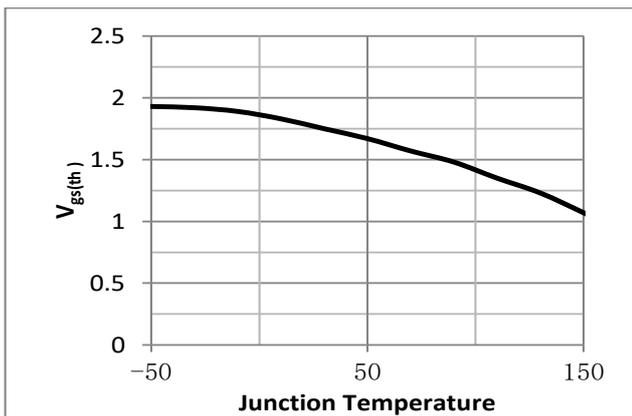


Fig.4 Resistance V.S Drain Current

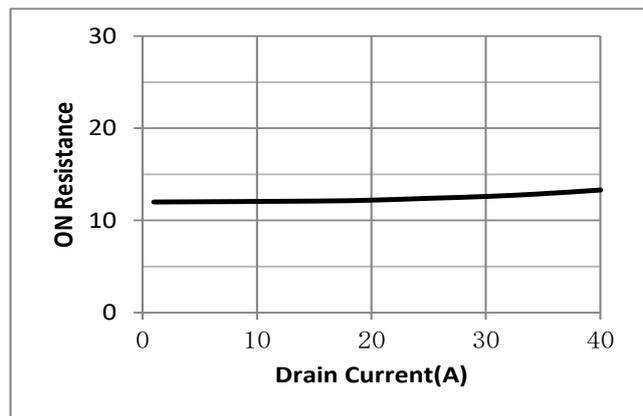


Fig.5 On-Resistance VS Gate Source Voltage

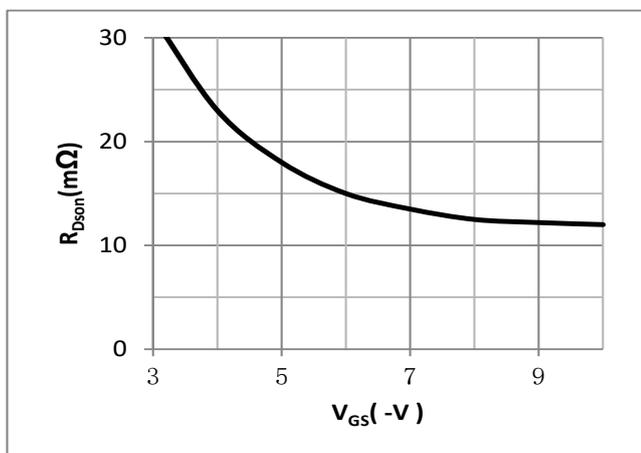
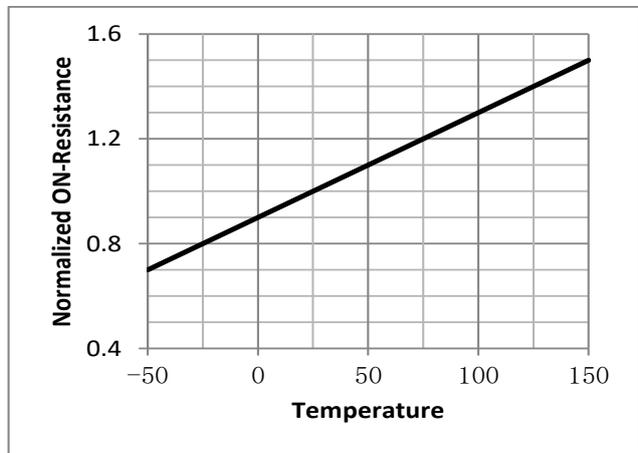


Fig.6 On-Resistance V.S Junction Temperature



•Test Circuit CHANNEL-N

Fig.1 Switching Time Measurement Circuit

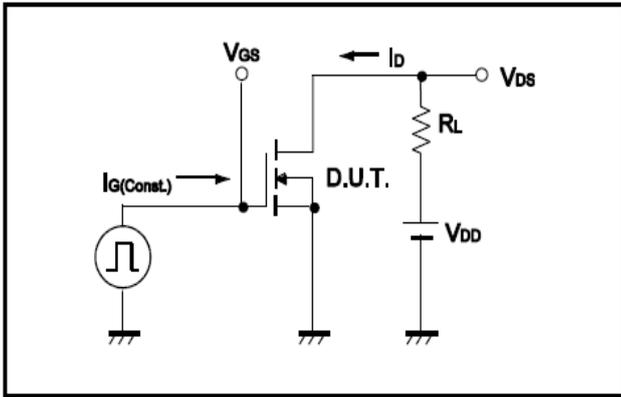


Fig.2 Gate Charge Waveform

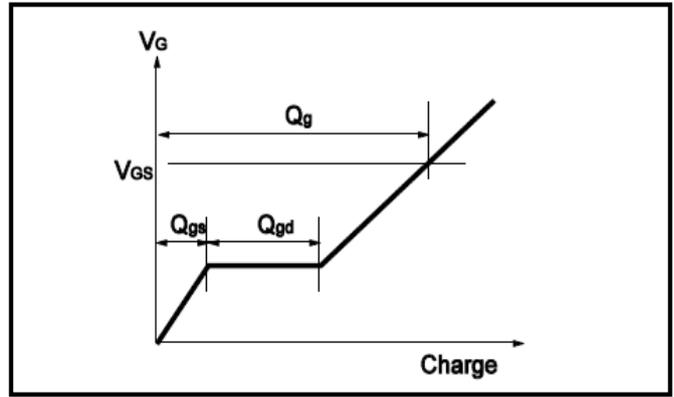


Fig.3 Switching Time Measurement Circuit

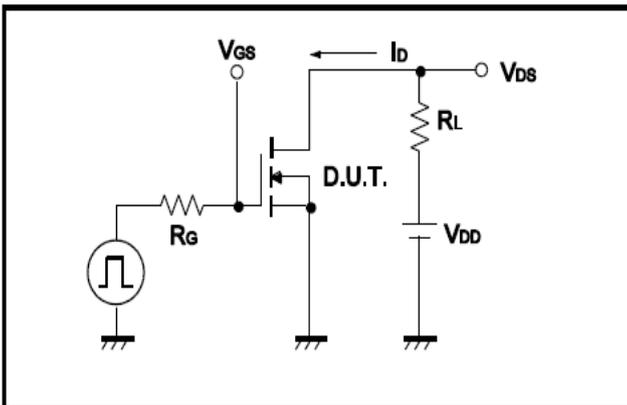


Fig.4 Gate Charge Waveform

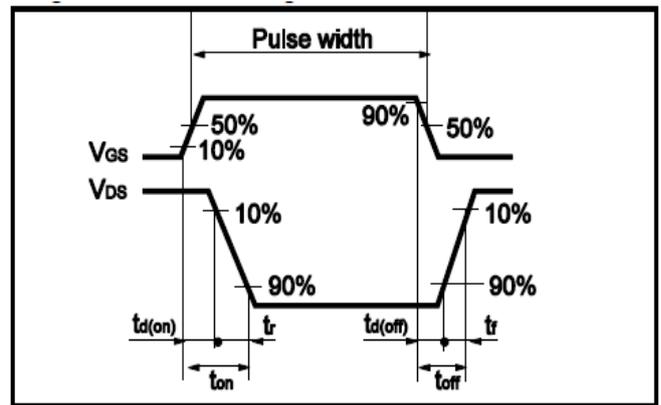


Fig.5 Avalanche Measurement Circuit

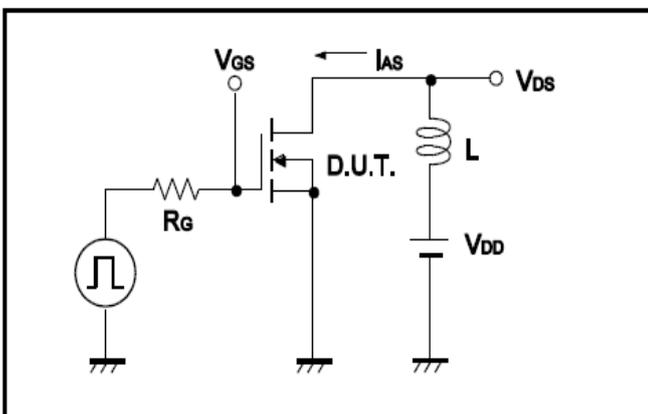
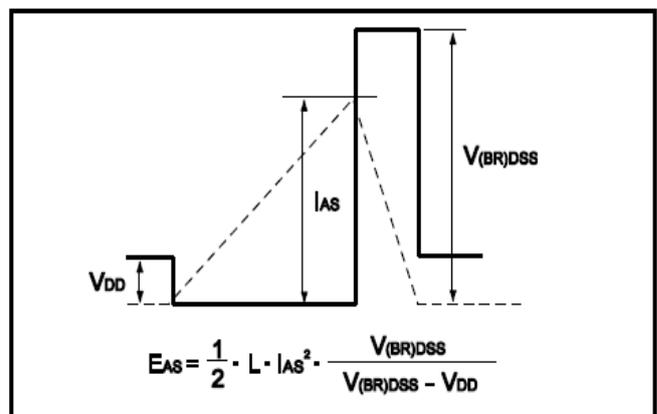


Fig.6 Avalanche Waveform



●P Channel characteristics curve

Fig.1 Power Dissipation Derating Curve

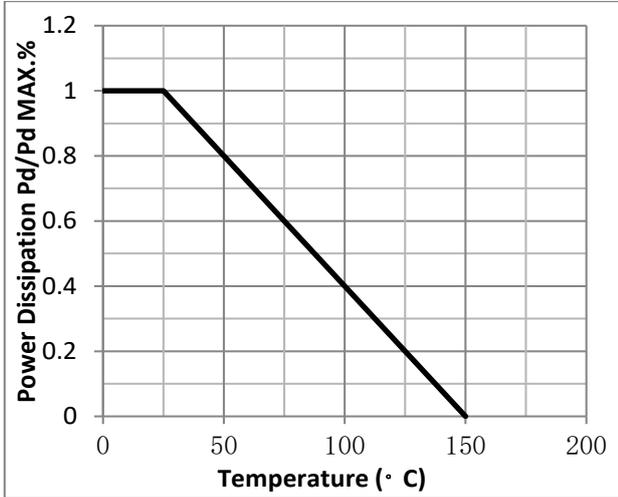


Fig.2 Typical output Characteristics

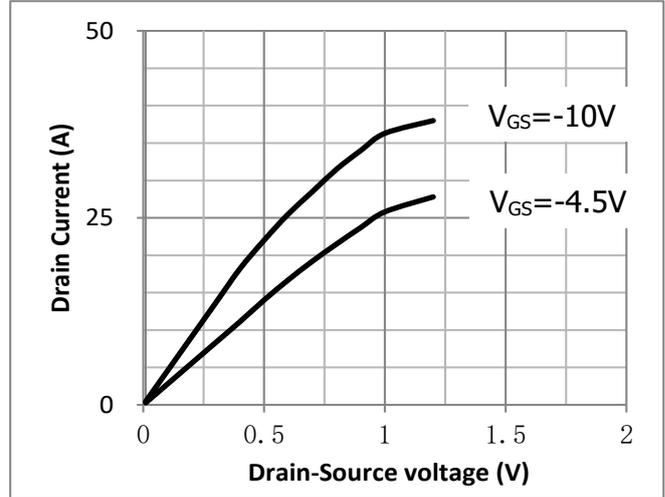


Fig.3 Threshold Voltage V.S Junction Temperature

Fig.4 Resistance V.S Drain Current

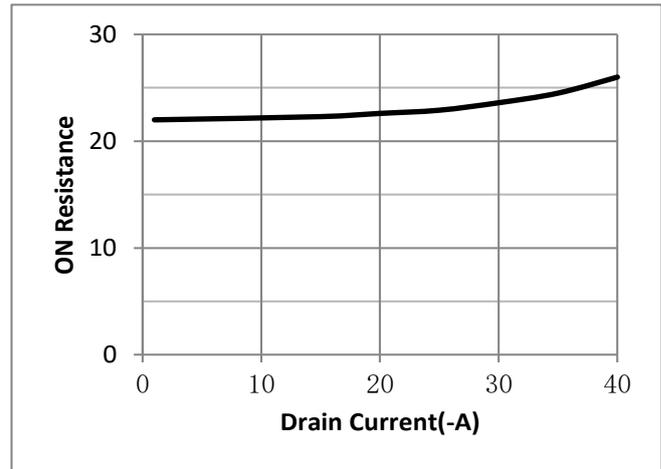
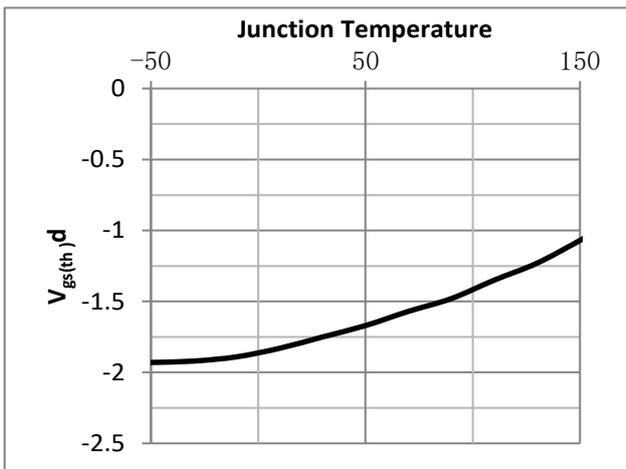
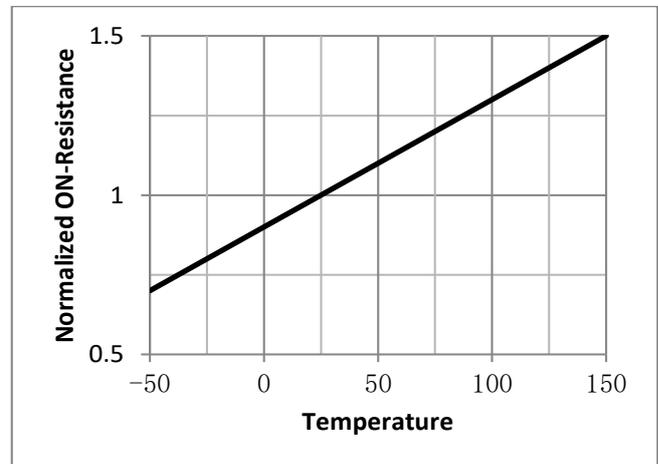
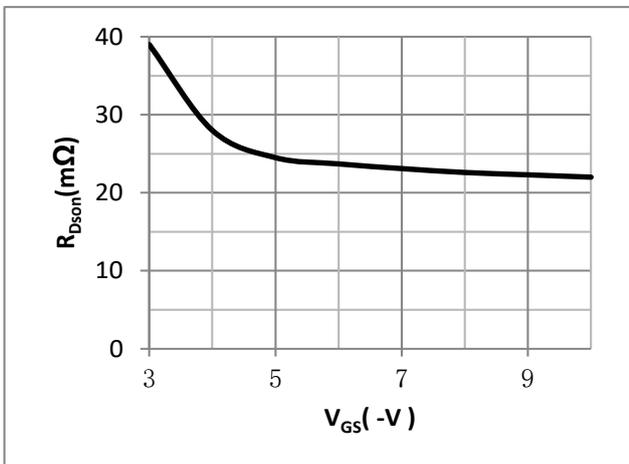


Fig.5 On-Resistance VS Gate Source Voltage

Fig.6 On-Resistance V.S Junction Temperature



•Test Circuit

Fig.1 Switching Time Measurement Circuit

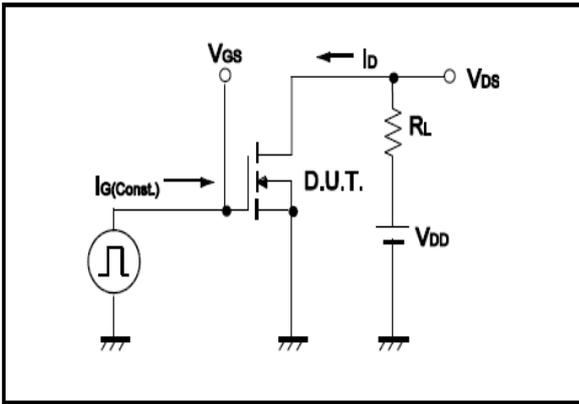


Fig.2 Gate Charge Waveform

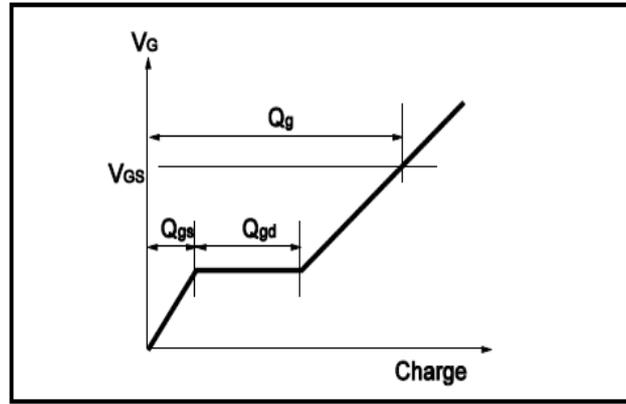


Fig.3 Switching Time Measurement Circuit

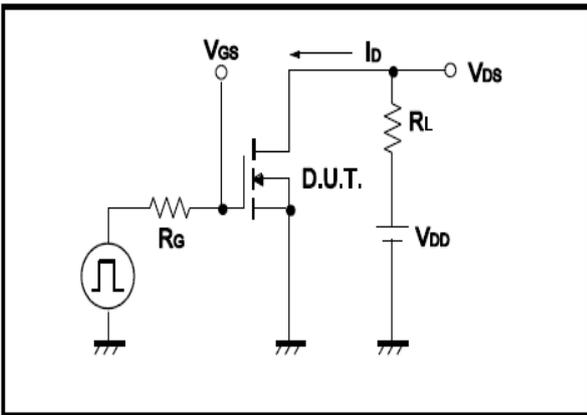


Fig.4 Gate Charge Waveform

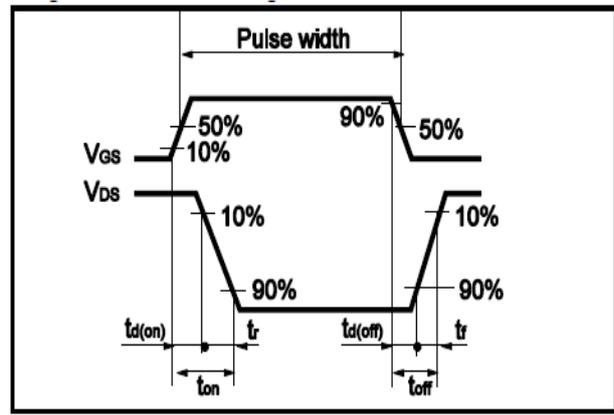


Fig.5 Avalanche Measurement Circuit

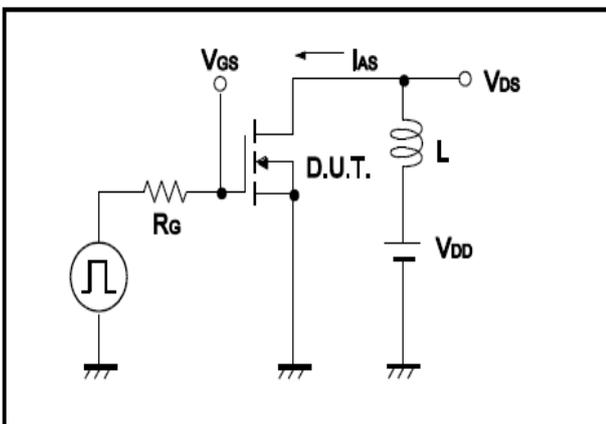
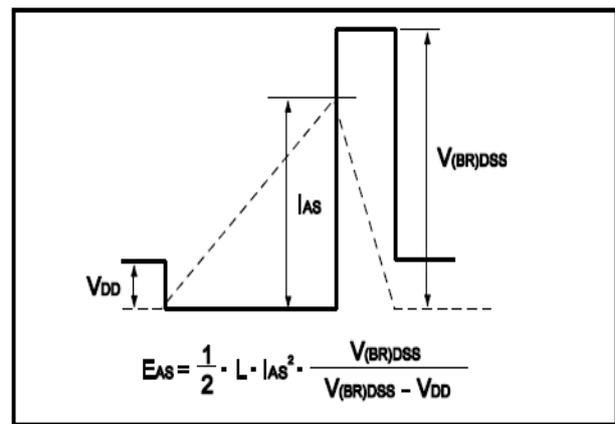
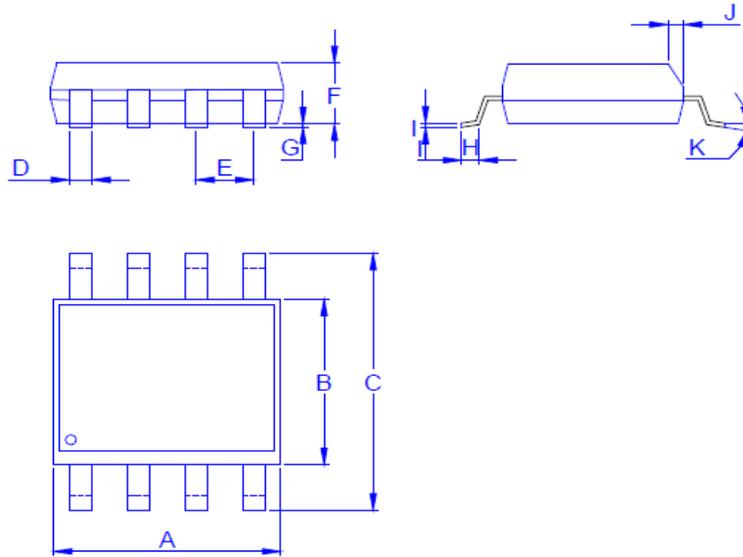


Fig.6 Avalanche Waveform



## Package Outline

**SOIC-8, 8leads**


## Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

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