AZ DISPLAYS,INC.

COMPLETE LCD SOLUTIONS

SPECIFICATIONS FOR
LIQUID CRYSTAL DISPLAY

PART NUMBER: □□ □ □ AGM3224P SERIES

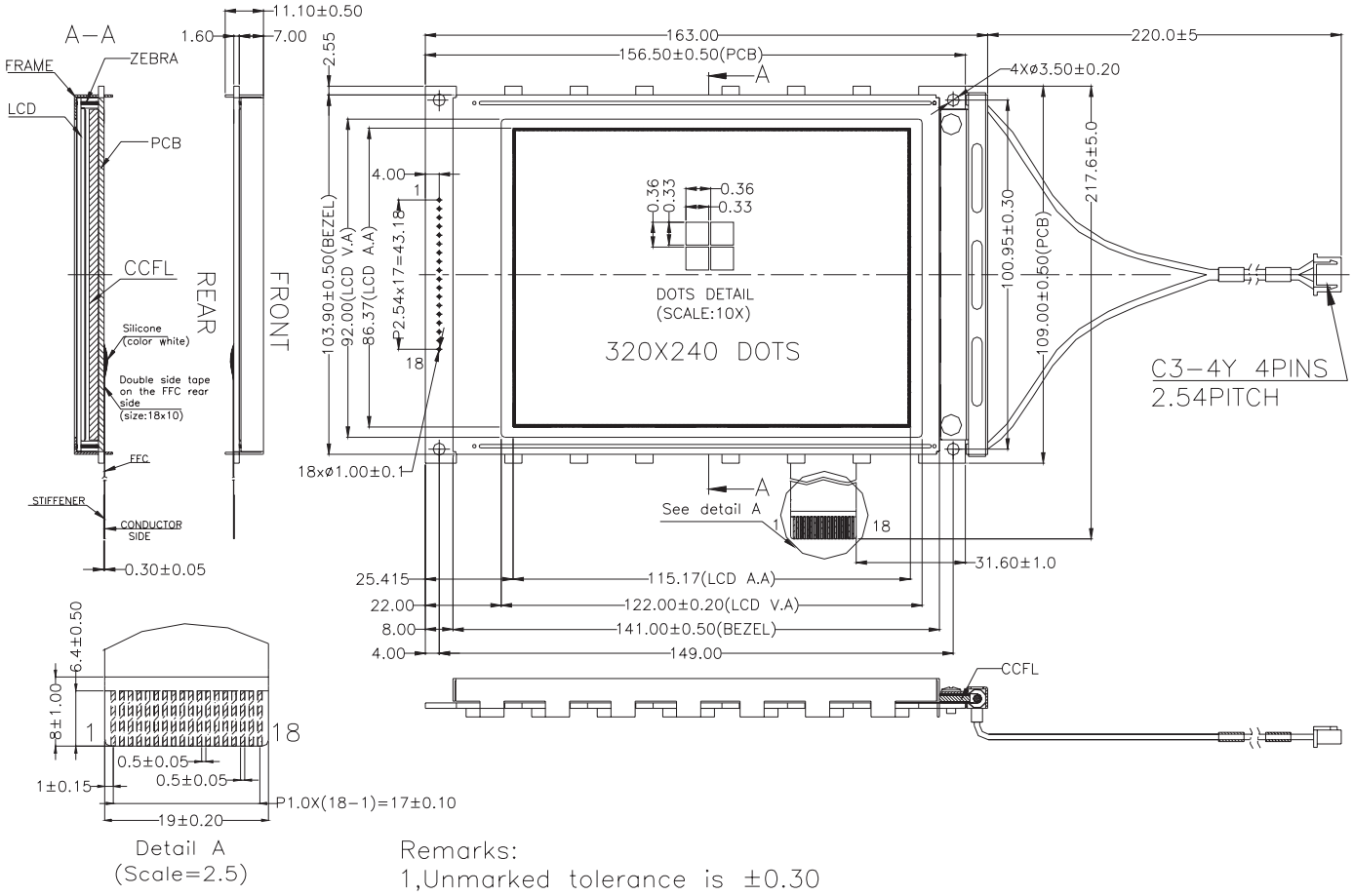
DATE:□ □ □ □ □ □ APRIL 05, 2007

1. FUNCTIONS &FEATURES

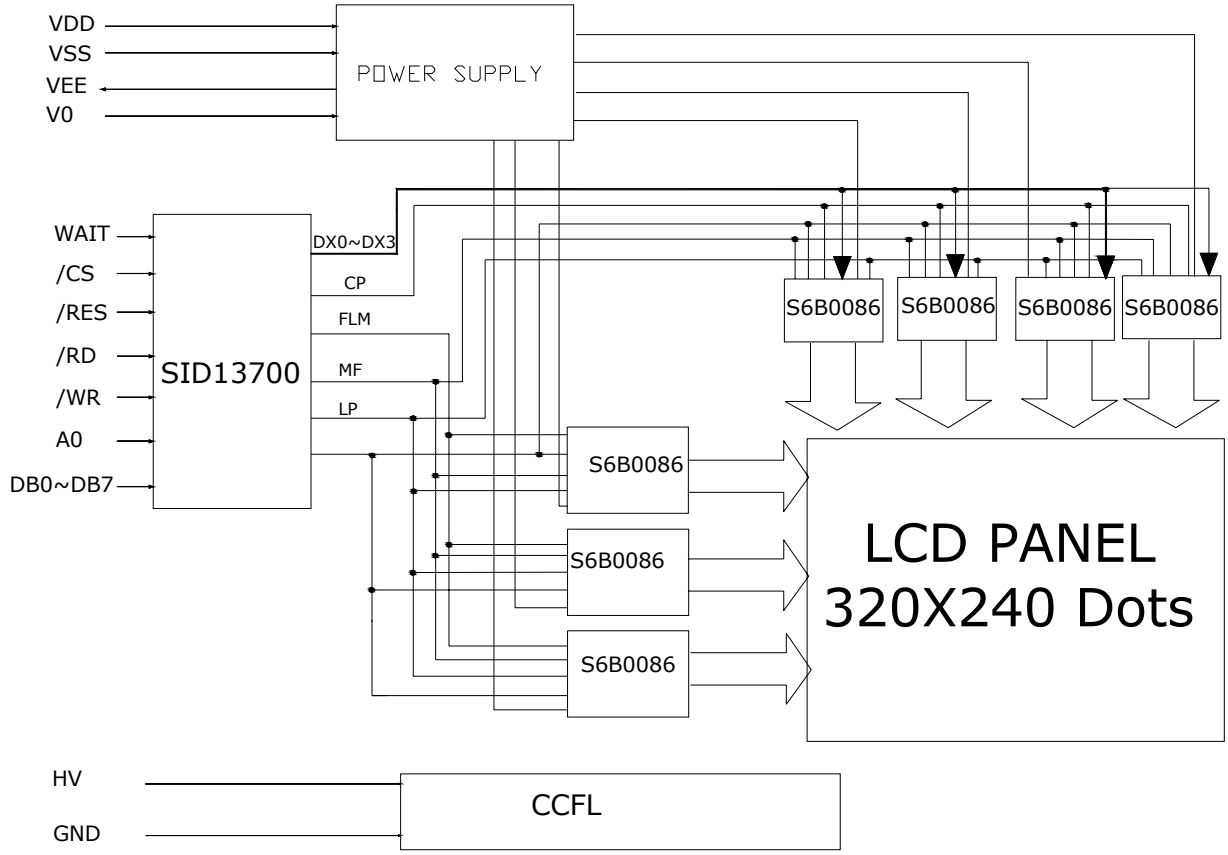
MODULE MODEL	LCD MODEL	LCD TYPE	REMARK
		STN Blue Transmissive Negative Mode	ROHS conformed

Viewing Direction	: 6 O'clock
Driving Scheme	: 1/240 Duty Cycle, 1/16 Bias
Display Content	: 320*240 Dots
Power Supply Voltage	: 5.0V
LCD Driving Voltage (V_{LCD}=V_{DD}-V_0)	: 24.0V
Module Size	: 163(L)*217.6(W)*11.1(T)
Dot Size	: 0.33(W)*0.33(H)mm
Dot Pitch	: 0.36(W)*0.36(H)mm
Negative Power generator	; AIC1652

2. EXTERNAL DIMENSIONS



3. BLOCK DIAGRAM



4. PIN ASSIGNMENT

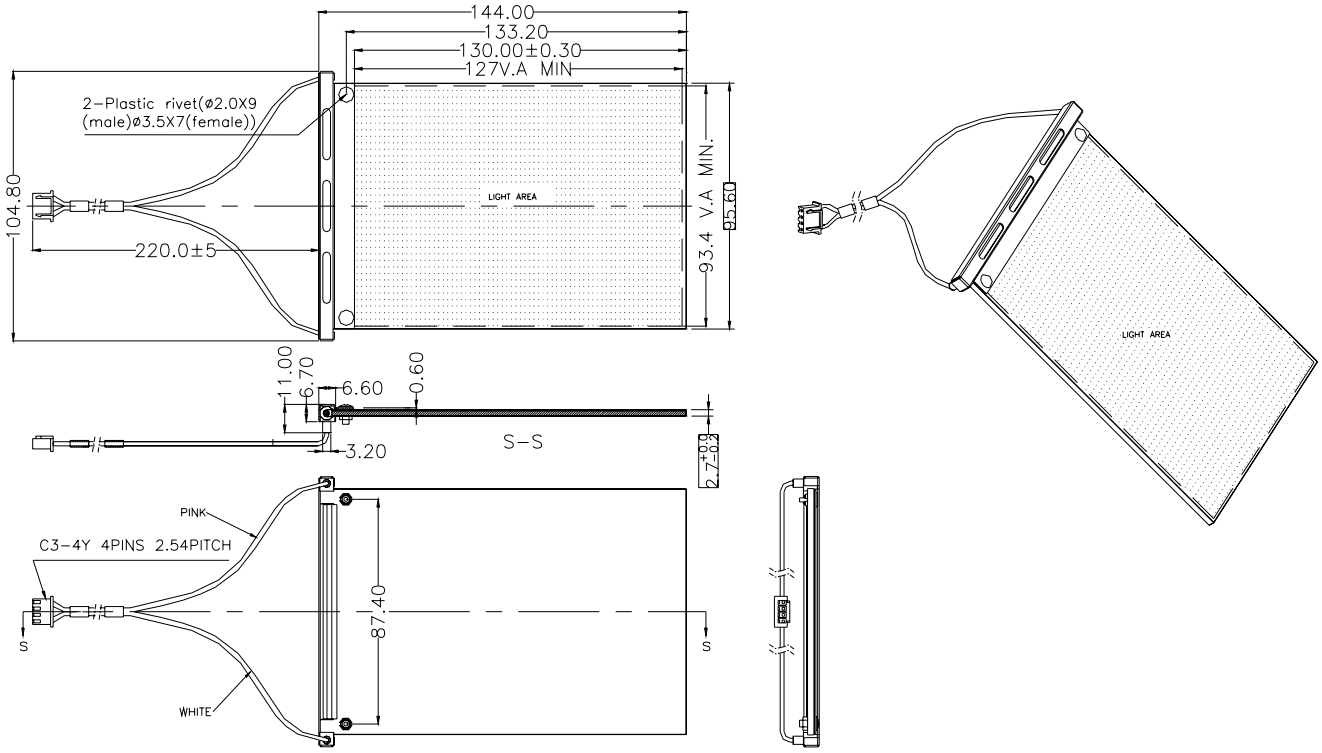
Interface Connector

Pin No.	Symbol	Function
1	WAIT	Wait
2	VSS	Ground terminal of module
3	VEE	Supply voltage for LCD
4	VDD	Power terminal of module(TYP:5.0V)
5~12	DB7~ DB0	Data bus
13	/WR	Data Write
14	/RD	Data Read
15	A0	Command/Data select
16	V0	LCD contrast adjust voltage
17	/CS	Chip selection
18	/RES	Reset signal

CCFL Connector

Pin No.	Symbol	Function
1	HV	Power supply voltage for CCFL
2	NC	No used
3	NC No	used
4	GND	Ground line (from inverter)

5. BACKLIGHT



	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_l		500		V	If=5mA
Forward Current	I_l		5.0	6.0	mA	
Lighting Frequency	fosc	33	55	80	KHz	
Power Dissipation	P_d		1.25	2.5	W	If=5mA
Luminous Intensity	IV	660	750		cd/㎡	
Luminous uniform		75			%	
Emission Wavelength	λ P	0.305	0.320	0.335		If=5mA Ta=25℃
Spectral Range		0.345	0.360	0.375		

	SYMBOL	RATINGS
Operating Temperature	Topr	-20℃ to +70℃
	Tsty	-30℃ to +80℃

6. ABSOLUTE MAXIMUM LIMIT

Item Sy	mbol	MIN	TYP	MAX	UNIT
Operating temperature	Top	-20	--	+70	℃
Storage temperature	Tst	-30	--	+80	℃
Input Voltage	Vi	-0.3	--	Vdd+0.3	V
Supply voltage for logic	Vdd-Vss -0.3		--	+7.0	V
Supply voltage for LCD	Vdd-V0	-0.3	--	+30.0	V
Static electricity	Be sure that you are grounded when handing LCM				

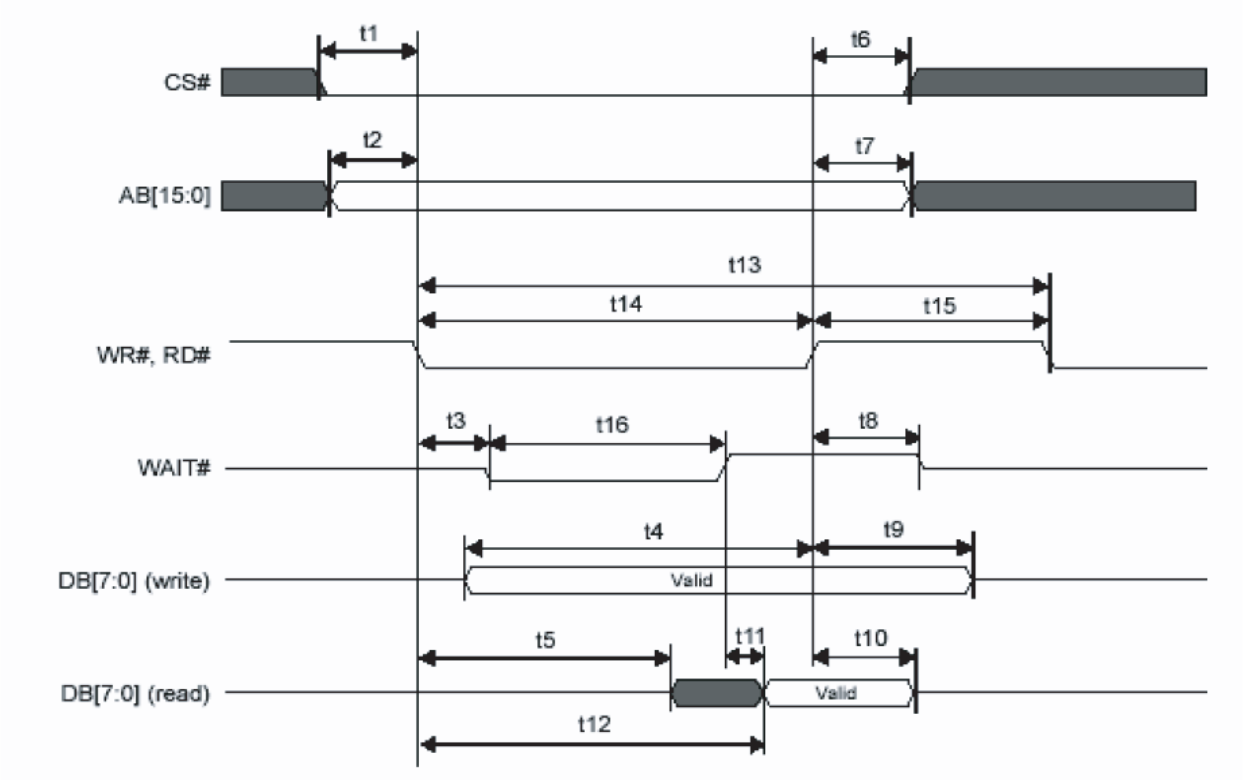
7. ELECTRICAL CHARACTERISTICS

Unless otherwise noted. VSS = 0V

Item Sym	bol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage for logic	Vdd-Vss	-- 2.7		5.0	5.5	V
Supply Voltage for LCD	Vdd -V0	--	6	24.0	28	V
Consumption current	Idd	--	--	TBD	--	mA

8. S1D13700 TIMING DIAGRAMS

Generic Bus Direct/Indirect Interface with WAIT Timing

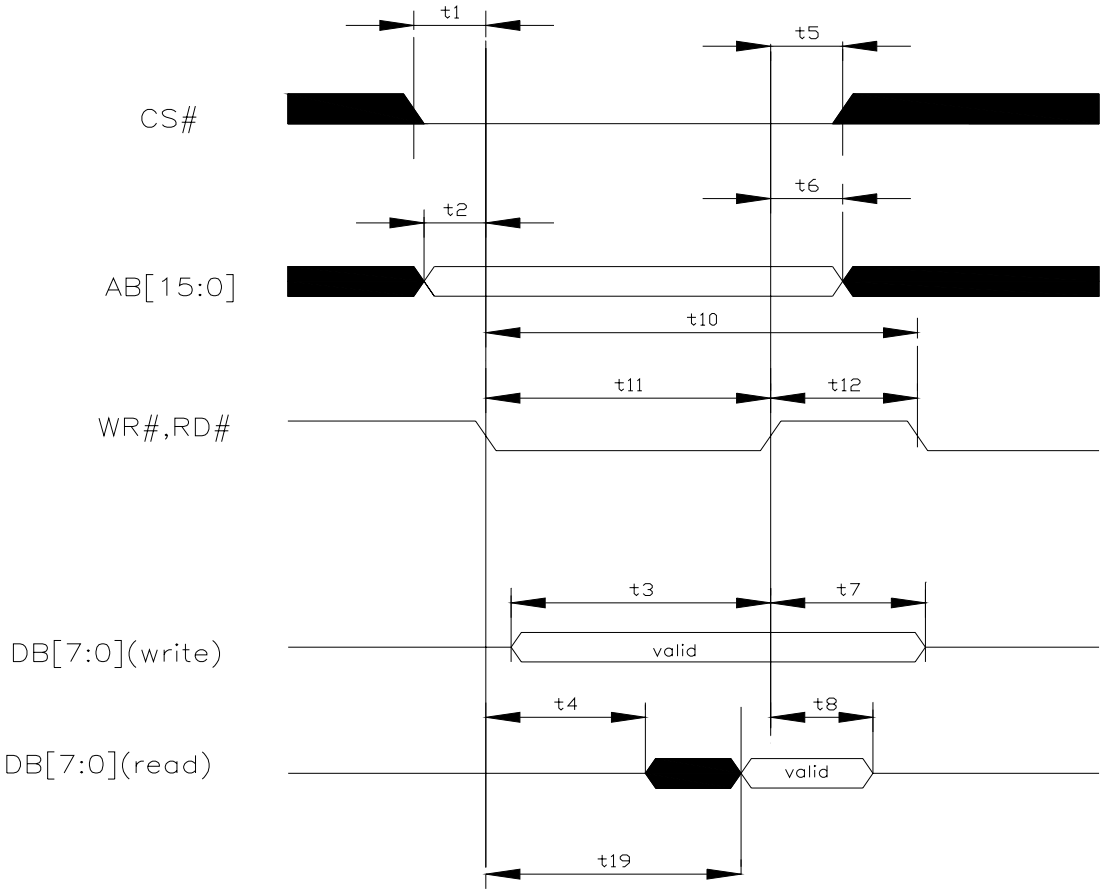


Generic Bus Direct/Indirect Interface with WAIT Timing

Symbol	Para meter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	-- 5	--		ns
t2	AB[15:0] setup time	5	-- 5	--		ns
t3	WR#, RD# falling edge to WAIT# driven low	2	15	2	--	ns
t4	DB[7:0] setup time to WR# rising edge (write cycle)	Note2	--	Note2	15	ns
t5	RD# falling edge to DB[7:0] driven (read cycle)	3	-- 3	--		ns
t6	CS# hold time	7	-- 7	--		ns
t7	AB[15:0] hold time	7	-- 7	--		ns
t8	RD#, WR# rising edge to WAIT# high impedance	2	10	2	10	ns
t9	DB[7:0] hold time from WR# rising edge (write cycle)	5	-- 5	--		ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t11	WAIT# rising edge to valid Data if WAIT# is used	--	Note3	--	Note 3	ns
t12	RD# falling edge to valid Data if WAIT# is not used	--	Note 4	--	Note 4	ns
t13	RD#, WR# cycle time	Note5	--	Note5	--	ns
t14	RD#, WR# pulse active time	5	-- 5	--		Ts
t15	RD#, WR# pulse inactive time	Note6	--	Note 6	--	ns
t16	WAIT# pulse active time	--	Note7	--	Note 7	ns

1. Ts = System clock period
2. t4min = 2Ts + 5
3. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
4. t12max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
5. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
7. t16max = 4Ts + 2

Generic Bus Direct/Indirect Interface without WAIT Timing

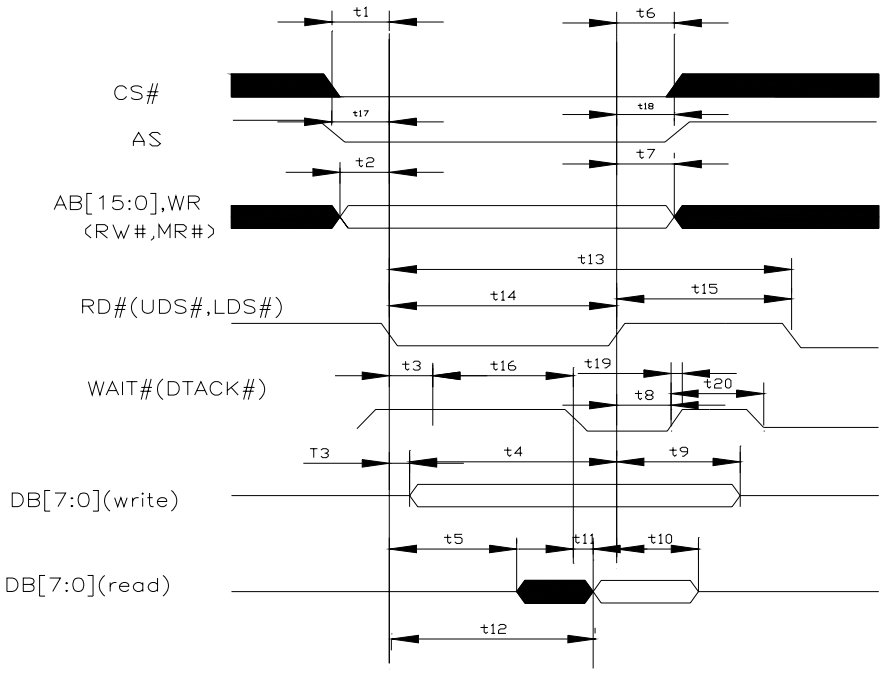


Symbol	Parameter	VDD=4.5 to 5.5V		VDD=2.7 to 4.5V		Unit
		min	max	min	max	
t1	CS# setup time	5	--	5	--	ns
t2	AB[15:0] setup time	5	--	5	---	ns
t3	DB[7:0] setup time to WR# rising edge (write cycle)	Note 2	--	Note 2	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	--	3	--	ns
t5	CS# hold time	7	--	7	--	ns
t6	AB[15:0] hold time	7	--	7	--	ns
t7	DB[7:0] hold time from WR# rising edge (write cycle)	5	--	5	--	ns
t8	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t9	RD# falling edge to valid Data (read cycle)	--	Note 3	--	Note 3	ns
t10	RD#, WR# cycle time	Note 4	--	Note 4	--	ns
t11	RD#, WR# pulse active time	5	--	5	--	Ts
t12	RD#, WR# pulse inactive time	Note 5	--	Note 5	--	ns

Note:

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

MC68K Family Bus Indirect/Direct Interface with DTACK# Timing

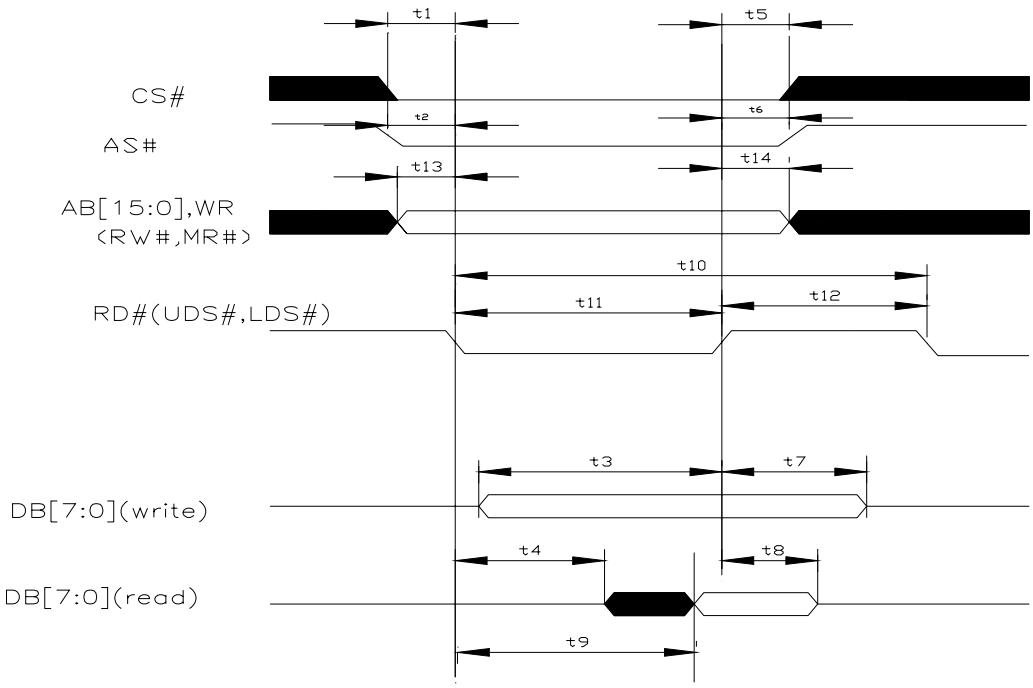


Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	--	5	--	ns
t2	AB[15:0] setup time	5	--	5	--	ns
t3	AS# falling edge to WAIT# driven	2	15	2	15	ns
t4	DB[7:0] setup time to RD# rising edge (write cycle)	Note2	--	Note2	--	ns
t5	RD# falling edge to DB[7:0] driven (read cycle)	3	--	3	--	ns
t6	CS# hold time	7	--	7	--	ns
t7	AB[15:0] hold time	7	--	7	--	ns
t8	RD# rising edge to WAIT# high impedance if Direct interface and in Power Save Mode	2	10	2	10	ns
t9	DB[7:0] hold time from RD# rising edge (write cycle)	5	--	5	--	ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t11	WAIT# falling edge to valid Data if WAIT# is used	--	Note3	--	Note 3	ns
t12	RD# falling edge to valid Data if WAIT# is not used	--	Note 4	--	Note 4	ns
t13	RD# cycle time	Note5	--	Note5	--	ns
t14	RD# pulse active time	5	--	5	--	Ts
t15	RD# pulse inactive time	Note6	--	Note 6	--	ns
t16	WAIT# pulse inactive time from WAIT# driven	--	Note7	--	Note 7	Ns
17	AS# setup time	0	--	0	--	ns
18	AS# hold time	0	--	0	--	ns
19	AS# rising edge to WAIT# high de-asserted if not Direct interface and not in Power Save Mode	--	10	--	10	ns
20	WAIT# pulse inactive time	0	N ote 8	0	N ote 8	ns

Note:

1. Ts = System clock period
2. t4min = 2Ts + 5
3. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
4. t12max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
5. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
7. t16max = 4Ts + 2
8. t20max = 1Ts - 15

MC68K Family Bus Indirect/Direct Interface without DTACK# Timing

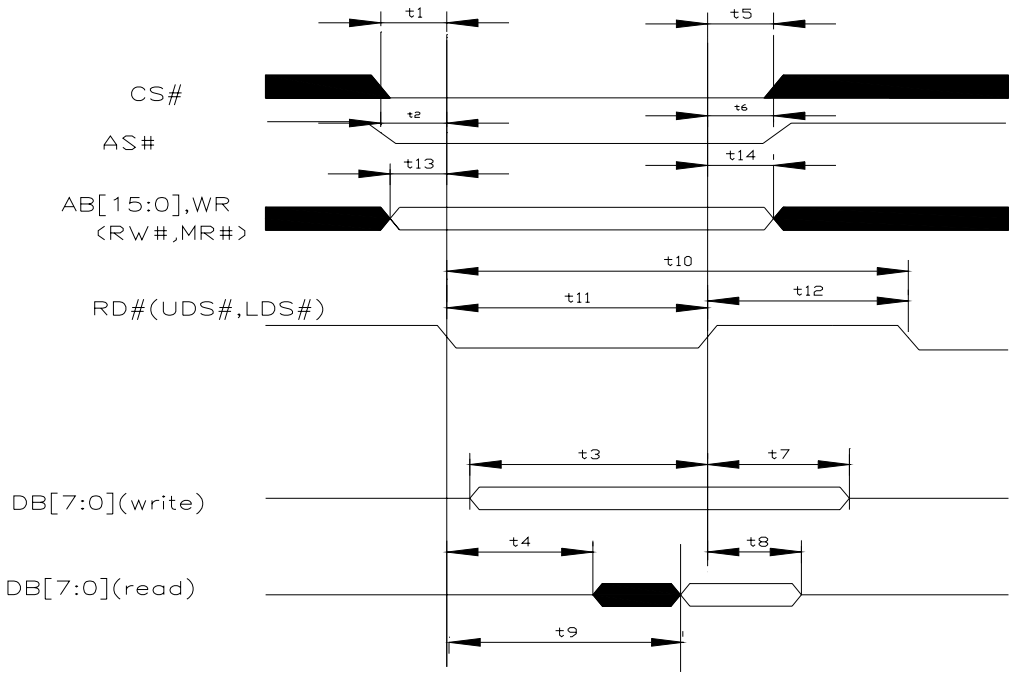


Symbol	Para meter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	-- 5	--		ns
t2	AB[15:0] setup time	5	-- 5	--		ns
t3	DB[7:0] setup time to RD# rising edge (write cycle)	Note2	--	Note2	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	-- 3	--		ns
t5	CS# hold time	7	-- 7	--		ns
t6	AB[15:0] hold time	7	-- 7	--		ns
t7	DB[7:0] hold time from RD# rising edge (write cycle)	5	-- 5	--		ns
t8	DB[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	--	Note 3	--	Note 3	ns
t10	RD# cycle time	Note 4	--	Note 4	--	ns
t11	RD# pulse active time	5	-- 5	--		Ts
t12	RD# pulse inactive time	Note 5	--	Note5	--	ns
t13	AS# setup time	0	-- 0	--		ns
t14	AS# hold time	0	-- 0	--		ns

Note:

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

M68K Family Bus Indirect Interface Timing



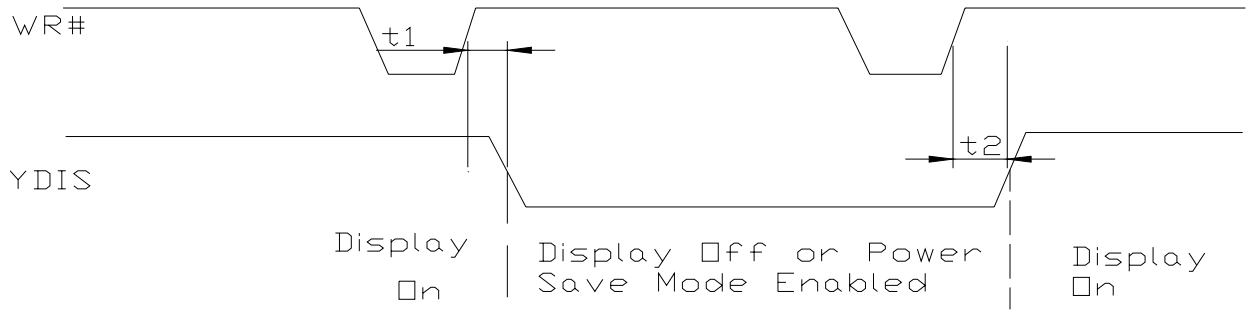
Note:CLK input to the M6800 interface must be driven synchronous to the host microprocessor.

Symbol	Para meter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	-- 5	--		ns
t2	AB[15:0] setup time	5	-- 5	--		ns
t3	DB[7:0] setup time to RD# falling edge (write cycle)	Note2	--	Note2	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	-- 3	--		ns
t5	CS# hold time	7	-- 7	--		ns
t6	AB[15:0] hold time	7	-- 7	--		ns
t7	DB[7:0] hold time from RD# falling edge (write cycle)	5	-- 5	--		ns
t8	DB[7:0] hold time from RD# falling edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	--	Note 3	--	Note 3	ns
t10	RD# cycle time	Note 4	--	Note 4	--	ns
t11	RD# pulse active time	5	-- 5	--		Ts
t12	RD# pulse inactive time	Note 5	--	Note5	--	ns
t13	AS# setup time	0	-- 0	--		ns
t14	AS# hold time	0	-- 0	--		ns

Note:

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

Power Save Mode/Display Enable Timing



Symbol	Para meter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1a	YDIS falling edge delay for Power Save Mode Enable in Indirect Mode (see Note 2)	--	2 --	2		Frames
t1b	YDIS falling edge delay for Display Off in Indirect Mode (58h)	--	1Ts+10	--	1Ts+10	ns
t1c	YDIS falling edge delay for Display Off in Direct Mode (see Note 3)	--	2Ts+10	--	2Ts+10	ns
t2	YDIS rising edge delay for Display On (see Note 3)	--	2Ts+10	--	2Ts+10	ns

Note:

1. Ts = System Clock Period
2. Power Save Mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0.
3. Display On/Off is controlled by the Display Enable bit, REG[09h] bit 0.

9. INDIRECT ADDRESSING COMMAND

Indirect Addressing Command

Indirect Addressing Command

Class	Register Address	Command	Register Description	Control Byte Value	No. of Bytes
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
Display Control	8009h - 800A	DISP ON/OFF	Enables/disables display and display attributes	58h 59h	1
	800Bh - 8014h	SCROLL	Sets screen block start addresses and sizes	44h	10
	8015h - 8016h	CSRFORM	Sets cursor type	5Dh	2
	8017h	CSRDIR	Sets direction of cursor movement	4Ch - 4Fh	0
	8018h	OVLAY	Sets display overlay format	5Bh	1
	8019h - 801Ah	CGRAM ADR	Sets start address of character generator RAM	5Ch	2
	801Bh	HDOT SCR	Sets horizontal scroll position	5A	1
Drawing Control	801Ch - 801Dh	CSRW	Sets cursor address	46h	2
	801Eh - 801Fh	CSRR	Reads cursor address	47h	2
	8020h	GRAYSCALE	Sets the Grayscale depth (bpp)	60h	1
Memory Control		MEMWRITE	Writes to memory	42h	n/a
		MEMREAD	Reads from memory	43h	

Command Set

In general, the internal registers of the SED13700 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.

2-byte parameter (where two bytes are treated as 1 data item) are handled as follows:

1. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
2. System Set, Scroll, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

10. CHARACTER GENERATOR

1. CG Characteristics

Internal Character Generator

The internal character generator is recommended for minimum system configurations containing a S1D13700, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5 x 7 pixel font
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CGRAM characters)
- Can be automatically spaced out up to 8 x 16 pixels

Character Generator RAM

The character generator RAM can be used for storing graphics characters. The character generator RAM can be mapped to any display memory location by the microprocessor, allowing effective usage of unused address space.

- Up to 8 x 8 pixel characters when REG[00h] bit 2 = 0 and 8 x 16 characters when REG[00h] bit 2 = 1
- Can be mapped anywhere in display memory address space if used with the character generator ROM (REG[00h] bit 0 = 0)

2.Setting the Character Generator Address

The CGRAM addresses in the display memory address space are not mapped directly from
the address in the Character Generator RAM Start Address registers, REG[19h] -REG[1Ah]. The data to be displayed is at a CGRAM address calculated from (REG[19h] -REG[1Ah]) + character code + ROW select address.
The following tables show the address mapping for CGRAM addresses.

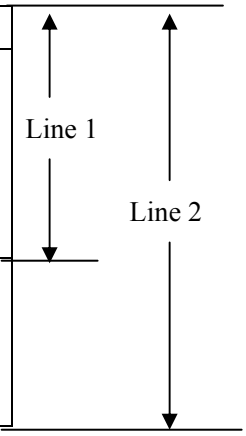
Character Fonts Where Number of Lines 8 (REG[00h] bit 2 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Character fonts, 9≧number of lines≧16 (M2=1, M1=0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

R_{OW}	R3	R2	R1	R0
$R_{OW}0$	0	0	0	0
$R_{OW}1$	0	0	0	1
$R_{OW}2$	0	0	1	0
↓	↓	↓	↓	↓
$R_{OW}7$	0	1	1	1
$R_{OW}8$	1	0	0	0
↓	↓	↓	↓	↓
$R_{OW}14$	1	1	1	0
$R_{OW}15$	1	1	1	1



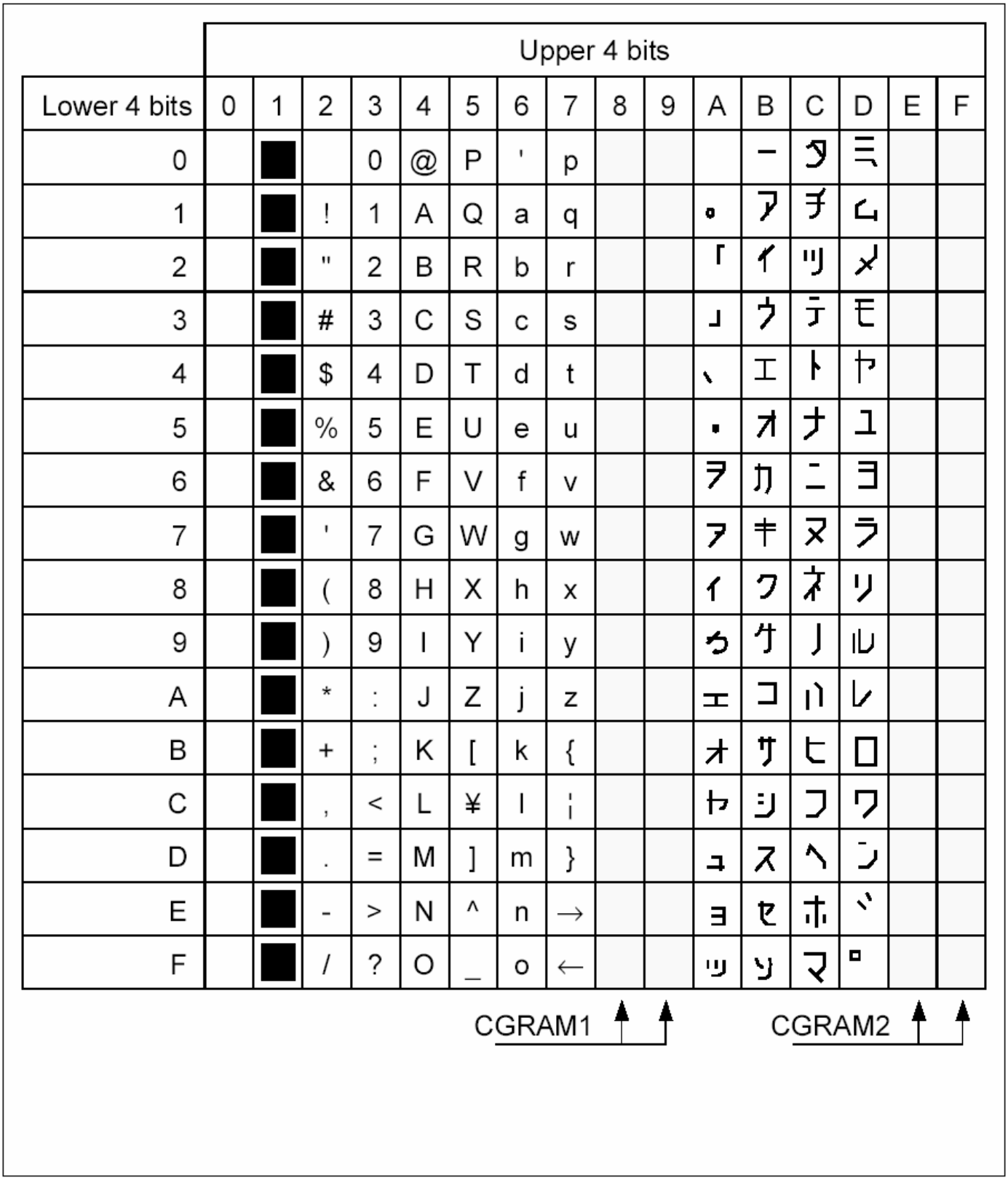
Row select address

Note: Lines=1: lines in the character bitmap≧8

Lines=2: lines in the character bitmap≧9

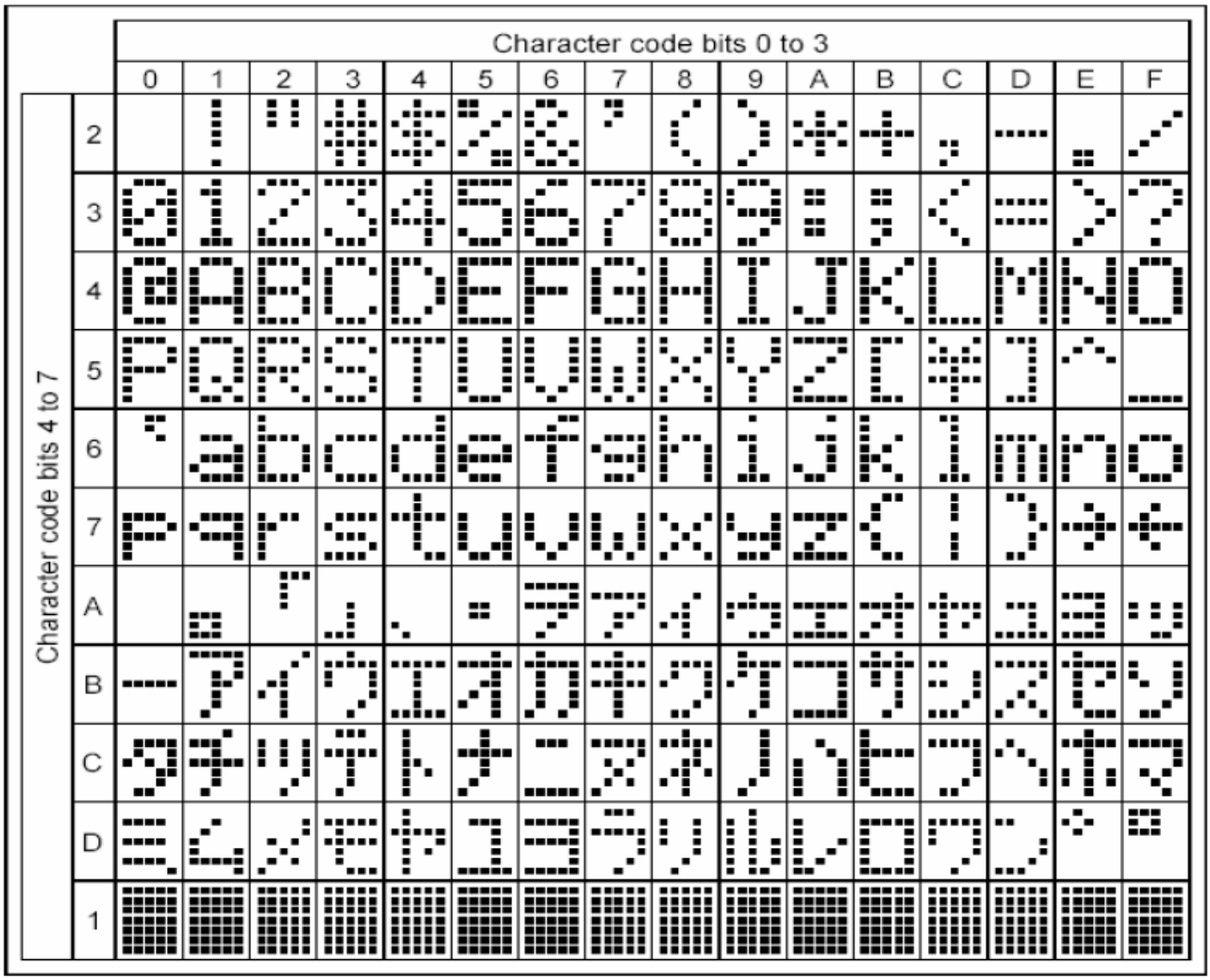
3. Character Codes

The following figure shows the character codes and the codes allocated to CG RAM. ALL codes can be used by the CG RAM if not using the internal ROM, but the CGRAM address must be set to 0.



On- chip character codes

4. Internal Character Generator Font



Note:The shaded positions indicate characters that have the whole 6 · 8 bitmap blackened.

11. MICROPRCESSOR INTERFACE

1 .System Bus Interface

CNF[4:0], A[15:1], A0, D[7:0], RD#, WR#, AS and CS are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. CNF[4:2] change the operation of the RD# and WR# pins to enable interfacing to either a Generic (Z80), M6800, or MC68K family bus, and should be pulled-up or pulleddown

Generic

The following table shows the signal states for each function.

Generic Interface Signals

A0	RD#	WR#	Function
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

2. M6800 Series

M6800 Series interface signals

A0	R/W#	E	Function
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

3. MC68K Series

MC68K series interface signals

A0	RD/WR#	LDS#	Function
1	1	0	Display data and cursor address read
0	0	0	Display data and parameter write
1	0	0	Command write

12. PCB DRAWING