

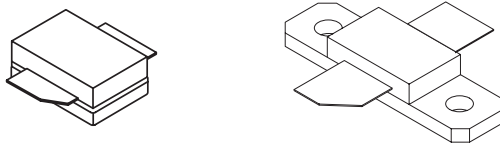


AGR09045E

45 W, 865 MHz—895 MHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR09045E is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for cellular band, code-division multiple access (CDMA), global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and time-division multiple access (TDMA) single and multicarrier class AB wireless base station amplifier applications. This device is manufactured on an advanced LDMOS technology, offering state-of-the-art performance, reliability, and thermal resistance. Packaged in an industry-standard CuW package capable of delivering a minimum output power of 45 W, it is ideally suited for today's RF power amplifier applications.



AGR09045EU (unflanged) AGR09045EF (flanged)

Figure 1. Available Packages

Features

Typical performance ratings are for IS-95 CDMA, pilot, sync, paging, traffic codes 8—13:

- Output power (POUT): 10 W.
- Power gain: 20 dB.
- Efficiency: 28%.
- Adjacent channel power ratio (ACPR) for 30 kHz bandwidth (BW):
(750 kHz offset: -45 dBc)
(1.98 MHz offset: -60 dBc).
- Input return loss: 10 dB.

High-reliability, gold-metalization process.

High gain, efficiency, and linearity.

Integrated ESD protection.

Si LDMOS.

Industry-standard packages.

45 W minimum output power.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR09045EU	R _{JC}	1.2	°C/W
AGR09045EF	R _{JC}	1.5	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V _{DSS}	65	Vdc
Gate-source Voltage	V _{GS}	-0.5, +15	Vdc
Drain Current—Continuous	I _D	4.25	Adc
Total Dissipation at T _C = 25 °C:			
AGR09045EU	P _D	146	W
AGR09045EF	P _D	117	W
Derate Above 25 °C:			
AGR09045EU	—	0.83	W/°C
AGR09045EF	—	0.67	W/°C
Operating Junction Temperature	T _J	200	°C
Storage Temperature Range	T _{STG}	-65, +150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR09045E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: $T_c = 30\text{ }^{\circ}\text{C}$.

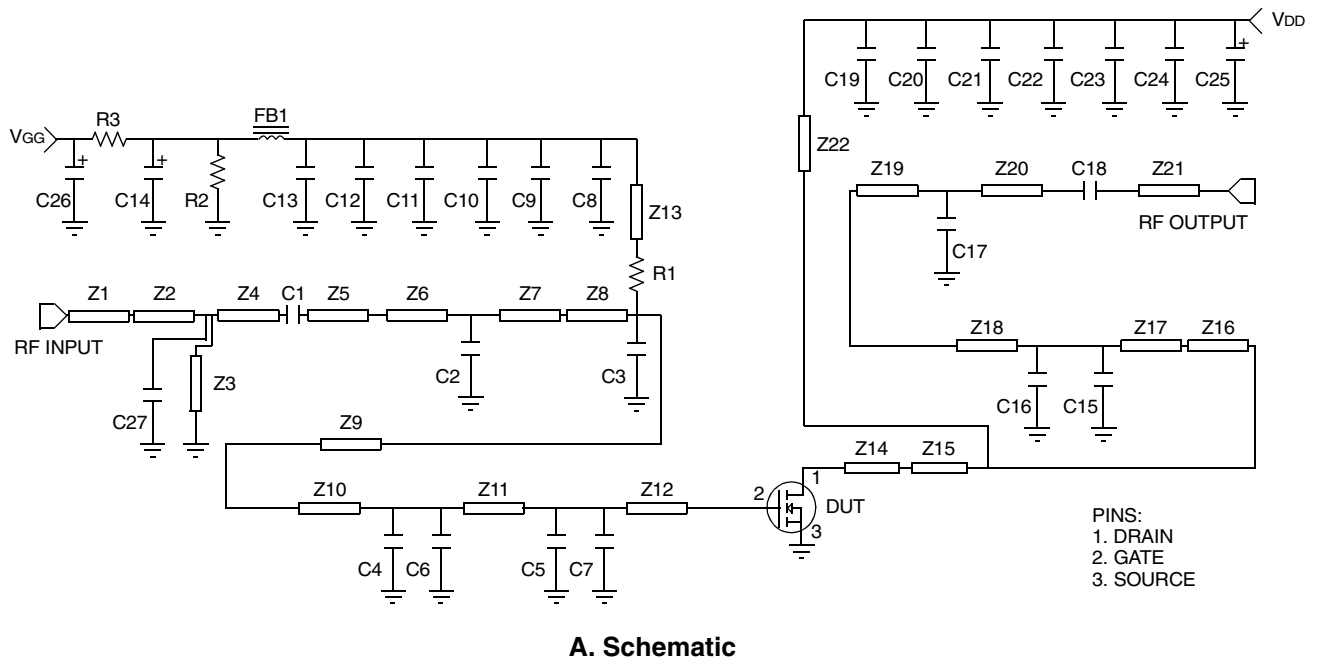
Table 4. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage ($V_{GS} = 0$, $I_D = 100\text{ }\mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current ($V_{GS} = 5\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	—	—	1.3	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$)	I_{DSS}	—	—	4	μAdc
On Characteristics					
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 1.0\text{ A}$)	G_{FS}	—	3	—	S
Gate Threshold Voltage ($V_{DS} = 10\text{ V}$, $I_D = 400\text{ }\mu\text{A}$)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$)	$V_{GS(Q)}$	—	3.5	—	Vdc
Drain-source On-voltage ($V_{GS} = 10\text{ V}$, $I_D = 1.0\text{ A}$)	$V_{DS(ON)}$	—	0.25	—	Vdc

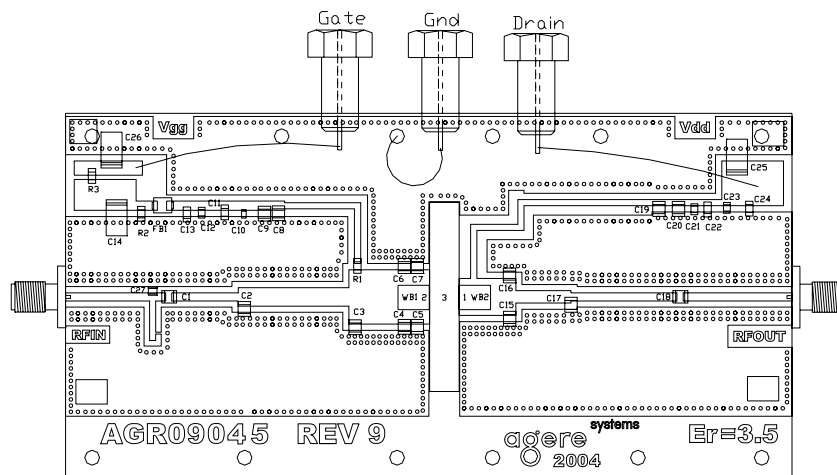
Table 5. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Input Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{ISS}	—	73	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{OSS}	—	23	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{RSS}	—	1.2	—	pF
Functional Tests (in Agere Systems Supplied Test Fixture) (Test frequencies (f) = 865 MHz, 880 MHz, 895 MHz)					
Linear Power Gain ($V_{DS} = 28\text{ V}$, $P_{OUT} = 6\text{ W}$, $I_{DQ} = 450\text{ mA}$)	GL	19	20	—	dB
Output Power ($V_{DS} = 28\text{ V}$, 1 dB compression, $I_{DQ} = 450\text{ mA}$)	P_{1dB}	45	60	—	W
Drain Efficiency ($V_{DS} = 28\text{ V}$, $P_{OUT} = P_{1dB}$, $I_{DQ} = 450\text{ mA}$)		—	59	—	%
Third-order Intermodulation Distortion (100 kHz spacing, $V_{DS} = 28\text{ V}$, $P_{OUT} = 45\text{ WPEP}$, $I_{DQ} = 450\text{ mA}$)	IMD	—	−31	—	dBc
Input Return Loss	IRL	—	10	—	dB
Ruggedness ($V_{DS} = 28\text{ V}$, $P_{OUT} = 45\text{ W}$, $I_{DQ} = 450\text{ mA}$, $f = 880\text{ MHz}$, $V_{SWR} = 10:1$, all angles)	—	No degradation in output power.			

Test Circuit Illustrations for AGR09045E



A. Schematic



Parts List:

Microstrip line: Z1 0.670 in. x 0.066 in.; Z2 0.035 in. x 0.066 in.; Z3 0.297 in. x 0.050 in.; Z4 0.069 in. x 0.066 in.; Z5 0.538 in. x 0.066 in.; Z6 0.050 in. x 0.150 in.; Z7 0.797 in. x 0.150 in.; Z8 0.050 in. x 0.440 in.; Z9 0.299 in. x 0.440 in.; Z10 0.050 in. x 0.440 in.; Z11 0.050 in. x 0.440 in.; Z12 0.494 in. x 0.440 in.; Z13 1.024 in. x 0.050 in.; Z14 0.093 in. x 0.300 in.; Z15 0.050 in. x 0.300 in.; Z16 0.214 in. x 0.300 in.; Z17 0.050 in. x 0.300 in.; Z18 0.396 in. x 0.300 in.; Z19 0.050 x 0.300; Z20 0.808 in. x 0.066 in.; Z21 0.881 in. x 0.066 in.; Z22 2.048 in. x 0.050 in.

ATC® chip capacitor: C1, C8, C18, C19: 47 pF, 100B470JW; C2: 3.3 pF, 100B3R3BW; C3: 5.6 pF, 100B5R6BW;
 C4, C5, C6, C7: 12 pF, 100B120JW; C9, C16, C20: 10 pF, 100B100JW; C15: 1.8 pF, 100B1R8BW; C17: 6.8 pF, 100B6R8BW;
 C27: 8.2 pF, 100A8R2BW.

1206 size 0.25 W, fixed film, chip resistors: R1: 50 Ω , RM73B2B500J; R2: 43 k Ω , RM73B2B433J; R3: 1 k Ω , RM73B2B103J.

Murata® chip capacitor: C12, C23: 0.01 μ F, GRM40X7R103K100AL.

0603 chip capacitor: C10, C21: 220 pF.

Sprague® tantalum chip capacitor: C14, C25, C26: 22 μ F, 35 V.

Kreger® ferrite bead: FB1 2743D19447.

Kemet® chip capacitor: C13, C24: 0.10 μ F, C1206C104KRAC7800.

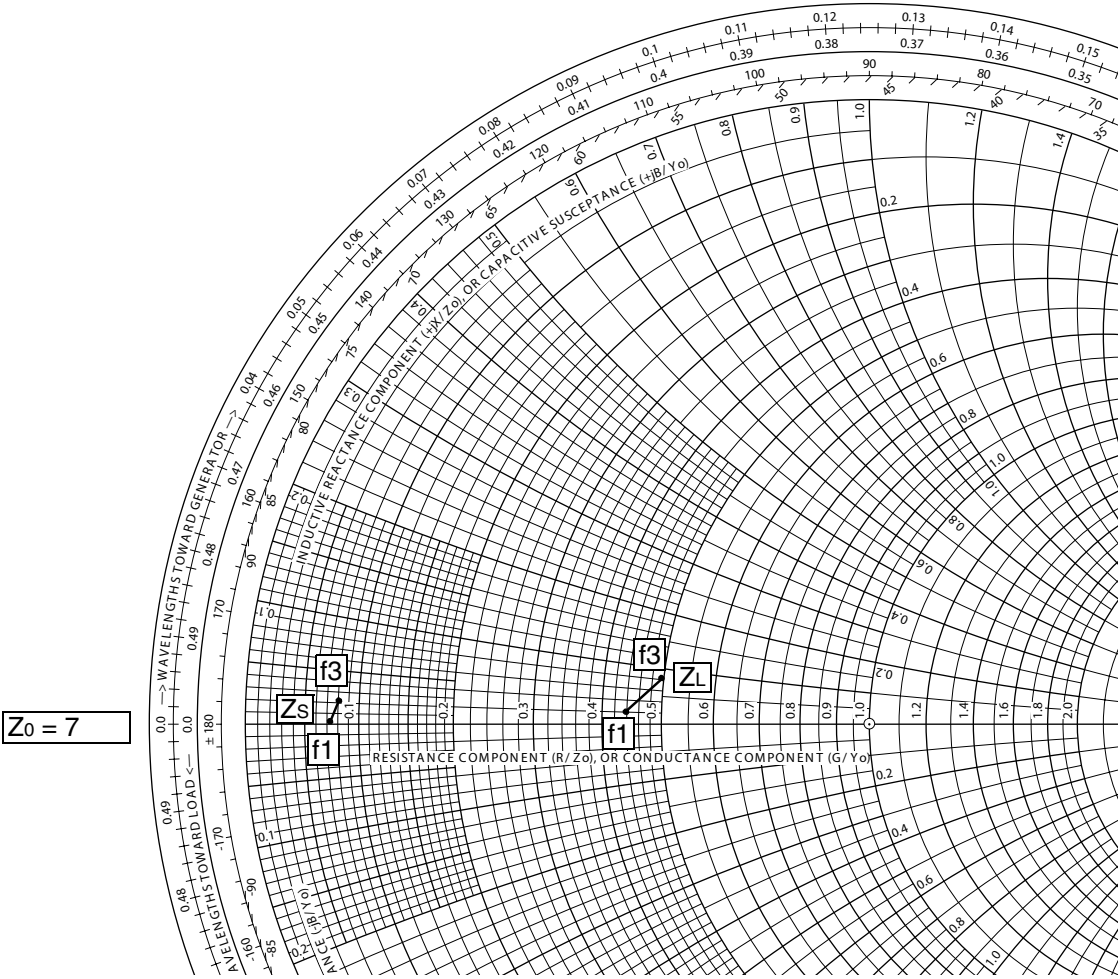
Vitramon® chip capacitor: C11, C22: 2200 pF, VJ1206Y222KXA.

Taconic® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, $\epsilon_r = 3.5$.

B. Component Layout

Figure 2. AGR09045E Test Circuit

Typical Performance Characteristics



MHz (f)	Zs (Complex Source Impedance)	ZL (Complex Optimum Load Impedance)
865 (f1)	0.479 + j0.043	3.12 + j0.070
880 (f2)	0.529 + j0.072	3.20 + j0.316
895 (f3)	0.553 + j0.101	3.32 + j0.590

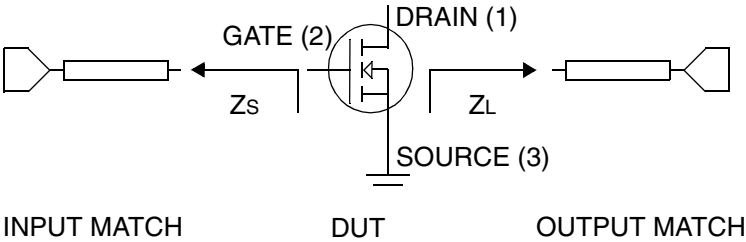


Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)

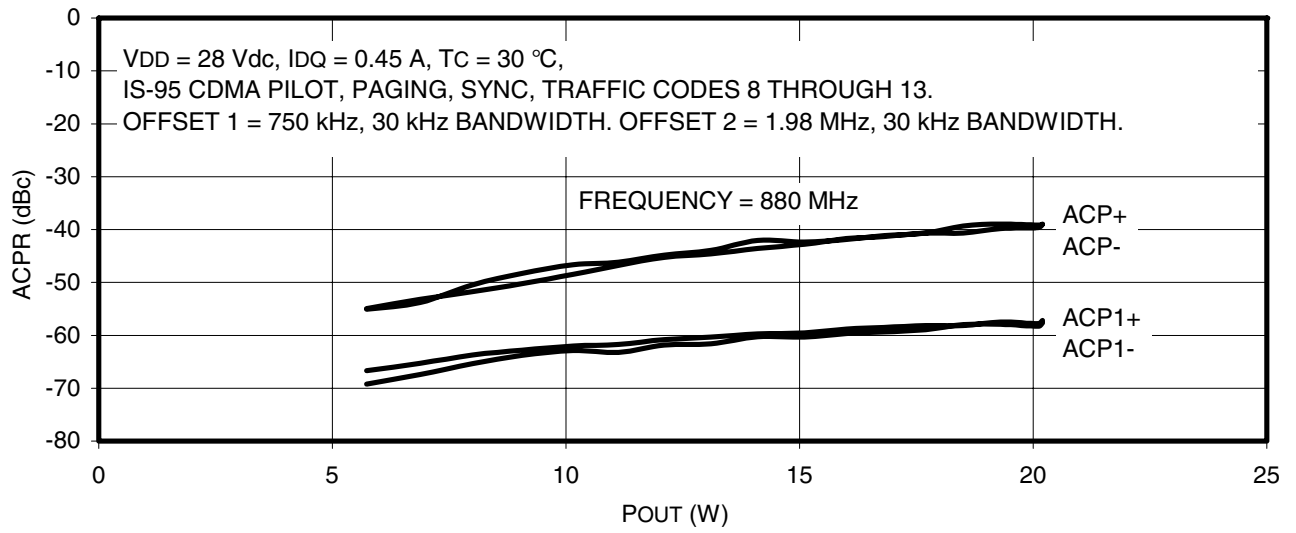


Figure 4. ACPR vs. P_{OUT}

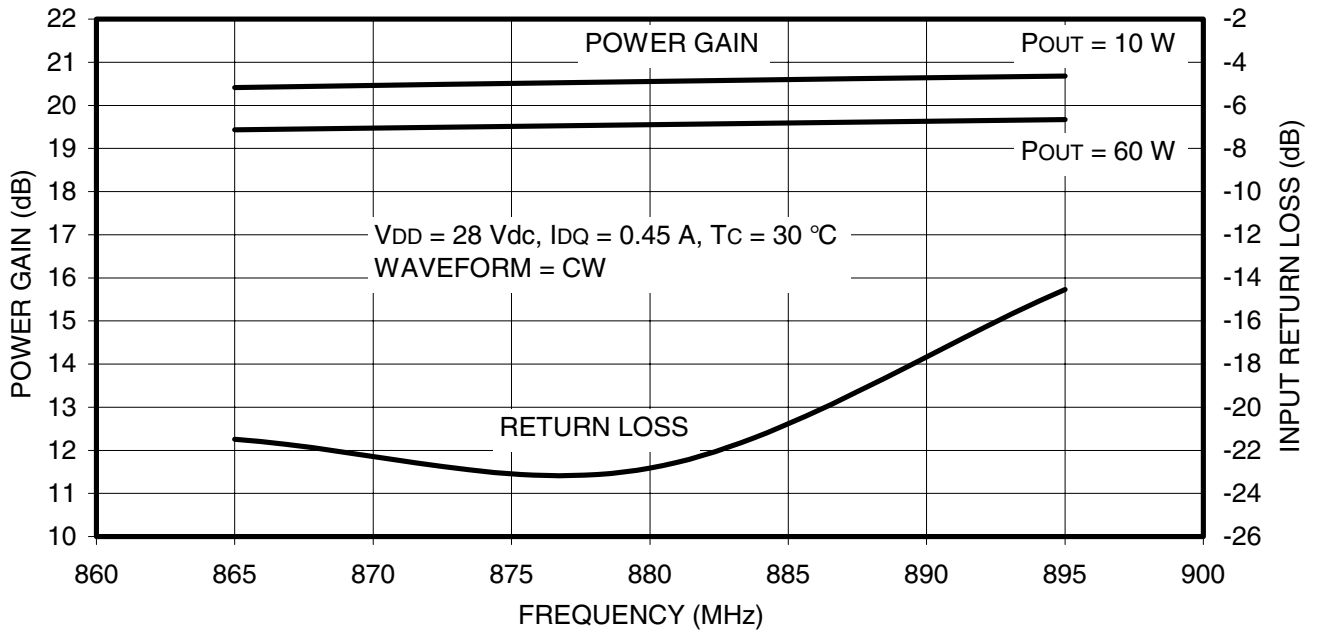


Figure 5. Power Gain and Return Loss vs. Frequency

Typical Performance Characteristics (continued)

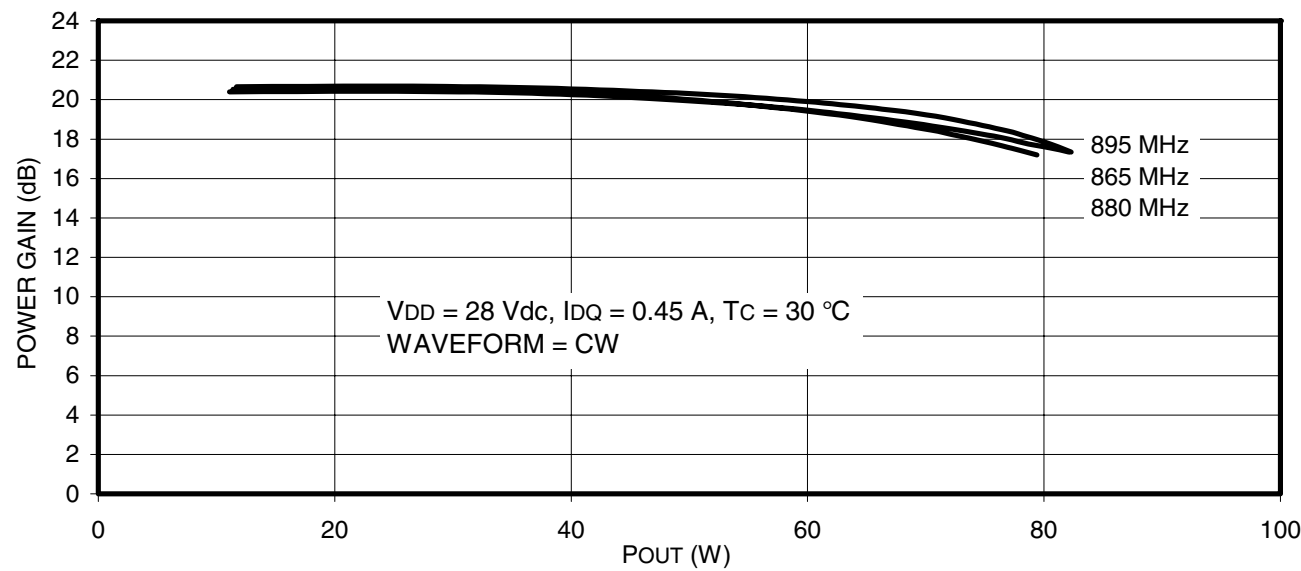


Figure 6. Power Gain vs. Power Out

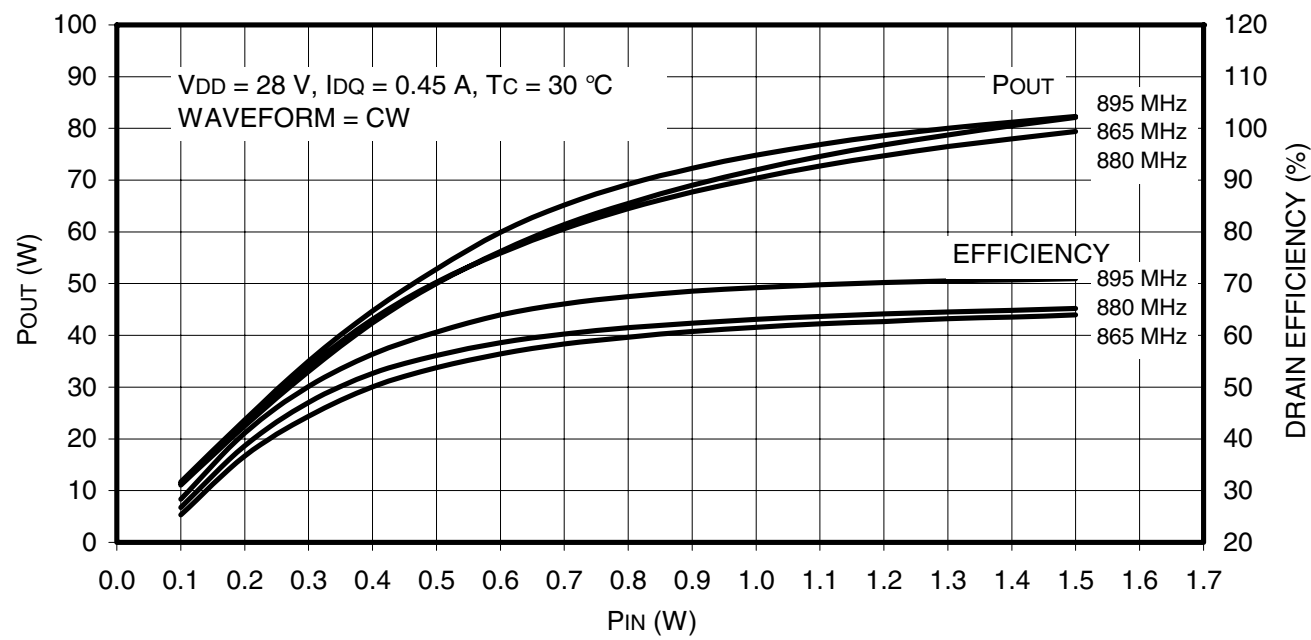
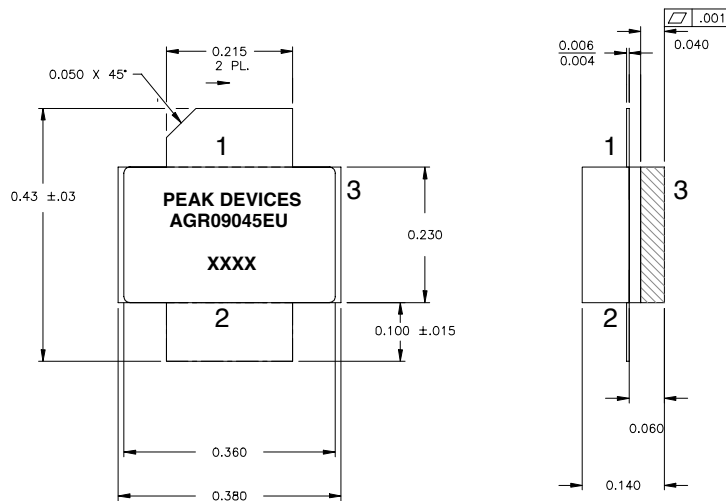


Figure 7. Power Out and Drain Efficiency vs. Input Power

Package Dimensions

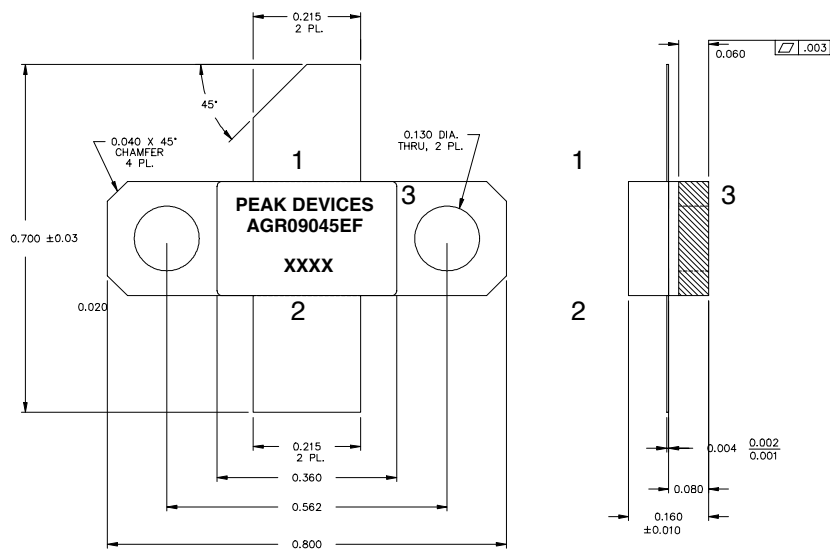
All dimensions are in inches. Tolerances are ± 0.005 in. unless specified.

AGR09045EU



PINS:
 1. DRAIN
 2. GATE
 3. SOURCE

AGR09045EF



PINS:
 1. DRAIN
 2. GATE
 3. SOURCE

XXXX - 4 Digit Trace Code

RF Power Product Information

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