TriQuint SEMICONDUCTOR

AGR19045EF
45 W, 1930 MHz—1990 MHz, PCS LDMOS RF Power Transistor

Introduction

The AGR19045EF is a 45 W, 28 V N-channel laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for personal communication service (PCS) (1930 MHz—1990 MHz), global system for mobile communication (GSM/EDGE), time-division multiple access (TDMA), and single-carrier or multicarrier class AB power amplifier applications.

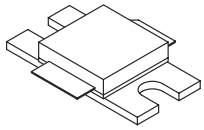


Figure 1. AGR19045EF (flanged) Package

Typical two carrier N-CDMA performance: V_{DD} = 28 V, I_{DQ} = 550 mA, f1 = 1958.75 MHz, f2 = 1961.25 MHz, IS-95 CDMA (pilot, sync, paging, traffic codes 8—13). Peak/average (P/A) = 9.72 dB at 0.01% probability on CCDF. 1.2288 MHz transmission bandwidth (BW). Adjacent channel power ratio (ACPR) measured over 30 kHz BW at f1 – 885 kHz and f2 + 885 kHz. Third-order intermodulation distortion (IM3) measured over a 1.2288 MHz BW at f1 – 2.5 MHz and f2 + 2.5 MHz:

- Output power (P_{OUT}): 9.5 W.
- Power gain: 15 dB.
- Efficiency: 24.8%.
- IM3: –34.5 dBc.
- ACPR: –49.5 dBc.

EDGE Features

Typical EDGE performance,
1990 MHz, 26 V, I_{DQ} = 400 mA:

- Output power (P_{OUT}): 18 W typical.
- Power gain: 14.5 dB.
- Efficiency: 35% typical.
- Spectral regrowth:
  - @ ±400 kHz = –62 dBc.
  - @ ±600 kHz = –74 dBc.
- Error vector magnitude (EVM) = 2.0%.

GSM Features

Typical performance over entire GSM band:

- P1dB: 50 W typical.
- Power gain @ P1dB = 14.0 dB continuous wave (CW).
- Efficiency @ P1dB = 54% typical CW.
- Return loss: –10 dB.

Device Performance Features

High-reliability, gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 1930 MHz, 45 W CW output power.

Large signal impedance parameters available.

ESD Rating*

AGR19045EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Table 1. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C	P_D	115	W
Derate Above 25 °C	—	0.67	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 3. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0 V, I_D = 200μA	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.3	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	75	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 0.4 A)	G_{FS}	—	3.0	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 130 μA)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 400 mA)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 0.4 A)	$V_{DS(ON)}$	—	0.3	—	Vdc

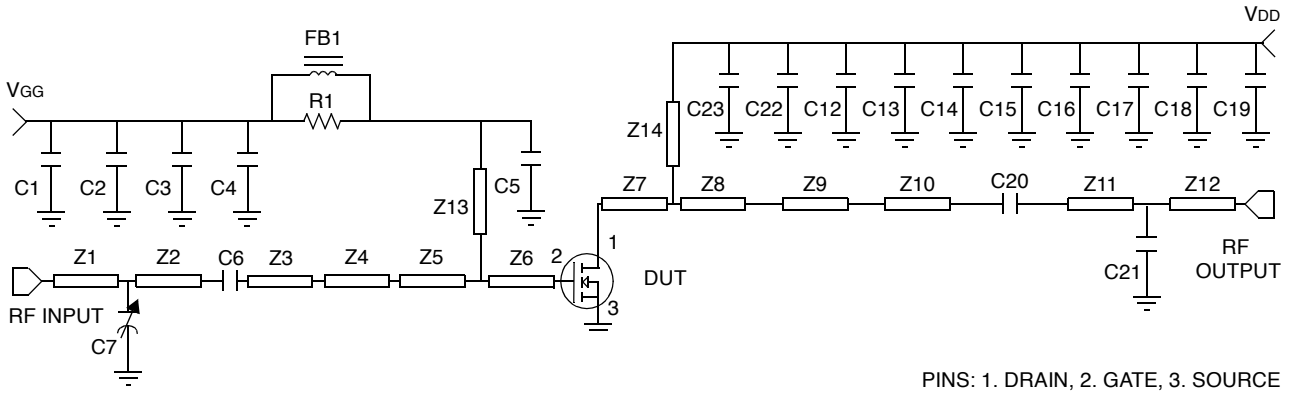
Electrical Characateristics (continued)

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. RF Characteristics

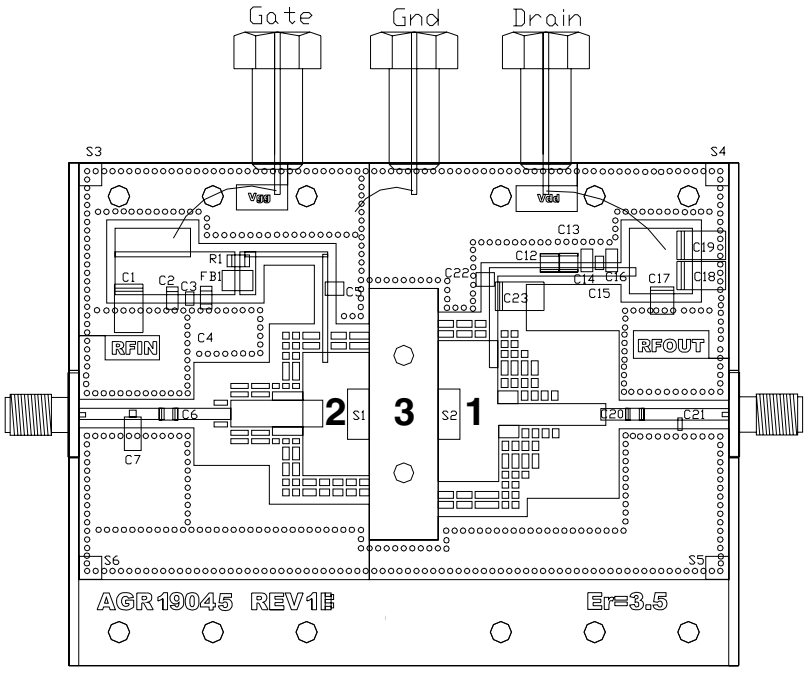
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	1.0	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{OUT} = 9 W average, 2-Carrier N-CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	G_{PS}	14.5	15.0	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{OUT} = 9 W average, 2-Carrier N-CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	η	—	24.8	—	%
Third-order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{OUT} = 9 W average, 2-Carrier N-CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; IM3 measured in a 1.228 MHz integration bandwidth centered at f1 – 2.5 MHz and f2 + 2.5 MHz, referenced to the carrier channel power)	IM3	—	–34.5	—	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{OUT} = 9 W average, 2-Carrier N-CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured in a 30 kHz integration bandwidth centered at f1 – 885 kHz and f2 + 885 kHz, referenced to the carrier channel power)	ACPR	—	–49.5	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{OUT} = 9 W average, 2-Carrier N-CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	IRL	—	–10	—	dB
Output Power at 1 dB Gain Compression (V_{DD} = 28 V, P_{OUT} = 45 W CW, f = 1990 MHz, I_{DQ} = 400 mA)	P1dB	45	50	—	W
Ruggedness (V_{DD} = 28 V, P_{OUT} = 45 W CW, I_{DQ} = 400 mA, f = 1930 MHz, VSWR = 10:1 [all phase angles])	Ψ	No degradation in output power.			

Test Circuit Illustrations for AGR19045EF



PINS: 1. DRAIN, 2. GATE, 3. SOURCE

A. Schematic



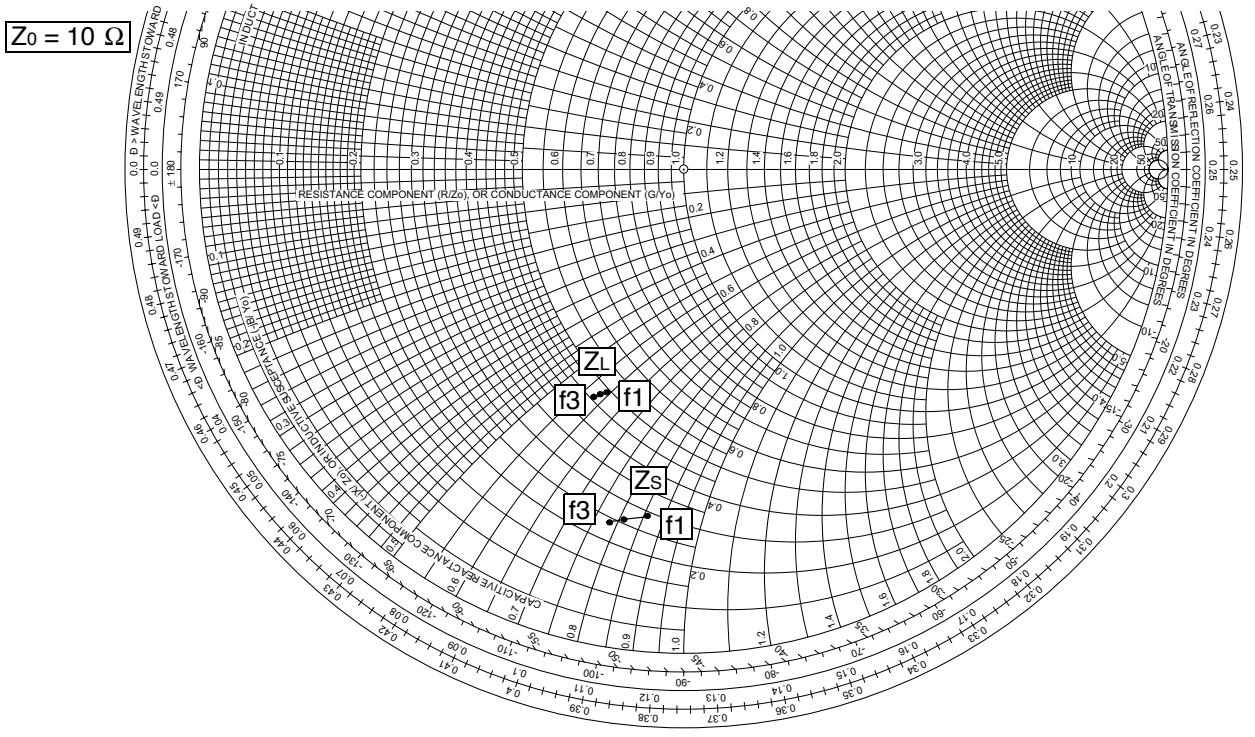
B. Component Layout

Parts List:

- Microstrip line: Z1, 0.320 in. x 0.067 in.; Z2, 0.185 in. x 0.067 in.; Z3, 0.345 in. x 0.067 in.; Z4, 0.250 in. x 0.160 in.; Z5, 0.180 in. x 0.260 in.; Z6, 0.400 in. x 0.735 in.; Z7, 0.355 in. x 0.840 in.; Z8, 0.120 in. x 0.280 in.; Z9, 0.525 in. x 0.130 in.; Z10, 0.145 in. x 0.067 in.; Z11, 0.245 in. x 0.067 in.; Z12, 0.290 in. x 0.067 in.; Z13, 0.370 in. x 0.030 in.; Z14, 0.280 in. x 0.050 in.
- *ATC*® B case chip capacitors: C5, C12, C22: 8.2 pF; C6, C20: 10 pF; C13: 1000 pF.
- *ATC* S case chip capacitor: C21: 0.2 pF
- *Kemet*® B case chip capacitors: C2, C16: 0.1 μF CDR33BX104AKWS. Tantalum capacitor: C17, 1 μF, 50 V, T491C.
- *Vitramon*® 1206: C4, C14: 22000 μF.
- *Johanson Giga-Trim*® variable capacitor C7: 0.4 pF—2.5 pF.
- *Murata*® 0805: C3, C15: 0.01 μF, GRM40X7R103K100AL.
- *Sprague*® tantalum surface-mount chip capacitor: C1, C18, C19, C23: 22 μF, 35 V.
- *Fair-Rite*® ferrite bead: FB1: 2743019447.
- Fixed film chip resistor: R1: 12 Ω, 0.25 W, 0.08 x 0.13.
- PCB etched circuit boards.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, εr = 3.5.

Figure 2. AGR19045EF Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
1930 (f1)	2.79 – j8.63	4.94 – j6.00
1960 (f2)	2.64 – j8.20	4.82 – j5.91
1990 (f3)	2.38 – j7.78	4.47 – j5.79

Note: ZL was chosen based on trade-offs between gain, output power, drain efficiency, and intermodulation distortion.

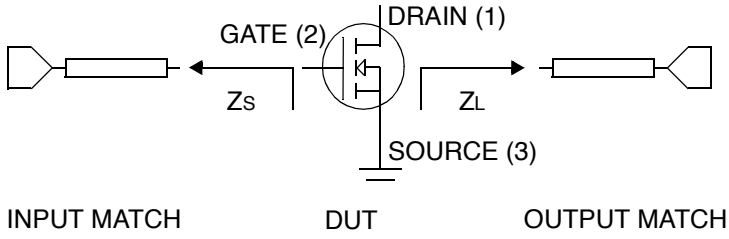
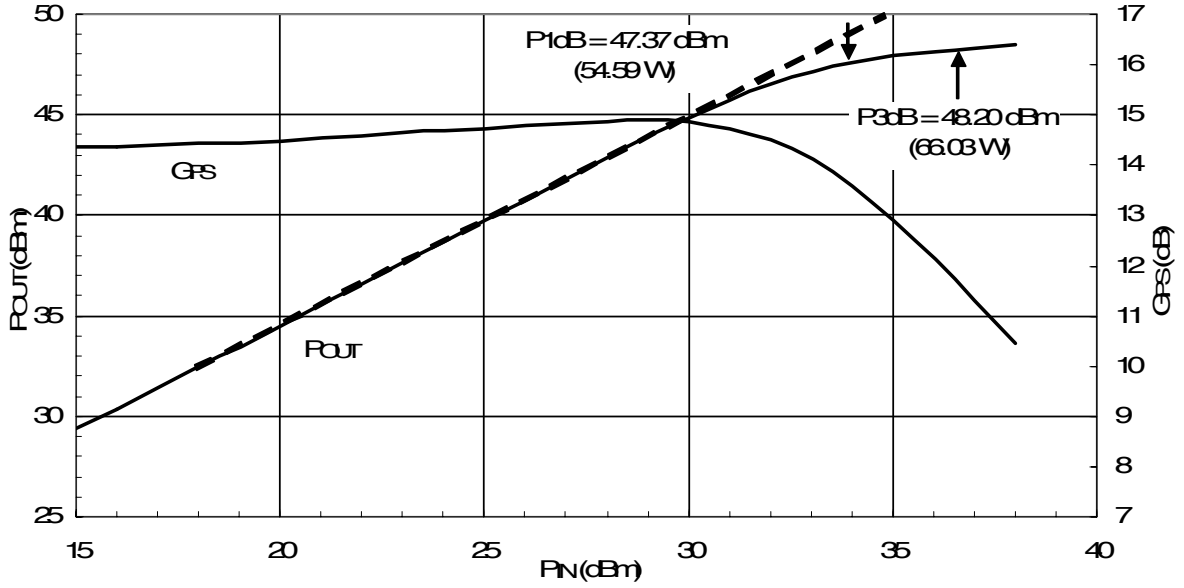


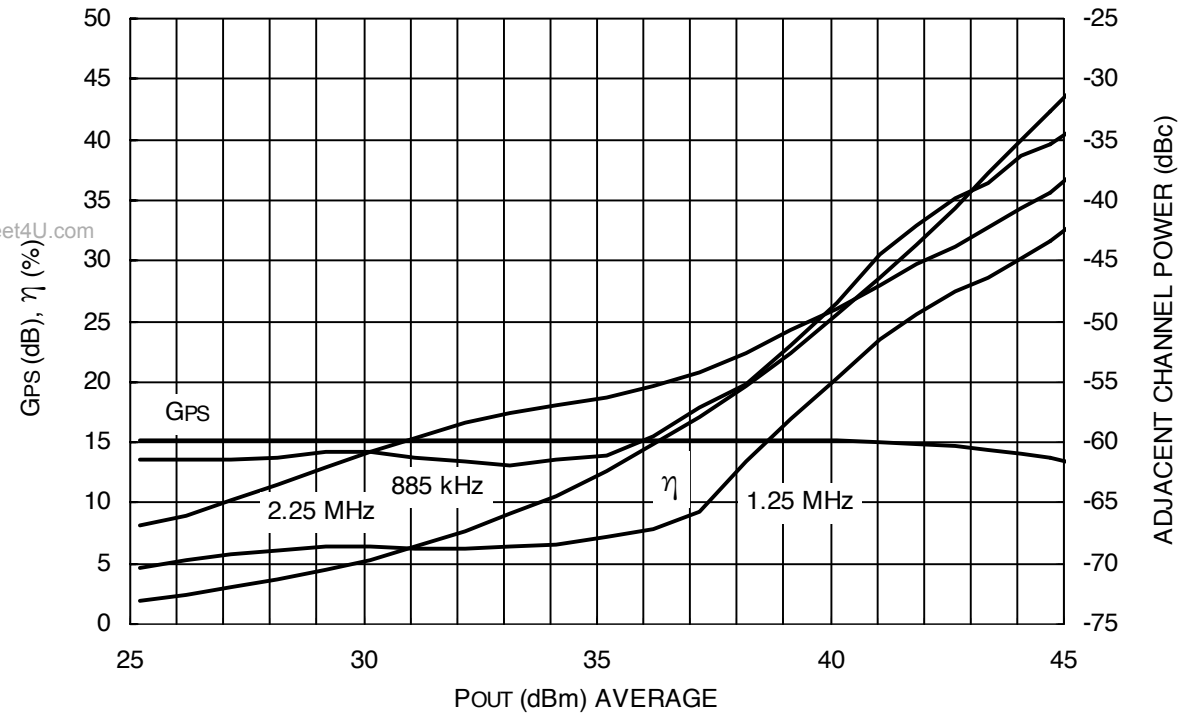
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 400 mA, CW center frequency = 1960 MHz.

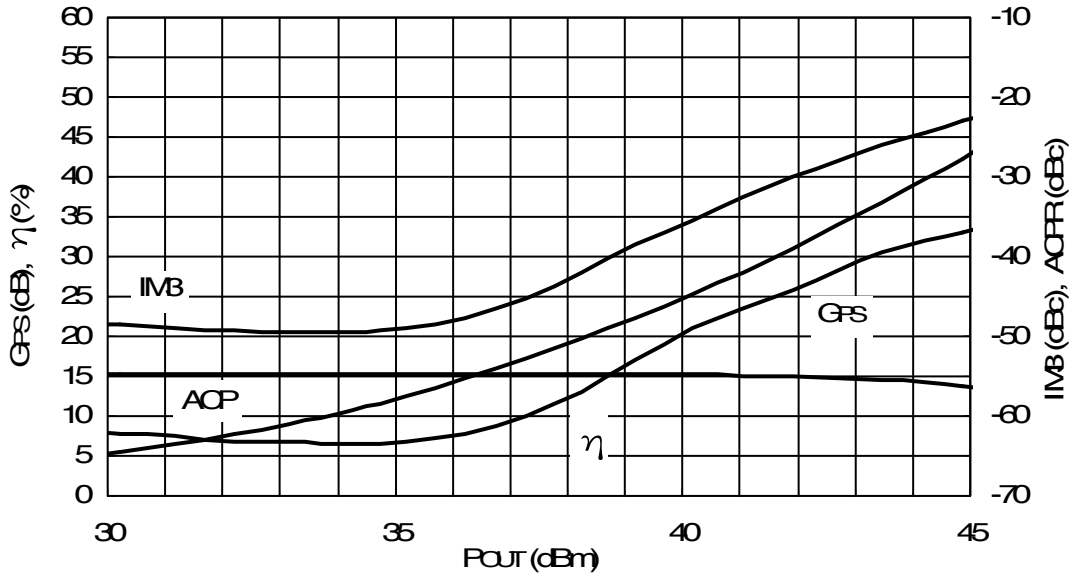
Figure 4. CW P_{OUT} vs. P_{IN}



Test Conditions:
V_{DD} = 28 V, I_{DQ} = 550 mA, f1 = 1960 MHz, N-CDMA, 2.5 MHz @ 1.2288 MHz bandwidth. Peak/Average = 9.72 dB @ 0.01% probability (CCDF). Channel spacing (bandwidth): 885 kHz (30 kHz), 1.25 MHz (12.5 kHz), 2.25 MHz (1 MHz).

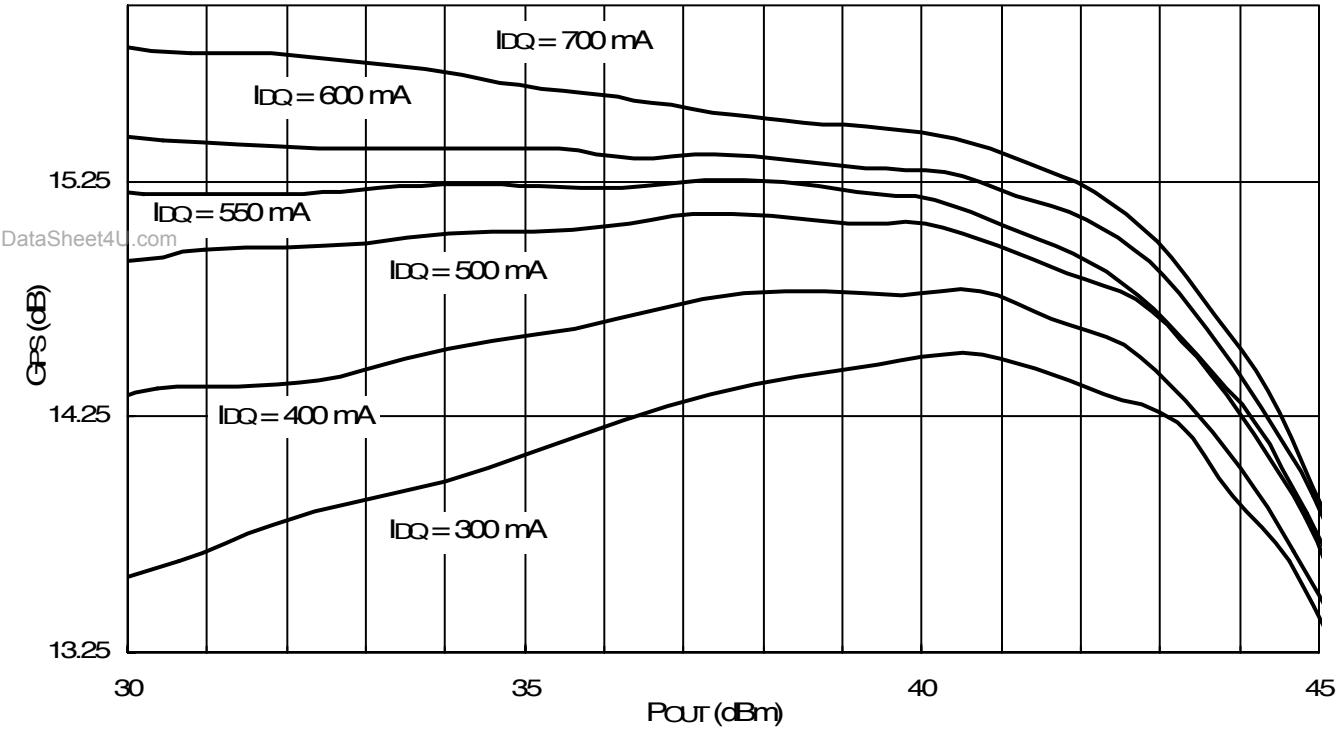
Figure 5. N-CDMA ACPR, Power Gain, and Drain Efficiency vs. Power

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 V, I_{DQ} = 550 mA, f1 = 1958.75 MHz, f2 = 1961.25 MHz. 2 x N-CDMA, 2.5 MHz @ 1.2288 MHz bandwidth. Peak/average = 9.72 dB @ 0.01% probability (CCDF). Channel spacing (bandwidth); ACPR: 885 kHz (30 kHz), IM3: 2.5 MHz (1.2288 MHz).

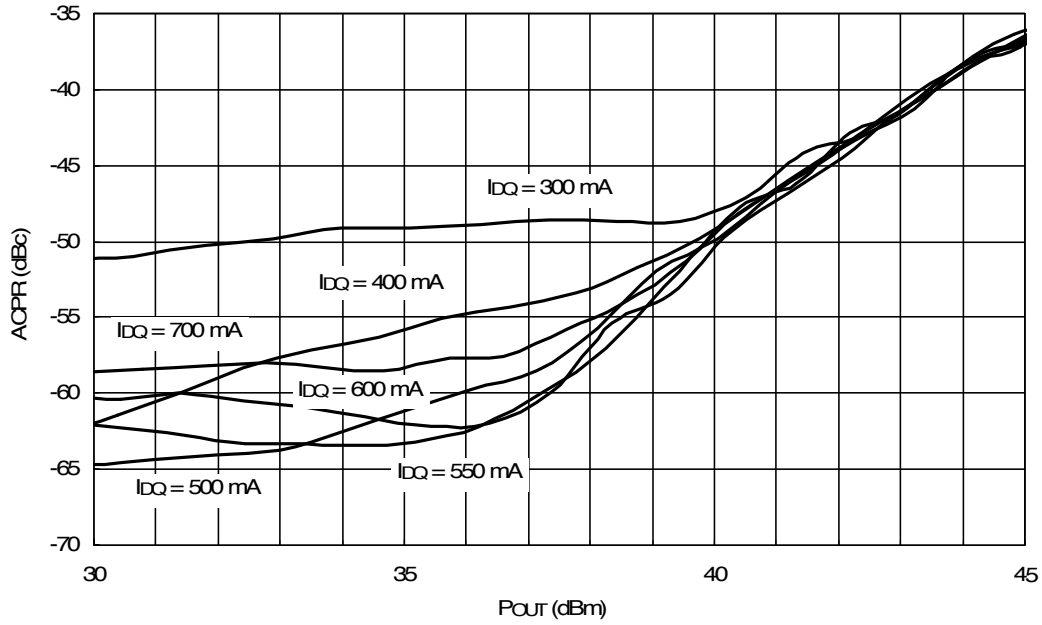
Figure 6. 2-Carrier N-CDMA ACPR, IM3, Power Gain, and Drain Efficiency vs. Power



Test Conditions:
V_{DD} = 28 V_{DC}, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2-carrier N-CDMA measurement.

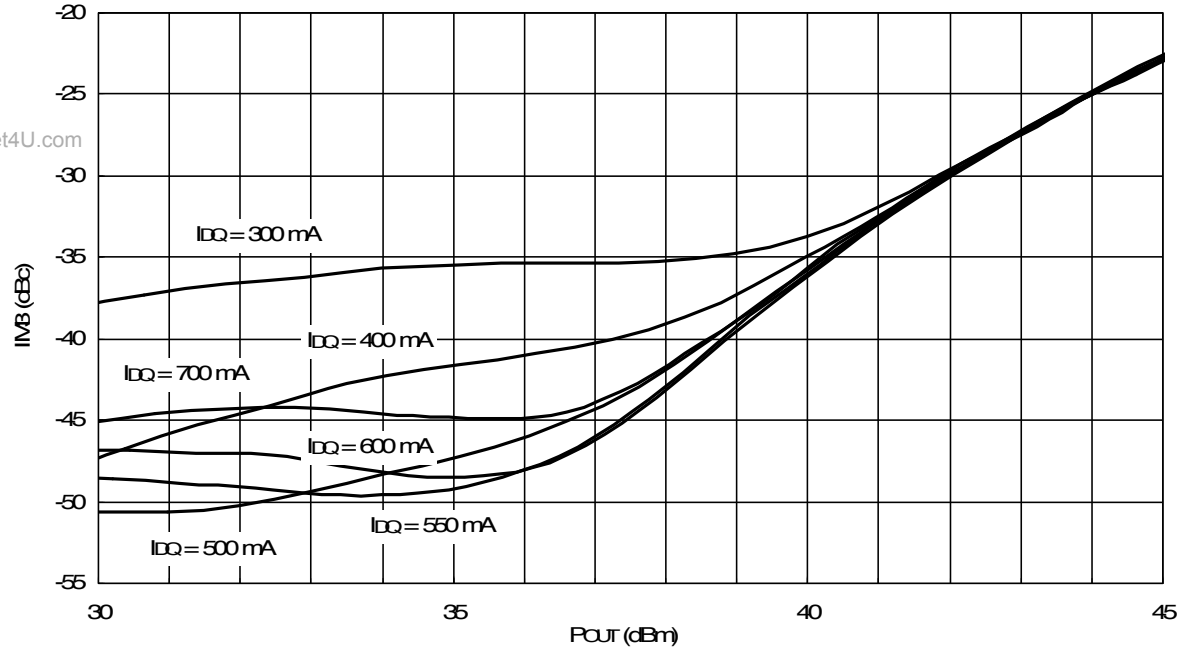
Figure 7. 2-Carrier N-CDMA, G_{PS} vs. P_{OUT}

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 V_{DC}, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2-carrier N-CDMA measurement.

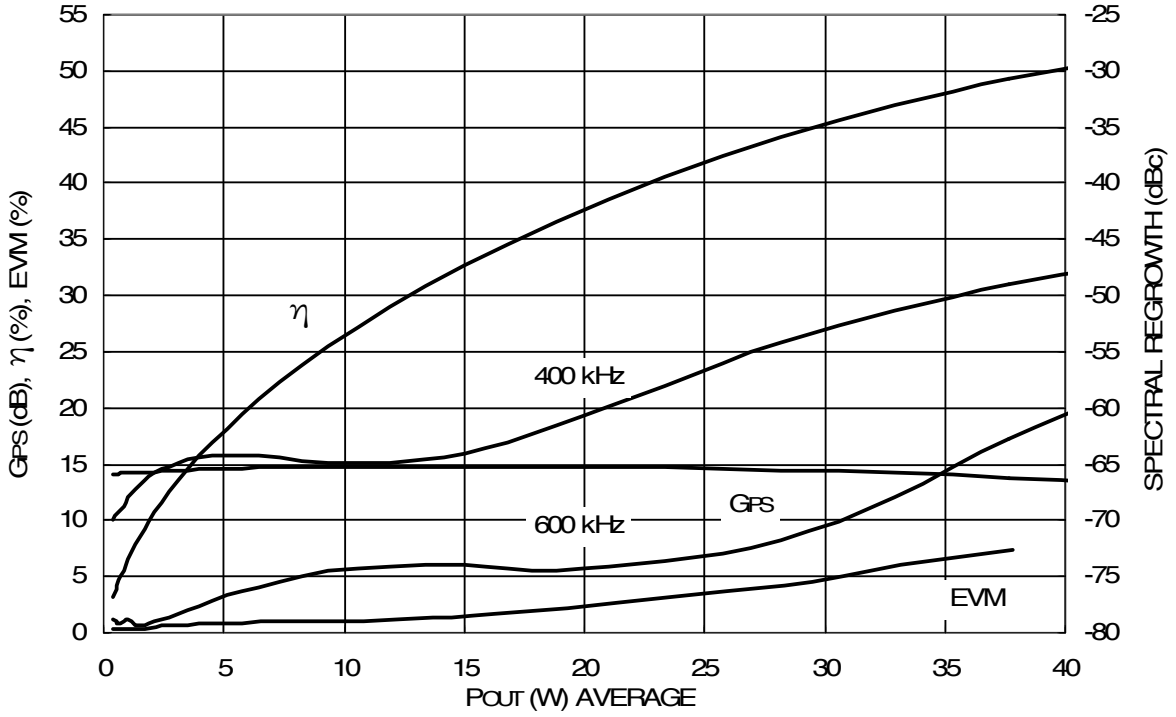
Figure 8. ACPR vs. P_{OUT}



Test Conditions:
V_{DD} = 28 V_{DC}, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2-carrier N-CDMA measurement.

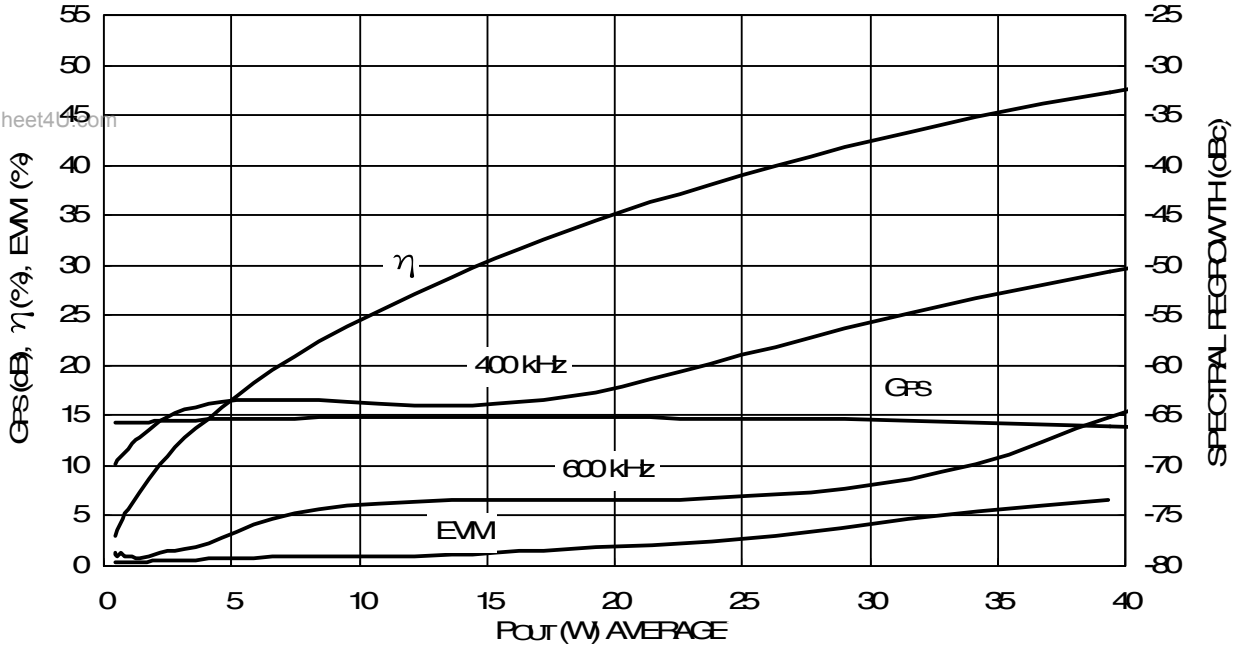
Figure 9. IM3 vs. P_{OUT}

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = 1960 MHz, modulation = GSM/EDGE.

Figure 10. GSM/EDGE Power Gain, Drain Efficiency, Spectral Regrowth, and EVM Average vs. P_{OUT}



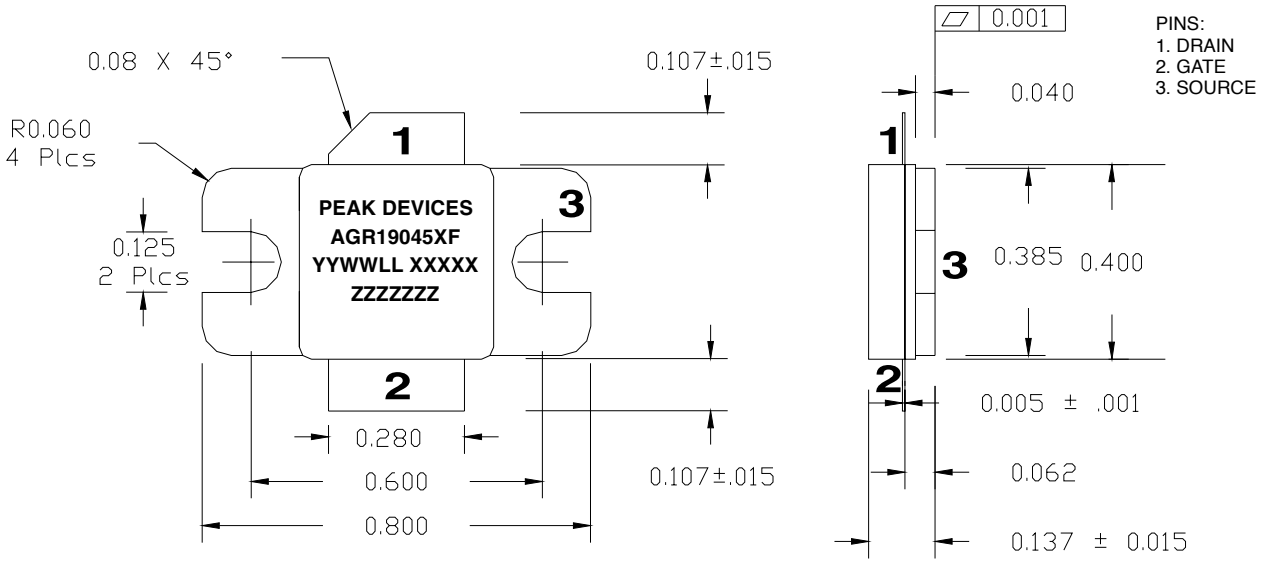
Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 400 mA, f = 1960 MHz, modulation = GSM/EDGE.

Figure 11. GSM/EDGE Power Gain, Drain Efficiency, Spectral Regrowth, and EVM Average vs. P_{OUT}

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR19045EF



Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.