TriQuint SEMICONDUCTOR

AGR19060E
60 W, 1930 MHz—1990 MHz, PCS LDMOS RF Power Transistor

Introduction

The AGR19060E is a 60 W, 28 V N-channel laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for personal communication service (PCS) (1930 MHz—1990 MHz), global system for mobile communication (GSM/EDGE), time-division multiple access (TDMA), and single-carrier or multicarrier class AB power amplifier applications.

AGR19060EU (unflanged) **AGR19060EF (flanged)**

Figure 1. Available Packages

N-CDMA Features

Typical 2 carrier N-CDMA performance: V_{DD} = 28 V, I_{DQ} = 700 mA, f1 = 1958.75 MHz, f2 = 1961.25 MHz, IS-95 CDMA (pilot, sync, paging, traffic codes 8—13). Peak/average (P/A) = 9.72 dB at 0.01% probability on CCDF. 1.2288 MHz transmission bandwidth (BW). Adjacent channel power ratio (ACPR) measured over 30 kHz BW at f1 – 885 kHz and f2 + 885 kHz. Third-order intermodulation distortion (IM3) measured over a 1.2288 MHz BW at f1 – 2.5 MHz and f2 + 2.5 MHz.
— Output power (P_{OUT}): 12 W.
— Power gain: 15.5 dB.
— Efficiency: 23.5%.
— IM3: –36 dBc.
— ACPR: –50.5 dBc.

EDGE Features

Typical EDGE performance (1960 MHz, 26 V, I_{DQ} = 500 mA):
— Output power (P_{OUT}): 25 W.
— Power gain: 15.3 dB.
— Efficiency: 37%.
— Modulation spectrum:
@ ±400 kHz = –61.0 dBc.
@ ±600 kHz = –74.0 dBc.
— Error vector magnitude (EVM) = 2.5%.

GSM Features

Typical performance over entire GSM band:
— P1dB: 60 W typical.
— Continuous wave (CW) power gain: @ P1dB = 14.5 dB.
— CW efficiency @ P1dB = 53% typical.
— Return loss: –12 dB.

Device Performance Features

High-reliability, gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 1930 MHz, 60 W CW output power.

Large signal impedance parameters available.

ESD Rating*

AGR19060E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Table 1. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case:			
AGR19060EU	$R_{\theta JC}$	1.00	°C/W
AGR19060EF	$R_{\theta JC}$	1.00	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C:			
AGR19060EU	P_D	175	W
AGR19060EF	P_D	175	W
Derate Above 25 °C:			
AGR19060EU	—	1.00	W/°C
AGR19060EF	—	1.00	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 3. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0 V, I_D = 300 μA	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.8	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	100	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 0.45 A)	G_{FS}	—	4.0	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 180 μA)	$V_{GS(th)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 500 mA)	$V_{GS(Q)}$	—	3.6	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 0.45 A)	$V_{DS(on)}$	—	0.08	—	Vdc

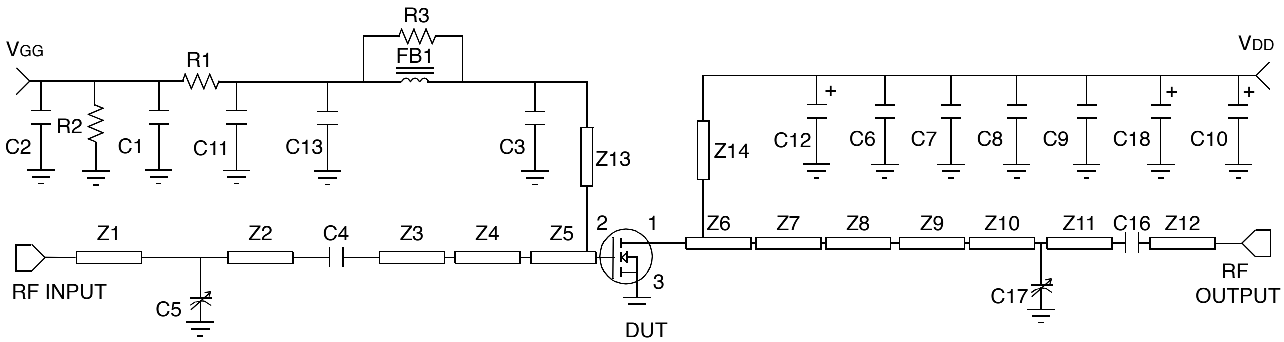
Electrical Characteristics (continued)

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

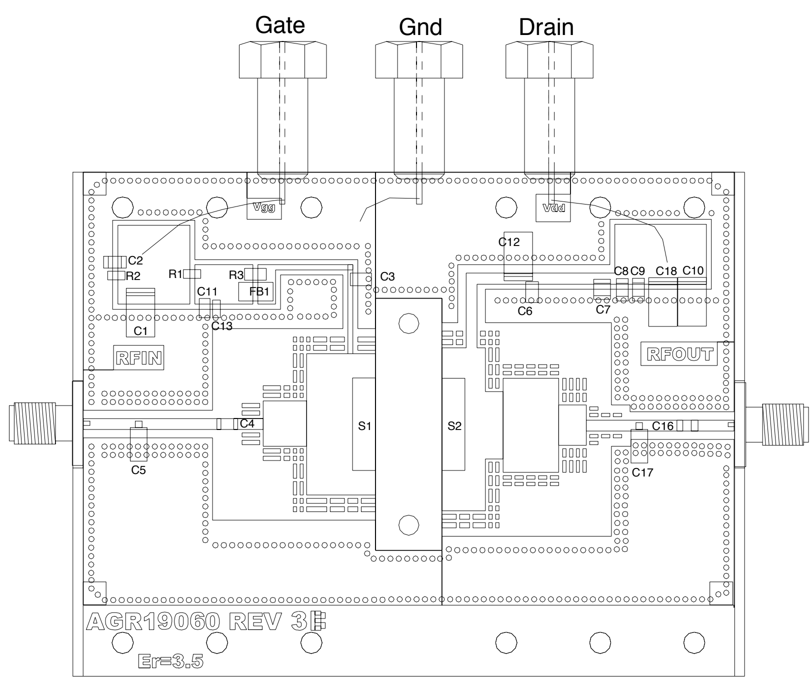
Table 4. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz) (Part is internally matched both on input and output.)	C_{RSS}	—	1.3	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{OUT} = 12 W average, 2-Carrier N-CDMA, I_{DQ} = 700 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	G_{PS}	14.5	15.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{OUT} = 12 W average, 2-Carrier N-CDMA, I_{DQ} = 700 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	η	—	23.5	—	%
Third-order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{OUT} = 12 W average, 2-Carrier N-CDMA, I_{DQ} = 700 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; IM3 measured in a 1.2288 MHz integration BW centered at f1 – 2.5 MHz and f2 + 2.5 MHz, referenced to the carrier channel power)	IM3	—	–36	—	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{OUT} = 12 W average, 2-Carrier N-CDMA, I_{DQ} = 700 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured in a 1.2288 MHz integration BW centered at f1 – 2.5 MHz and f2 + 2.5 MHz, referenced to the carrier channel power)	ACPR	—	–50.5	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{OUT} = 12 W average, 2-Carrier N-CDMA, I_{DQ} = 700 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	IRL	—	–12	—	dB
Output Power at 1 dB Gain Compression (V_{DD} = 28 V, P_{OUT} = 60 W CW, f = 1990 MHz, I_{DQ} = 500 mA)	P1dB	60	70	—	W
Ruggedness (V_{DD} = 28 V, P_{OUT} = 60 W CW, I_{DQ} = 350 mA, f = 1930 MHz, VSWR = 10:1 [all phase angles])	Ψ	No degradation in output power.			

Test Circuit Illustrations for AGR19060E



A. Schematic



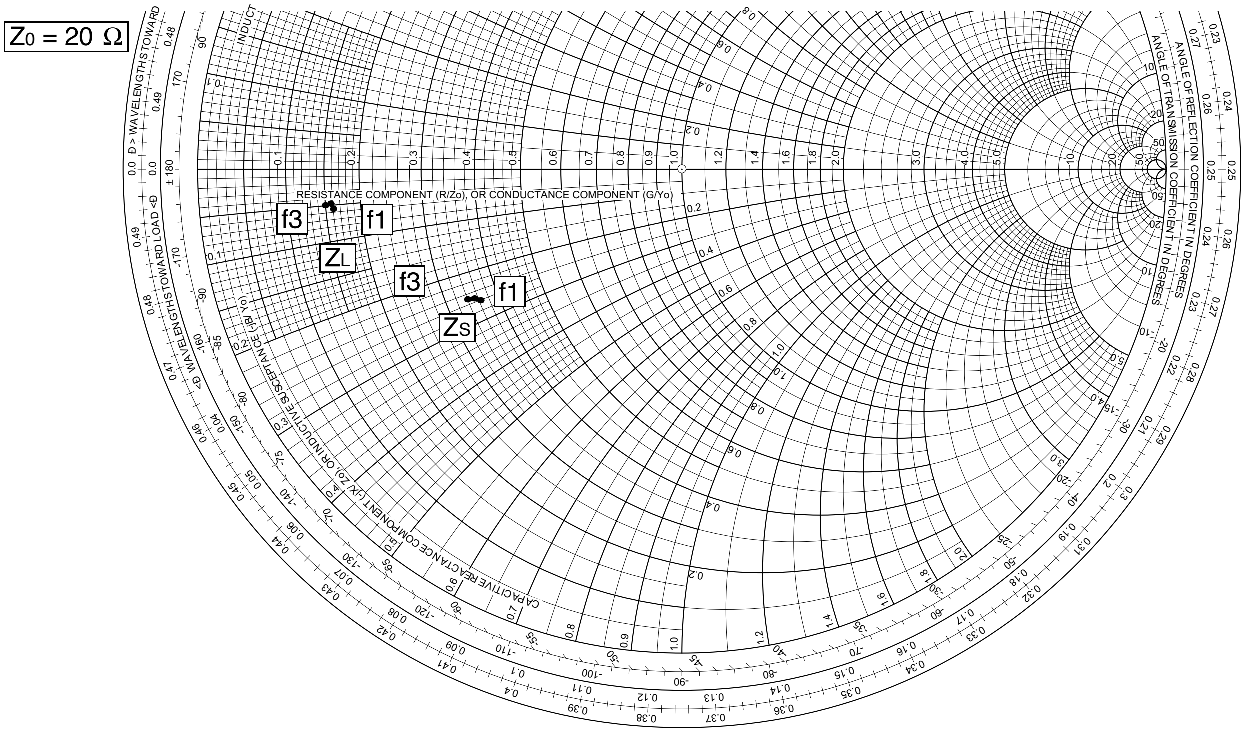
B. Component Layout

Parts List:

- Microstrip line: Z1 0.330 in. x 0.065 in.; Z2 0.470 in. x 0.065 in.; Z3 0.175 in. x 0.065 in.; Z4 0.260 in. x 0.270 in.; Z5 0.410 in. x 0.840 in.; Z6 0.260 in. x 0.970 in.; Z7 0.105 in. x 0.400 in.; Z8 0.330 in. x 0.560 in.; Z9 0.165 in. x 0.240 in.; Z10 0.315 in. x 0.065 in.; Z11 0.260 in. x 0.065 in.; Z12 0.255 in. x 0.065 in.; Z13 0.440 in. x 0.030 in.; Z14 0.695 in. x 0.050 in.
- *ATC*® B case chip capacitors: C3, C6: 8.2 pF, 100B8R2JCA500X; C4, C16: 10 pF, 100B100JCA500X; C7: 1000 pF, 100B102JCA500X.
- *Kemet*® B case chip capacitors: C9, C11: 0.10 μF, CDR33BX104AKWS.
- *Johanson Giga-Trim*® variable capacitors: C5, C17: 0.4 pF—2.5 pF.
- *Vitramon*® 1206: C2, C8: 22000 pF.
- *Murata*® 0805: C13: 0.01 μF, GRM40X7R103K100AL.
- *Fair-Rite*® ferrite bead: FB1, #2743019447.
- *Sprague*® tantalum, SMT, 35 V: C1, C10, C12: 22 μF; C18: 10 μF.
- Fixed film chip resistors, 0.25 W, 0.08 x 0.13: R1 510 Ω; R2 560 kΩ; R3 4.7 Ω.
- PCB etched circuit boards.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, ε_r = 3.5.

Figure 2. AGR19060E Test Circuit Schematic

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
1930 (f1)	7.24 – j5.20	3.23 – j1.07
1960 (f2)	7.04 – j5.00	3.06 – j0.99
1990 (f3)	6.87 – j4.96	2.97 – j1.00

Note: ZL was chosen based on trade-offs between gain, output power, drain efficiency, and intermodulation distortion.

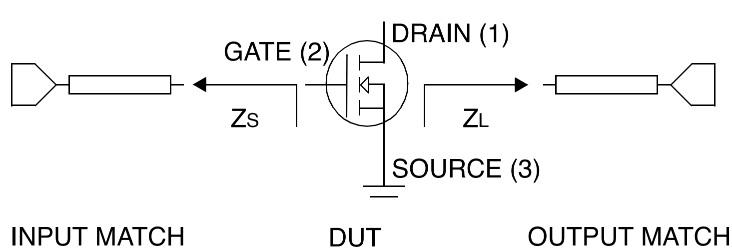
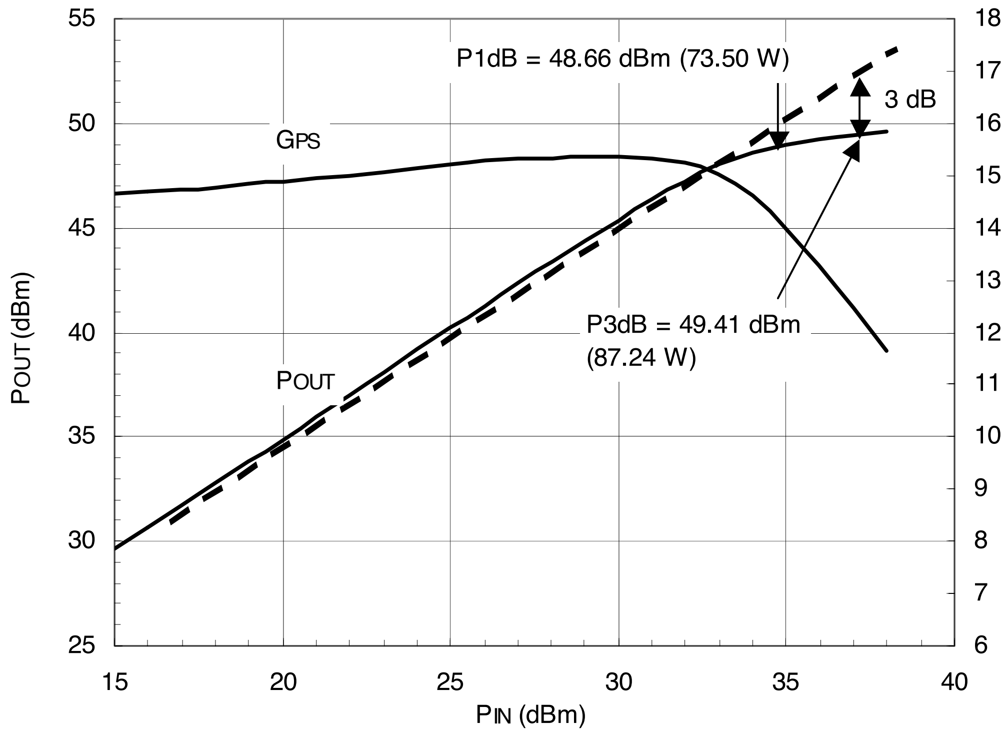


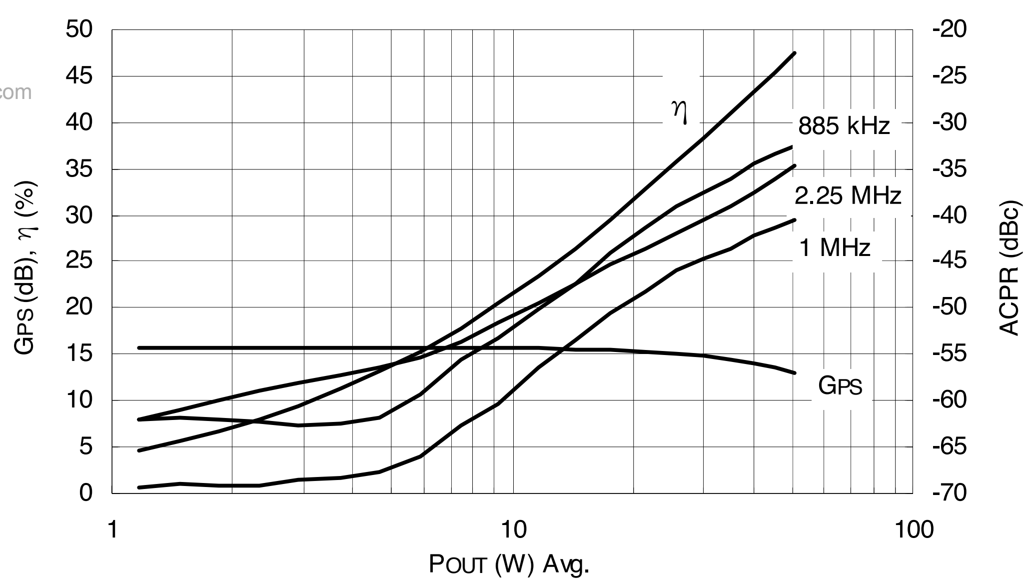
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 500 mA, CW, center frequency = 1960 MHz.

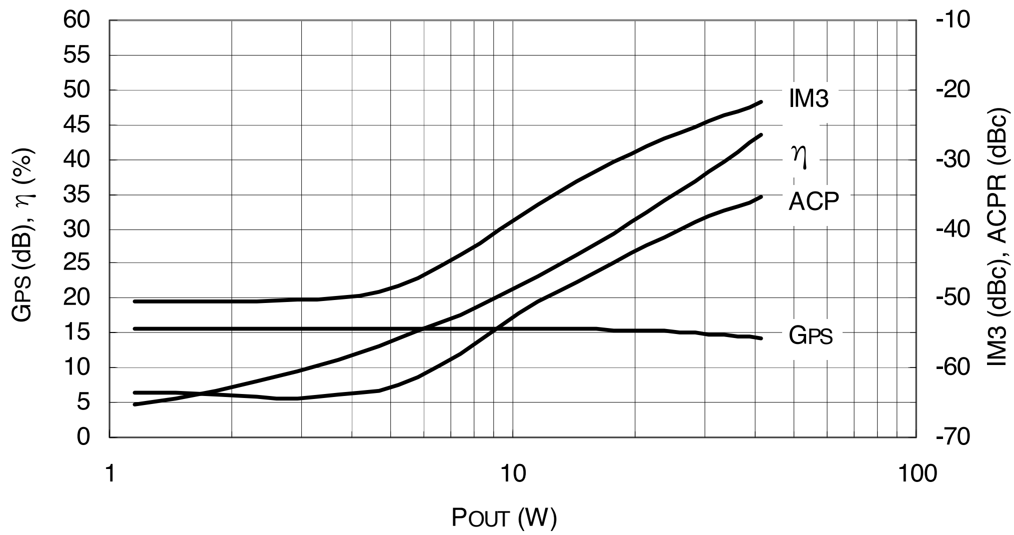
Figure 4. CW P_{OUT} vs. P_{IN}



Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 700 mA, f = 1960 MHz, N-CDMA, 2.5 MHz @ 1.2288 MHz BW, P/A = 9.72 dB @ 0.01% probability (CCDF), channel spacing (BW) 885 kHz (30 kHz), 1.25 MHz (12.5 kHz), 2.25 MHz (1 MHz).

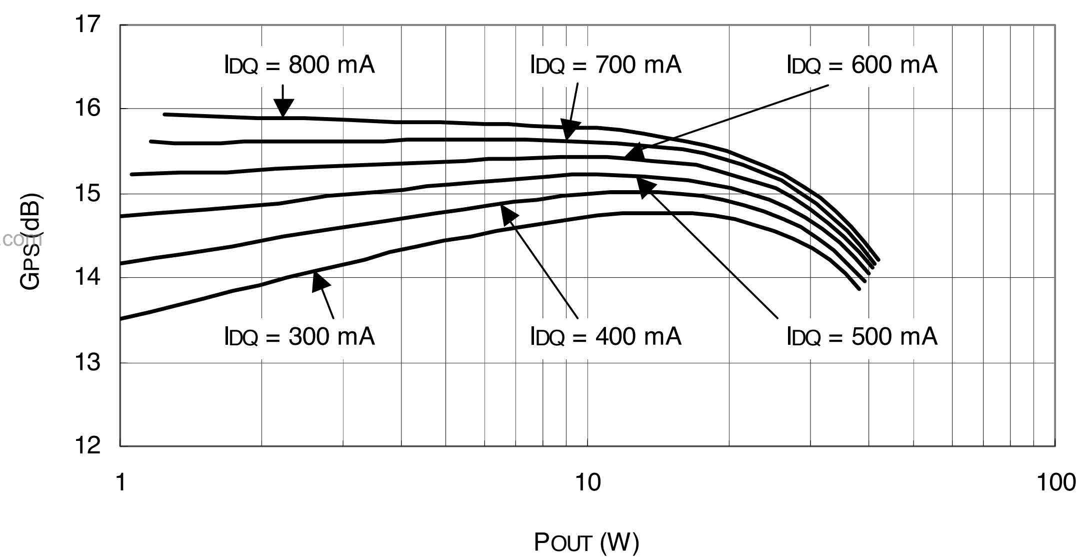
Figure 5. N-CDMA ACPR, Power Gain, and Drain Efficiency vs. P_{OUT}

Typical Performance Characteristics (continued)



Test Conditions:
VDD = 28 Vdc, IDQ = 700 mA, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2 x N-CDMA, 2.5 MHz @ 1.2288 MHz BW, P/A = 9.72 dB @ 0.01% probability (CCDF), channel spacing (BW) ACPR: 885 kHz (30 kHz), IM3: 2.5 MHz (1.2288 MHz).

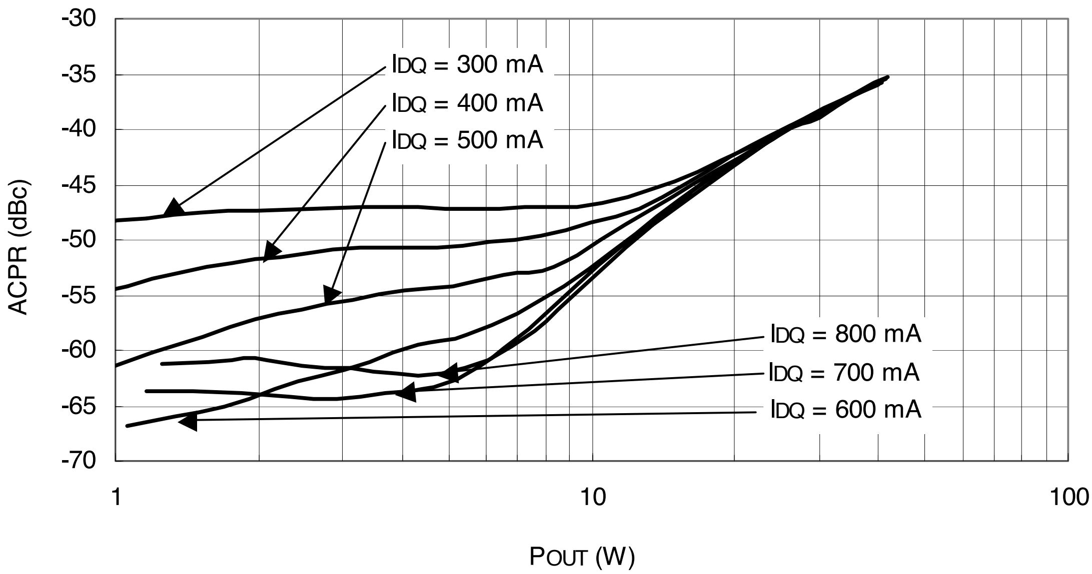
Figure 6. 2-Carrier N-CDMA ACPR, IM3, Power Gain, and Drain Efficiency vs. POUT



Test Conditions:
VDD = 28 Vdc, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2 carrier N-CDMA measurement.

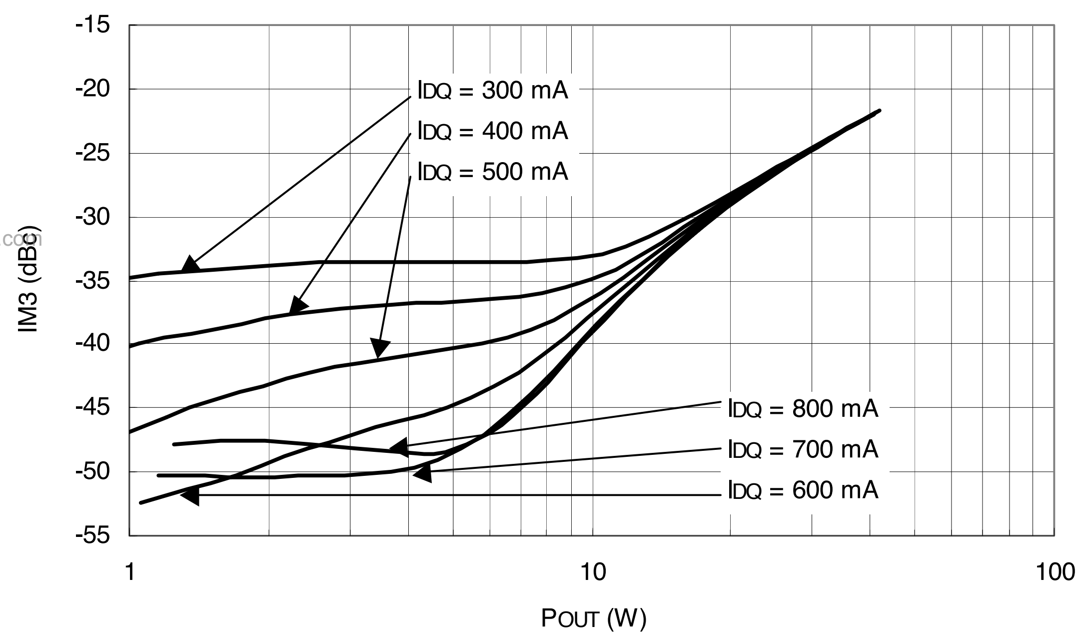
Figure 7. 2-Carrier N-CDMA Power Gain vs. POUT

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 Vdc, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2 carrier N-CDMA measurement.

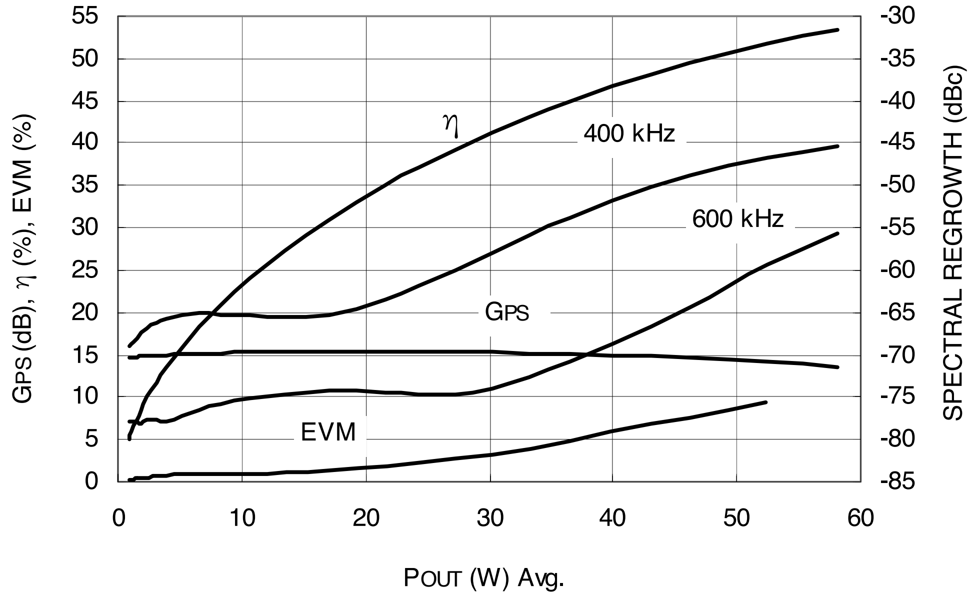
Figure 8. ACPR vs. P_{OUT}



Test Conditions:
V_{DD} = 28 Vdc, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2 carrier N-CDMA measurement.

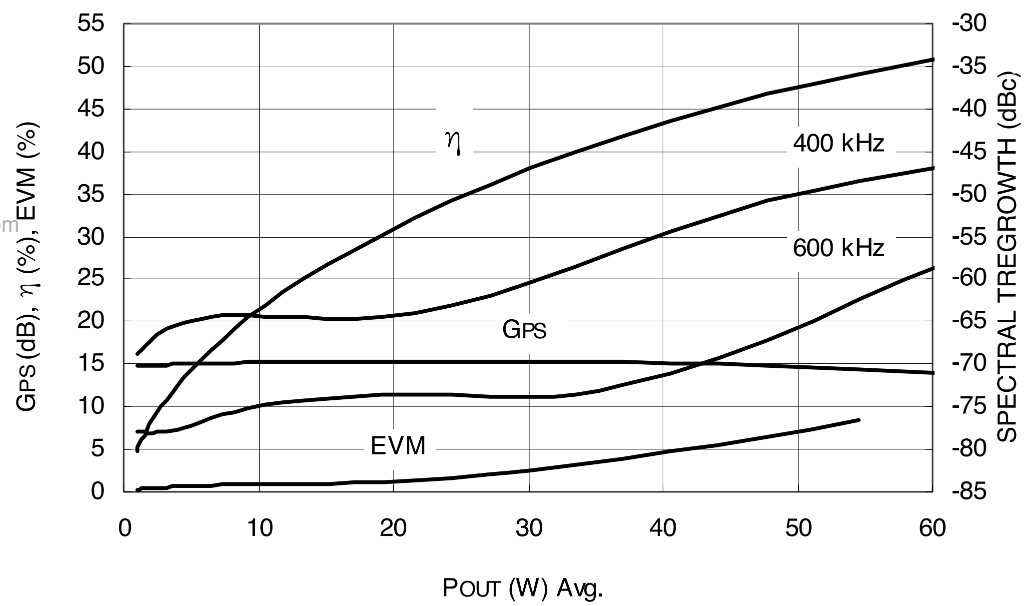
Figure 9. IM3 vs. P_{OUT}

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1960 MHz, modulation = GSM/EDGE.

Figure 10. GSM/EDGE Power Gain, Drain Efficiency, Spectral Regrowth, and EVM vs. P_{OUT}



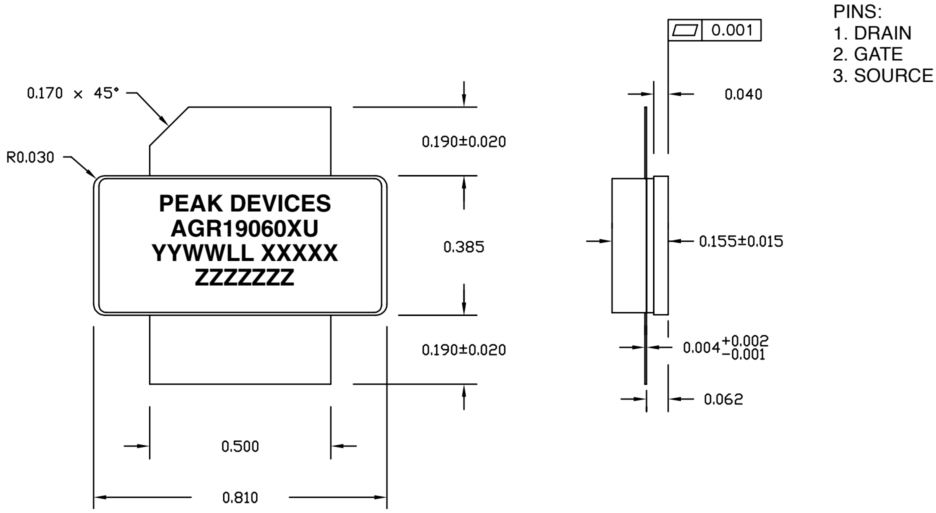
Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 1960 MHz, modulation = GSM/EDGE.

Figure 11. GSM/EDGE Power Gain, Drain Efficiency, Spectral Regrowth, and EVM vs. P_{OUT}

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR19060EU



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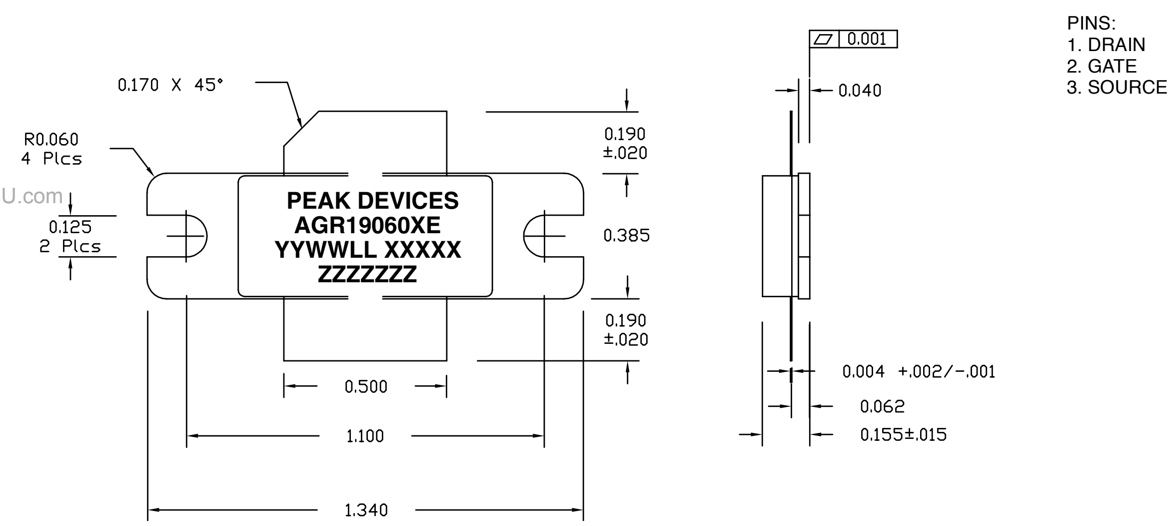

Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; BK = Bangkok, Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.