TriQuint SEMICONDUCTOR

AGR19180EF
180 W, 1930 MHz—1990 MHz, PCS LDMOS RF Power Transistor

Introduction

The AGR19180EF is a 180 W, 28 V N-channel laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for personal communication service (PCS) (1930 MHz—1990 MHz), code division multiple access (CDMA), global system for mobile communication (GSM/EDGE), time division multiple access (TDMA), and single-carrier or multicarrier class AB power amplifier applications.

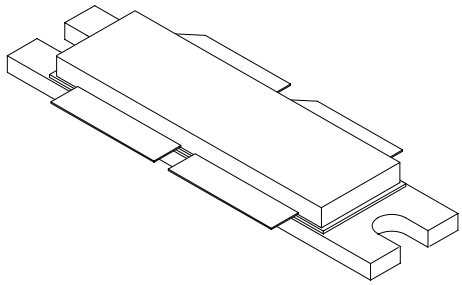


Figure 1. AGR19180EF (flanged) Package

CDMA Features

Typical two carrier CDMA performance:
V_{DD} = 28 V, I_{DQ} = 1600 mA, P_{OUT} = 38 W,
f1 = 1958.75 MHz, f2 = 1961.25 MHz, IS-95/97 CDMA pilot, sync, paging, traffic codes 8—13 (9 channels) 1.2288 MHz channel bandwidth (BW), adjacent channel power ration (ACPR) measured over a 30 kHz BW at f1 – 885 kHz, f2 + 885 kHz. Distortion products measured over 1.2288 MHz channel BW at f1 – 2.5 MHz, f2 + 2.5 MHz. Peak/avg = 9.72 dB @ 0.01% probability on CCDF:

- Output power: 38 W.
- Power gain: 14.5 dB.
- Efficiency: 26%.
- IM3: –33 dBc.
- ACPR: –48.5 dBc
- Return loss: –12 dB.

Device Performance Features

High-reliability, gold-metalization process.

Hot carrier injection (HCI) induced bias drift of <5% over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 1960 MHz, 180 W output power pulsed 4 μs at 10% duty.

Large signal impedance parameters available.

ESD Rating*

AGR19180EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1000	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Table 1. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C	P_D	500	W
Derate Above 25 °C	—	3	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 3. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 400 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	6	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	200	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	12	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 600 μA)	$V_{GS(TH)}$	—	—	3.0	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 2 x 800 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

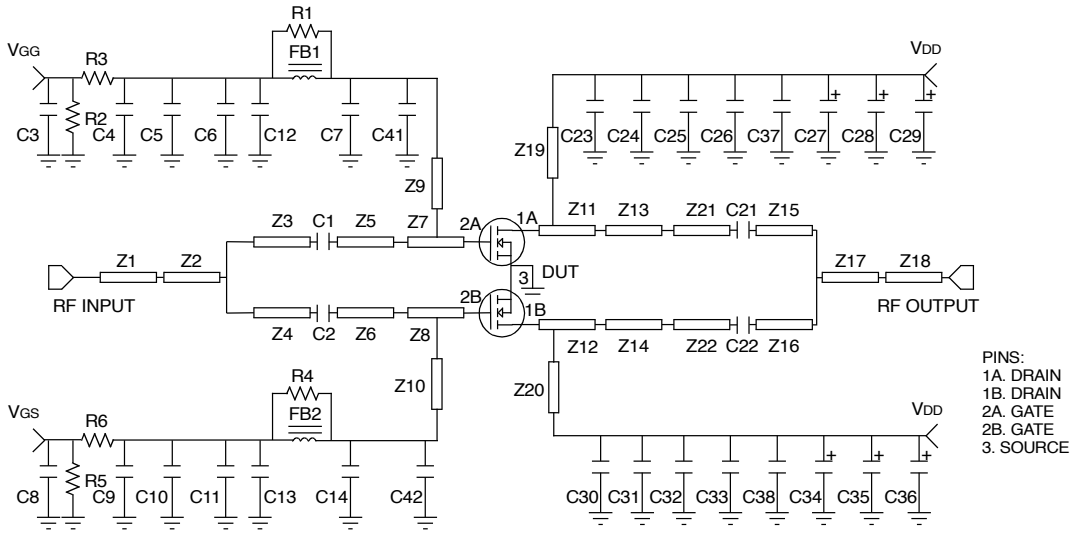
Electrical Characateristics (continued)

Table 4. RF Characteristics

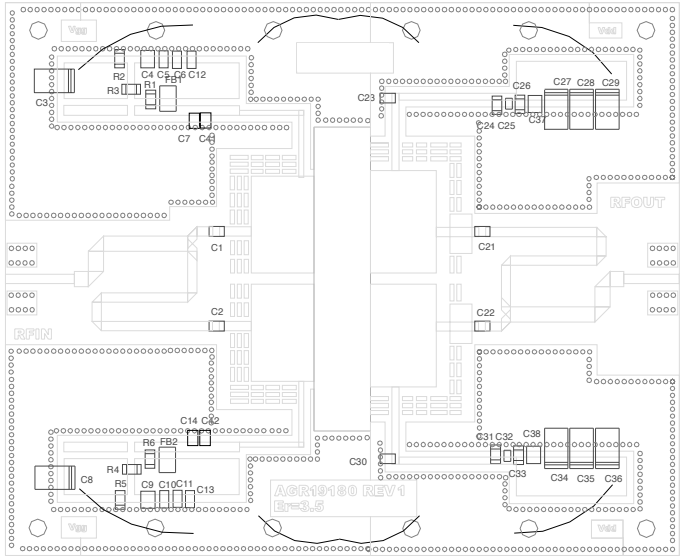
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (Part is internally matched both on input and output.)	C_{RSS}	—	4.0	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{OUT} = 38 W average, two carrier N-CDMA, I_{DQ} = 1600 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	G_{PS}	—	14.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{OUT} = 38 W average, two carrier N-CDMA, I_{DQ} = 1600 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	η	—	26	—	%
Third-order Intermodulation Distortion* (V_{DD} = 28 Vdc, P_{OUT} = 38 W average, two carrier N-CDMA, I_{DQ} = 1600 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; IM3 measured in a 1.2288 MHz integration bandwidth centered at f1 – 2.5 MHz and f2 + 2.5 MHz, referenced to the carrier channel power)	IM3	—	–33	—	dBc
Adjacent Channel Power Ratio* (V_{DD} = 28 Vdc, P_{OUT} = 38 W average, two carrier N-CDMA, I_{DQ} = 1600 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured in a 30 kHz integration bandwidth centered at f1 – 885 kHz and f2 + 885 kHz, referenced to the carrier channel power)	ACPR	—	–48.5	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{OUT} = 38 W average, two carrier N-CDMA, I_{DQ} = 1600 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	IRL	—	–12	—	dB
Ruggedness (V_{DD} = 28 V, P_{OUT} = 180 W continuous wave (CW), I_{DQ} = 1600 mA, f = 1930 MHz, VSWR = 10:1 [all phase angles])	Ψ	No degradation in output power.			

* N-CDMA, typical peak/average ratio of 9.72 dB at 0.01% CCDF, f1 = 1958.75 MHz, and f2 = 1961.25 MHz. V_{DD} = 28 Vdc, I_{DQ} = 2 x 800 mA, and P_{OUT} = 38 W average.

Test Circuit Illustrations



A. Schematic



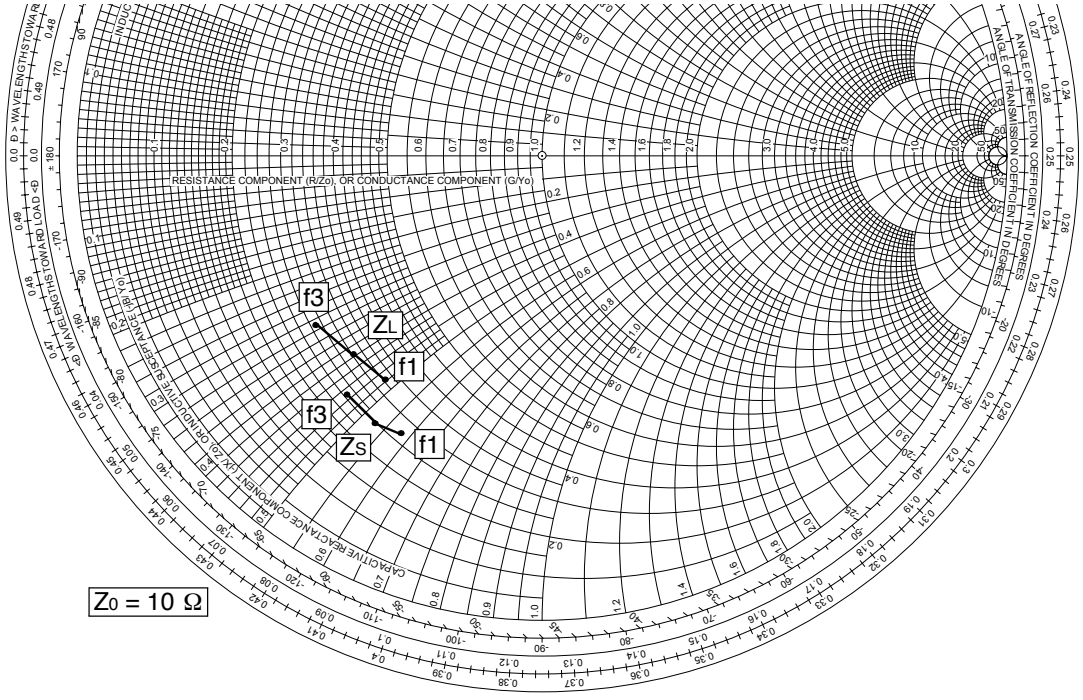
B. Component Layout

Parts List:

- Microstrip line: Z1 0.500 in. x 0.067 in.; Z2, Z17 1.080 in. x 0.110 in.; Z3, Z16 0.210 in. x 0.067 in.; Z4, Z15 2.020 in. x 0.067 in.; Z5, Z6 0.230 in. x 0.067 in.; Z7, Z8 0.455 in. x 0.700 in.; Z9, Z10 1.100 in. x 0.035 in.; Z11, Z12 0.475 in. x 0.740 in.; Z13, Z14 0.100 in. x 0.067 in.; Z18 0.230 in. x 0.067 in.; Z19, Z20 0.490 in. x 0.050 in.; Z21, Z22 0.160 in. x 0.285 in.
- *ATC*® chip capacitor: C1, C2, C21, C22: 10 pF; C7, C14, C23, C30, C41, C42: 8.2 pF; C12, C13: 1000 pF.
- *Kemet*® tantalum capacitor: C27, C34: 10 µF, 35 V T491D; C4, C9, C37, C38: 1 µF, 50 V T491C.
- *Kemet*® chip capacitor: C5, C10, C18, C26, C33: 0.1 µF.
- *Sprague*® tantalum surface-mount chip capacitor: C3, C8, C28, C29, C35, C36: 22 µF, 35 V.
- *Vitramon*® 1206 capacitor: C5, C12: 22000 pF.
- 1206 size chip resistor: R1, R4: 4.7 kΩ; R2, R5 560 kΩ, R3, R6: 1.02 kΩ.
- *Fair-Rite*® ferrite bead: FB1, FB2: 2743019447.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, εr = 3.5.

Figure 2. Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
1930 (f1)	2.58 – j5.9	3.2 – j4.67
1960 (f2)	2.36 – j5.26	2.85 – j3.86
1990 (f3)	2.37 – j4.51	2.72 – j3.07

ZS = Test circuit impedance as measured from gate to gate, balanced configuration.

ZL = Test circuit impedance as measured from drain to drain, balanced configuration.

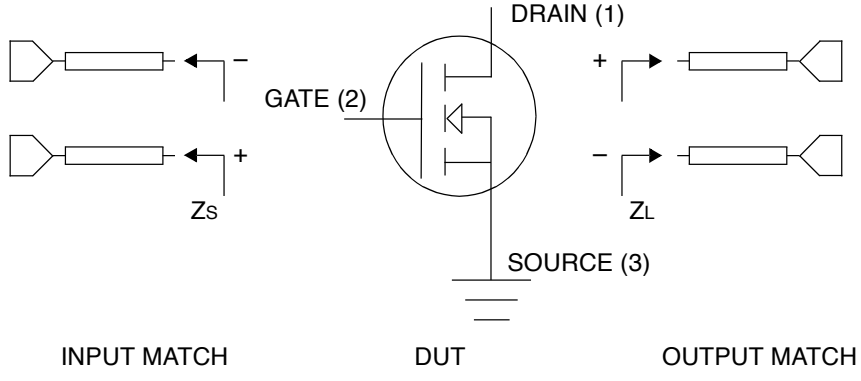


Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)

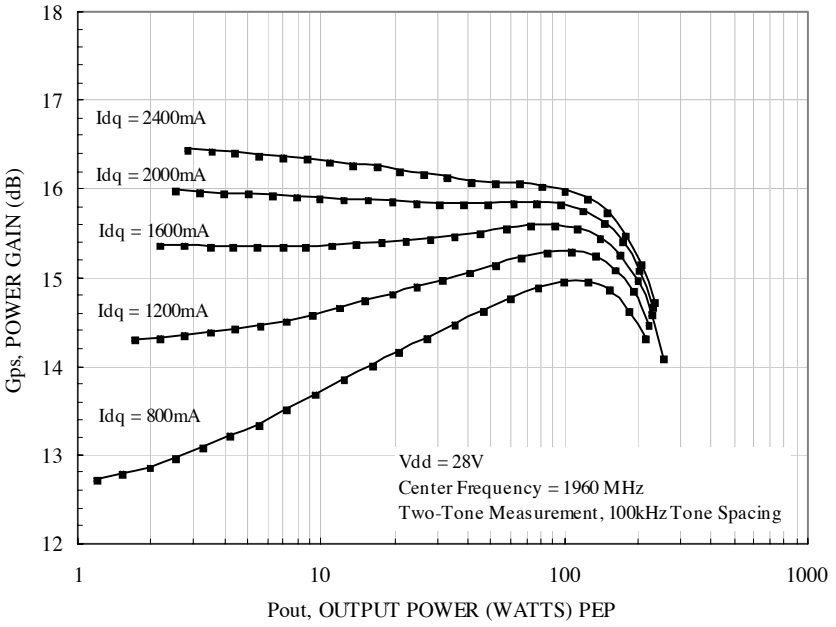


Figure 4. Two-Tone Power Gain versus Output Power

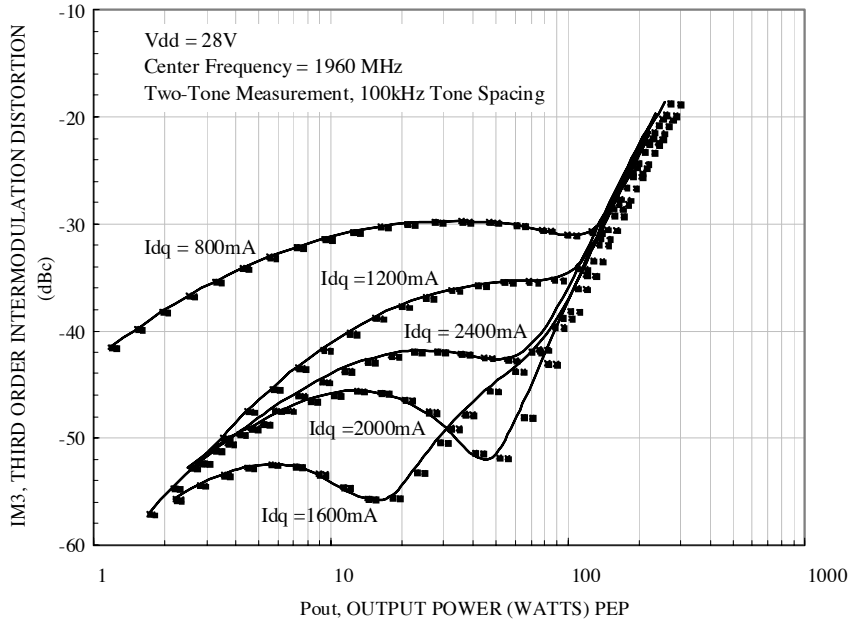


Figure 5. Third Order Intermodulation Distortion versus Output Power

Typical Performance Characteristics (continued)

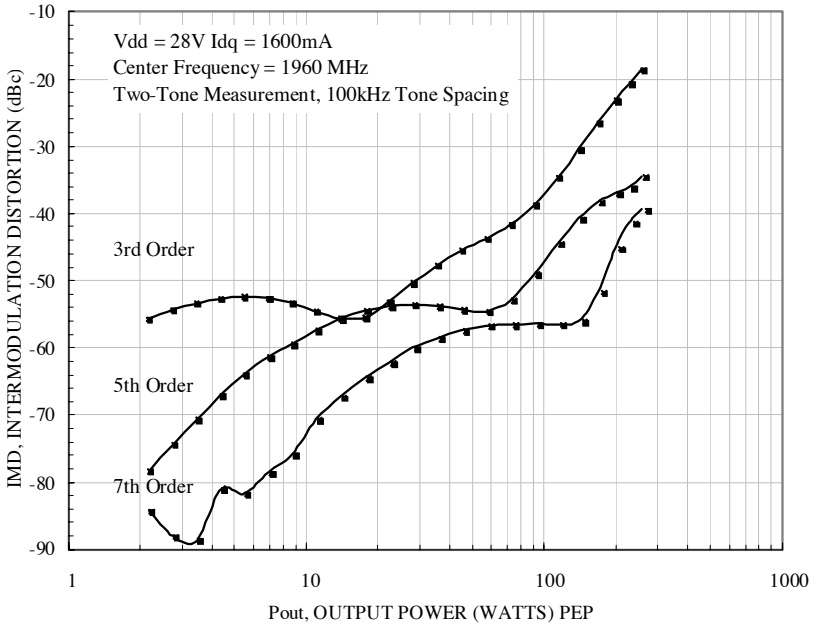


Figure 6. Intermodulation Distortion versus Output Power

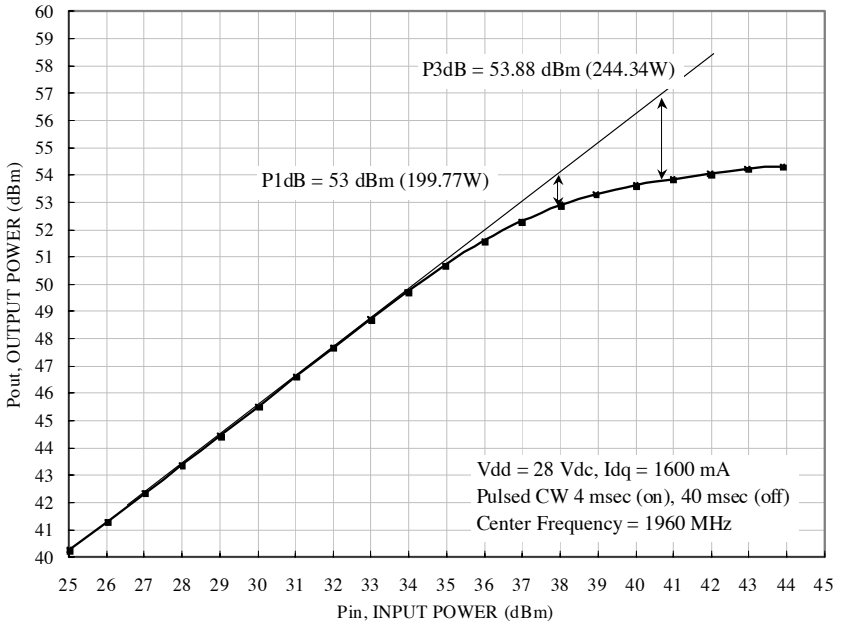


Figure 7. Pulsed CW Output Power versus Input Power

Typical Performance Characteristics (continued)

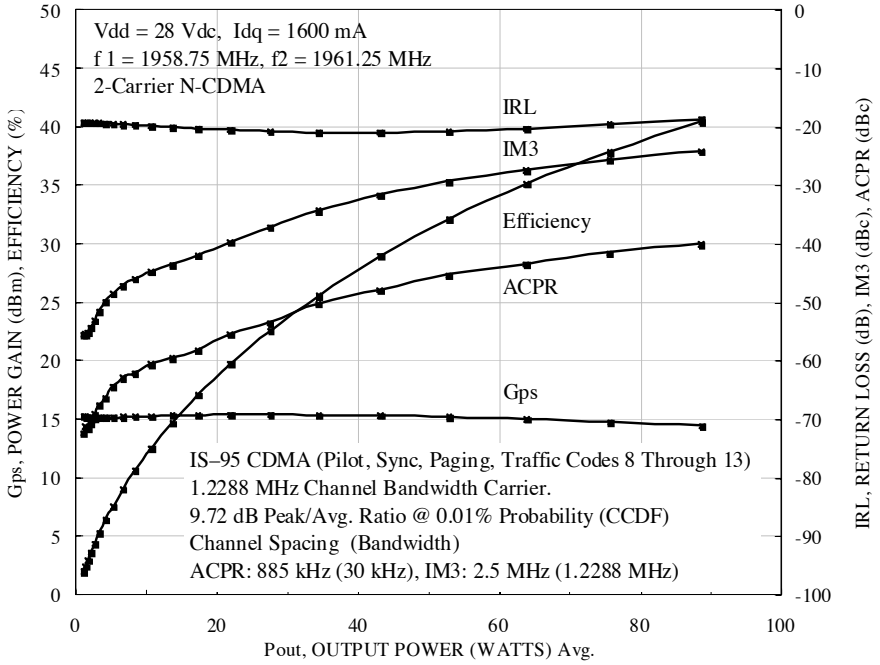


Figure 8. Two-Carrier N-CDMA ACPR, IM3, Power Gain, Drain Efficiency versus Output Power

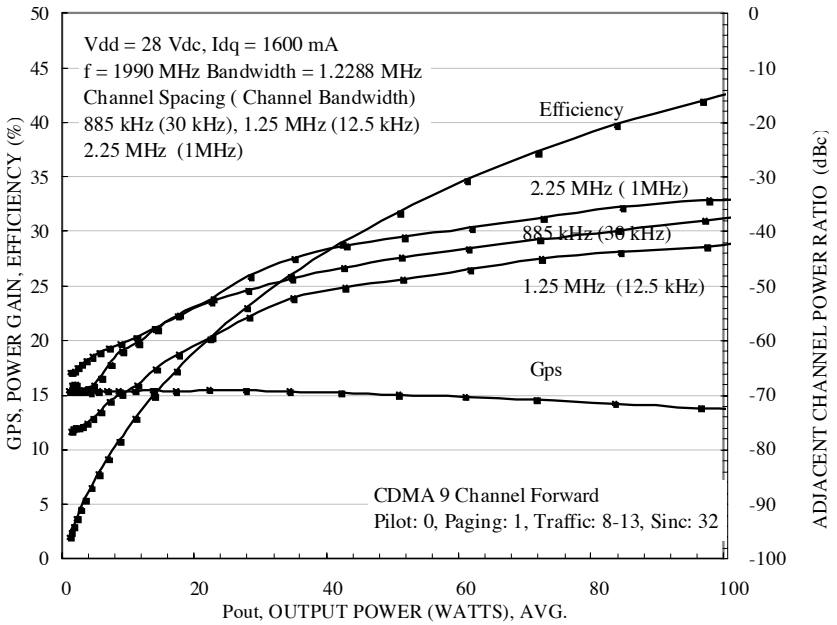
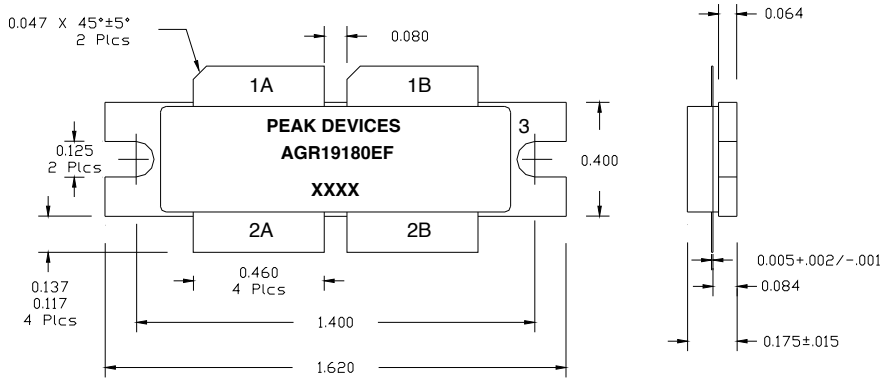


Figure 9. N-CDMA ACPR, Power Gain, Drain Efficiency versus Output Power

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.



PINS:
1A. DRAIN
1B. DRAIN
2A. GATE
2B. GATE
3. SOURCE

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