TriQuint SEMICONDUCTOR

AGR26180EF
180 W, 2.535 GHz—2.655 GHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR26180EF is a high-voltage, gold-metalized, enhancement mode, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for ultrahigh-frequency (UHF) applications, including multichannel multipoint distribution service (MMDS) for broadcasting and communications.

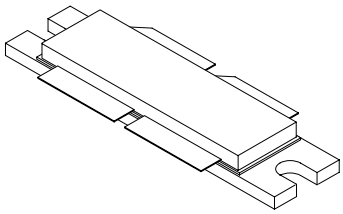


Figure 1. AGR26180EF Flanged Package

Features

Typical performance for MMDS systems.
f = 2600 MHz, I_{DQ} = 1700 mA, Vds = 28 V,
adjacent channel BW = 3.84 MHz, 5 MHz offset;
alternate channel BW = 3.84 MHz, 10 MHz offset.
Typical P/A ratio of 9.8 dB at 0.01% (probability) CCDF*:

— Output power: 27 W.
— Power gain: 12.5 dB.
— Efficiency: 20%.
— ACPR: –33 dBc.
— ACLR1: –35 dBc.
— Return loss: –12 dB.

Typical pulsed P1dB, 6 μs pulse at 10% duty: 185 W.
High-reliability, gold-metalization process.
Hot carrier injection (HCI) induced bias drift of <5% over 20 years.
Internally matched.
High gain, efficiency, and linearity.
Integrated ESD protection.
Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 2600 MHz, 180 W output power pulsed 4 μs at 10% duty.
Large signal impedance parameters available.

*The test signal utilized is 4-channel W-CDMA Test Model 1. This test signal provides an equivalent reference (occupied bandwidth and waveform EPF) for the actual performance with an MMDS waveform.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, +15	Vdc
Total Dissipation at T_C = 25 °C	P_D	500	W
Derate Above 25 °C	—	3	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, +150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR26180EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1000	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

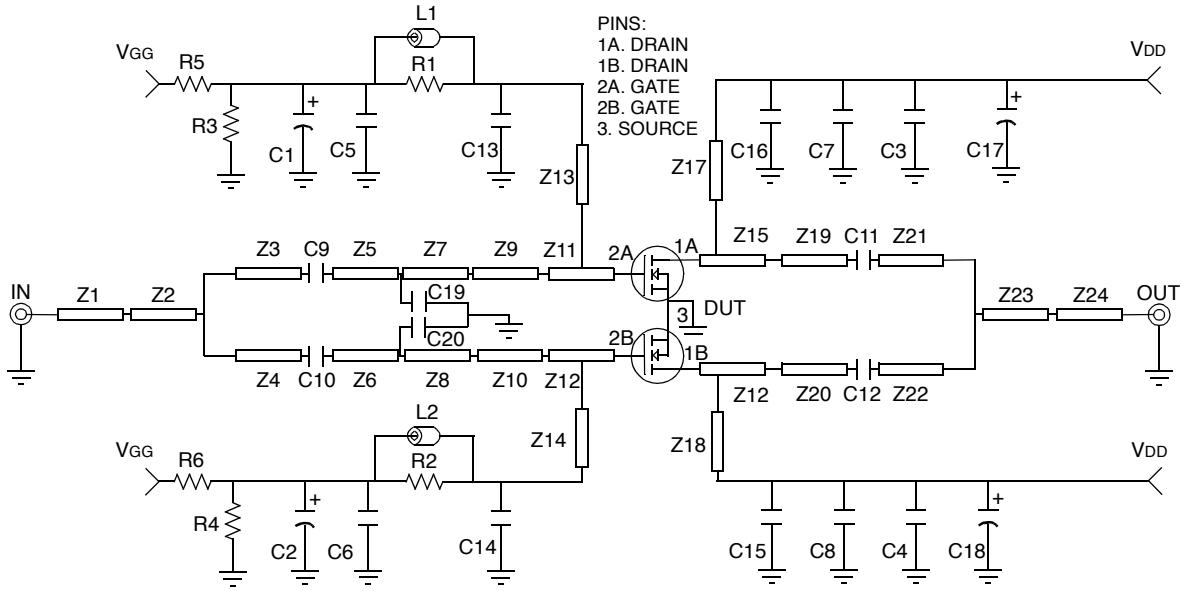
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 400 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	6	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	200	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	12	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 600 μA)	$V_{GS(TH)}$	2.8	3.4	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 2 x 850 mA)	$V_{GS(Q)}$	3.0	3.7	4.6	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

Table 5. RF Characteristics

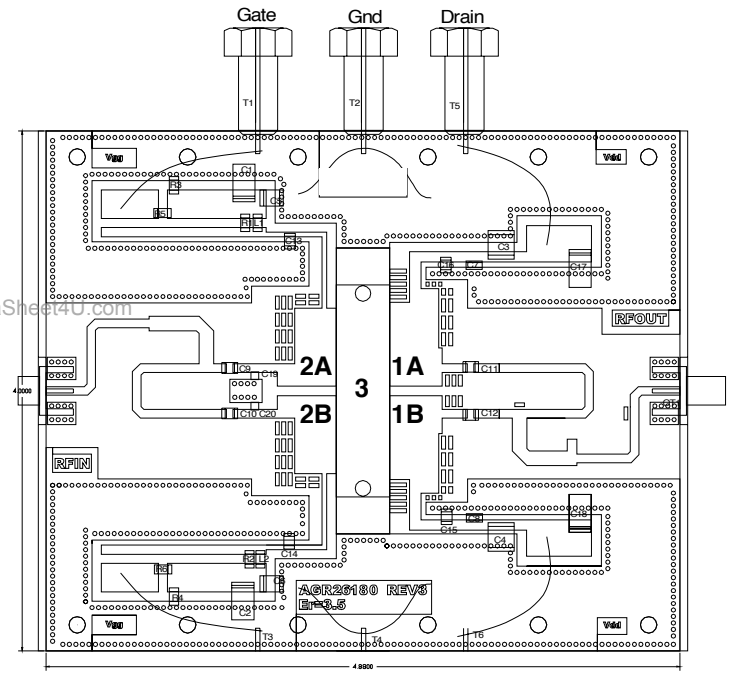
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	4.0	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain*	G_{PS}	—	12.5	—	dB
Drain Efficiency*	η	—	20	—	%
Third-order Intermodulation Distortion* (IM3 distortion measured over 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz)	IM3	—	–36	—	dBc
Adjacent Channel Power Ratio* (ACPR measured over BW of 3.84 MHz @ f1 – 5 MHz and f2 + 5 MHz)	ACPR	—	–40	—	dBc
Input Return Loss*	IRL	—	–12	—	dB
Power Output, 1 dB Compression Point, pulsed 4 μs at 10% duty. (V_{DD} = 28 V, f_C = 2655.0 MHz, pulsed 6 μs at 10% duty)	P_{1dB}	—	185	—	W
Output Mismatch Stress (V_{DD} = 28 V, P_{OUT} = 180 W (pulsed 4 μs at 10% duty), I_{DQ} = 2 x 850 mA, f_C = 2655.0 MHz VSWR = 10:1; [all phase angles])	ψ	No degradation in output power.			

* 3GPP W-CDMA, typical P/A ratio of 8.5 dB at 0.01% CCDF, f1 = 2645.0 MHz, and f2 = 2655 MHz. V_{DD} = 28 Vdc, I_{DQ} = 2 x 850 mA, and P_{OUT} = 27 W average. Nominal operating voltage 28 Vdc.

Test Circuit Illustrations for AGR26180EF



A. Schematic



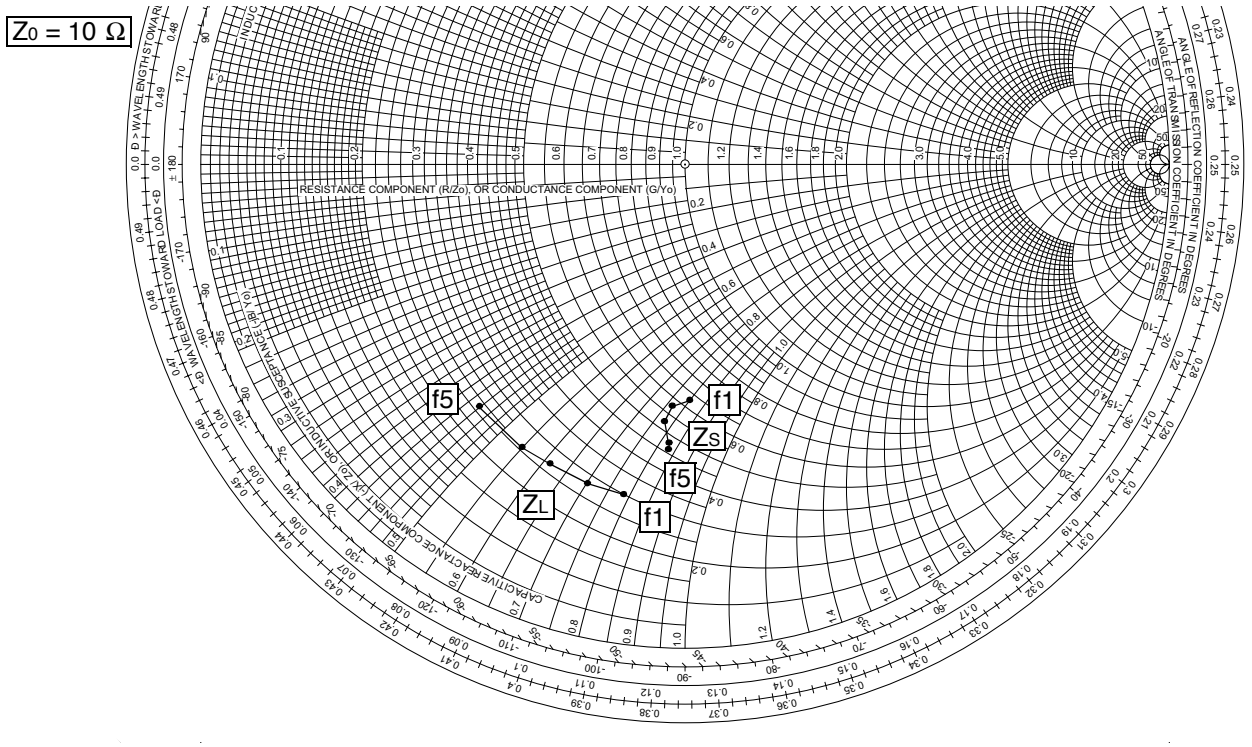
Parts List:

- Microstrip line: Z1, Z29 1.330 in. x 0.066 in.;
  Z2, Z27 0.753 in. x 0.112 in.;
  Z3 0.145 in. x 0.066 in.; Z4 1.578 in. x 0.066 in.;
  Z5, Z6 0.160 in. x 0.066 in.;
  Z7, Z8 0.172 in. x 0.066 in.;
  Z9, Z10 0.134 in. x 0.171 in.;
  Z11, Z12 0.320 in. x 0.600 in.;
  Z13, Z14 0.856 in. x 0.043 in.;
  Z15, Z16 0.155 in. x 0.645 in.;
  Z17, Z18 0.217 in. x 0.750 in.;
  Z19, Z20 0.473 in. x 0.088 in.;
  Z21, Z22 0.026 in. x 0.293 in.;
  Z23, Z24 0.194 in. x 0.066 in.;
  Z25 1.718 in. x 0.066 in.; Z26 0.341 in. x 0.066 in.;
  Z28 0.150 in. x 0.075 in.
- *ATC®* chip capacitor:
  C9, C10, C11, C12: 4.7 pF 100B47_J500;
  C3, C14, C15, C16: 5.6 pF 100B5R6J_500;
  C19, C20: 0.7 pF 100A0R7J_500.
  C27: 47 pF 100A470JW;
  C28: 8.2 pF 100B8R2BW.
  C4, C5: 12 pF 100B120JW;
- *Murata®* 50 V chip capacitor:
  C3, C4: 4.7 µF, GRM55ER7H475KA01;
  C5, C6: 2.2 µF, GRM43ER71H225KA01L;
  C7, C8: 0.12 µF, LLL31MR71H124MD01.
- *AVX™* 35 V capacitor:
  C1, C2, C17, C18: 15 µF TPSD156K035R0300.
- 1206 size chip resistors:
  R1, R2: 4.7 Ω; R3, R4: 560 kΩ; R5, R6 470 Ω.
- *Fair-Rite®* ferrite bead L1, L2: 2512067007Y3.
- *Taconic®* ORCER RF-35: board material,
  1 oz. copper, 30 mil thickness, εr = 3.5.

B. Component Layout

Figure 2. Component Layout

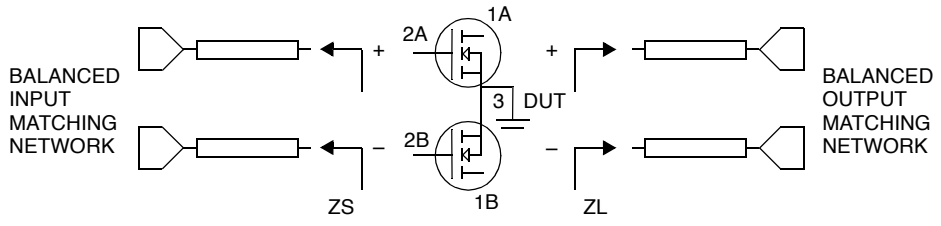
Typical Performance Characteristics



MHz (f)	ZS Ω (complex source impedance)	ZL Ω (complex optimum load impedance)
2500 (f1)	6.4 – j8.0	3.0 – j7.8
2550 (f2)	5.8 – j7.6	2.9 – j7.0
2600 (f3)	5.2 – j7.7	2.7 – j6.2
2650 (f4)	4.7 – j8.3	2.6 – j5.5
2700 (f5)	4.5 – j8.4	2.5 – j4.7

ZS = Test circuit impedance as measured from gate to gate, balanced configuration.

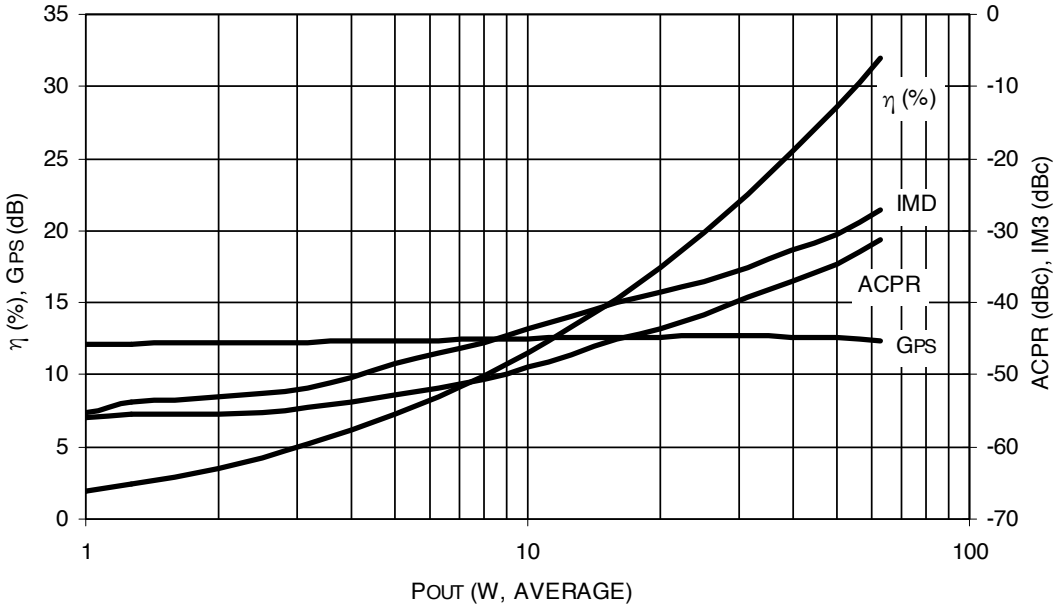
ZL = Test circuit impedance as measured from drain to drain, balanced configuration.



PINS: 1A & 1B DRAIN, 2A & 2B GATE, 3 SOURCE

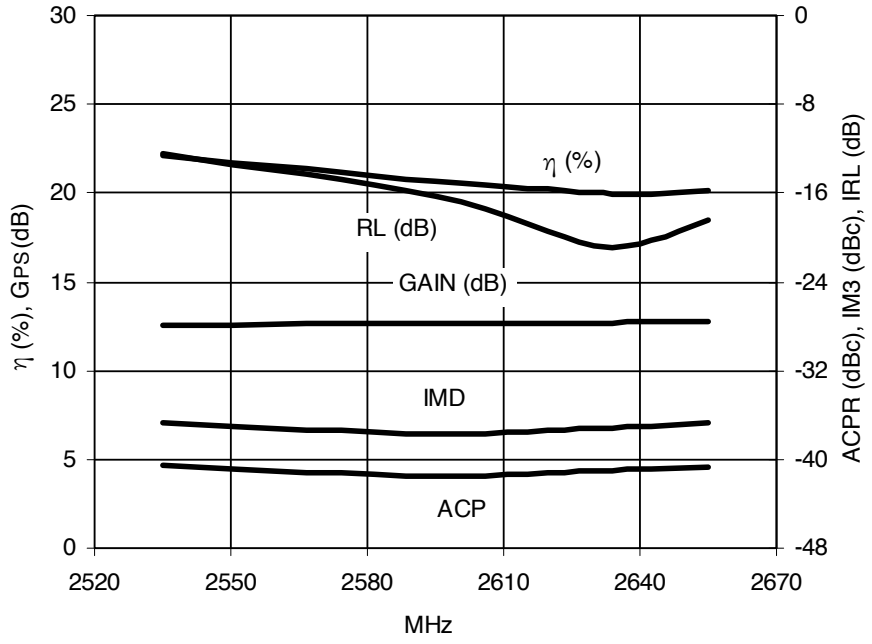
Figure 3. Series Equivalent Balanced Input and Output Impedances

Typical Performance Characteristics (continued)



Test conditions:
Two-carrier W-CDMA 3GPP, peak-to-average = 8.5 dB @ 0.01% CCDF, f1 = 2590 MHz, f2 = 2600 MHz, V_{DD} = 28 V, I_{DQ} = 1700 mA.

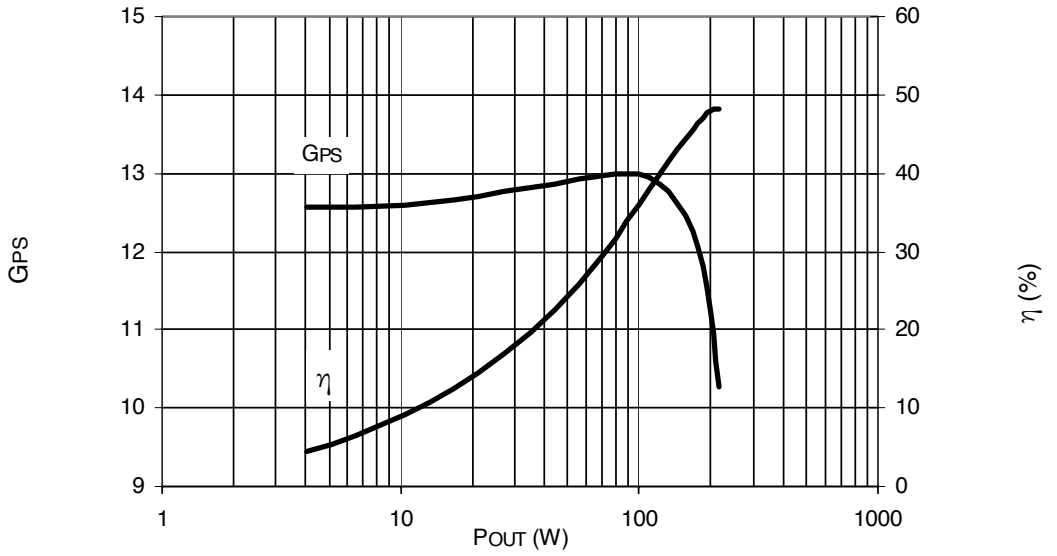
Figure 4. Power Gain, Drain Efficiency, ACPR, and IM3 vs. Output Power



Test conditions:
Two-carrier W-CDMA 3GPP, peak-to-average = 8.5 dB @ 0.01% CCDF, f1 = 2590 MHz, f2 = 2600 MHz, V_{DD} = 28 V, I_{DQ} = 1700 mA, P_{OUT} = 27 W.

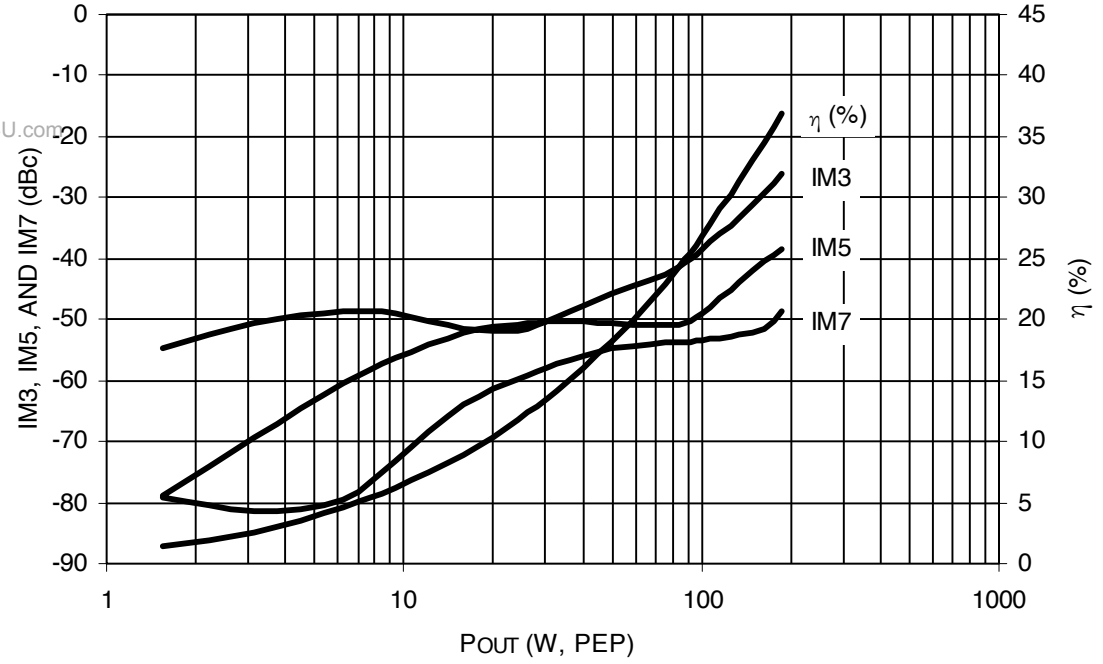
Figure 5. Power Gain, Drain Efficiency, ACPR, IM3, and IRL vs. Frequency

Typical Performance Characteristics (continued)



Test conditions:
28 VDS, IDQ = 1700 mA, 2600 MHz.

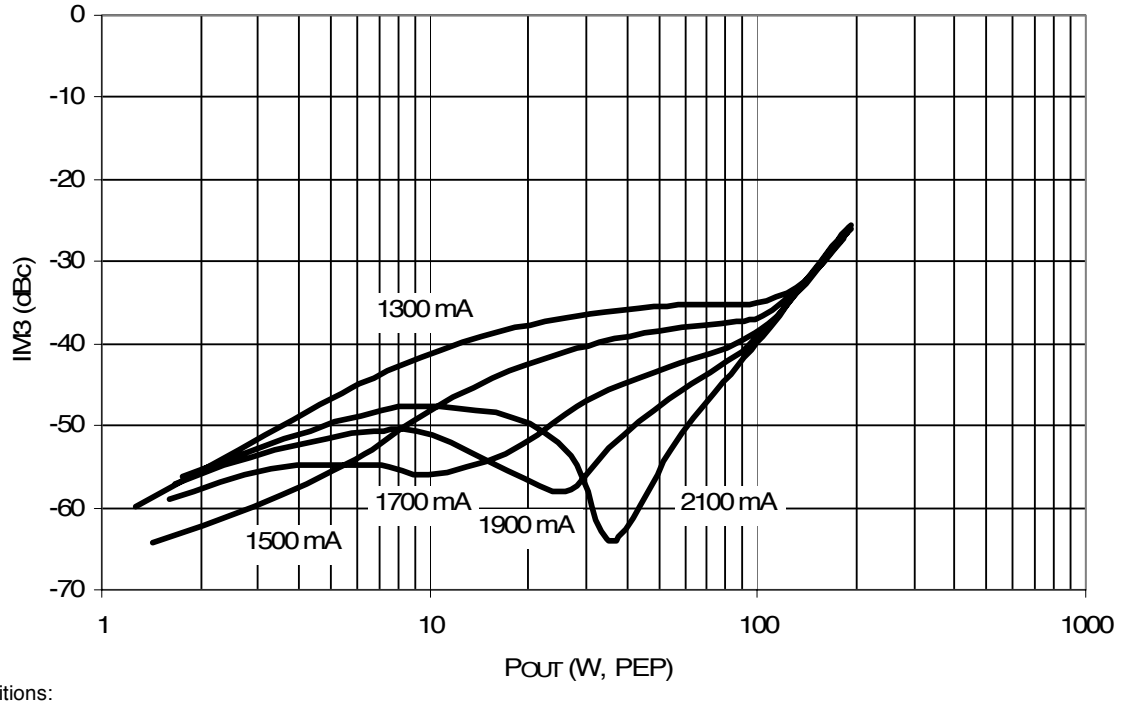
Figure 6. Power Gain and Drain Efficiency vs. Output Power (CW signal data)



Test conditions:
Two-tone measurement @ 10 MHz tone spacing, VDD = 28 VDC, f1 = 2590 MHz, f2 = 2600 MHz.

Figure 7. IMD vs. POUT

Typical Performance Characteristics (continued)



Test conditions:
Two-tone measurement @ 10 MHz tone spacing, V_{DD} = 28 V_{DC}, f1 = 2590 MHz, f2 = 2600 MHz.

Figure 8. IMD vs. Output Power and I_{DQ}

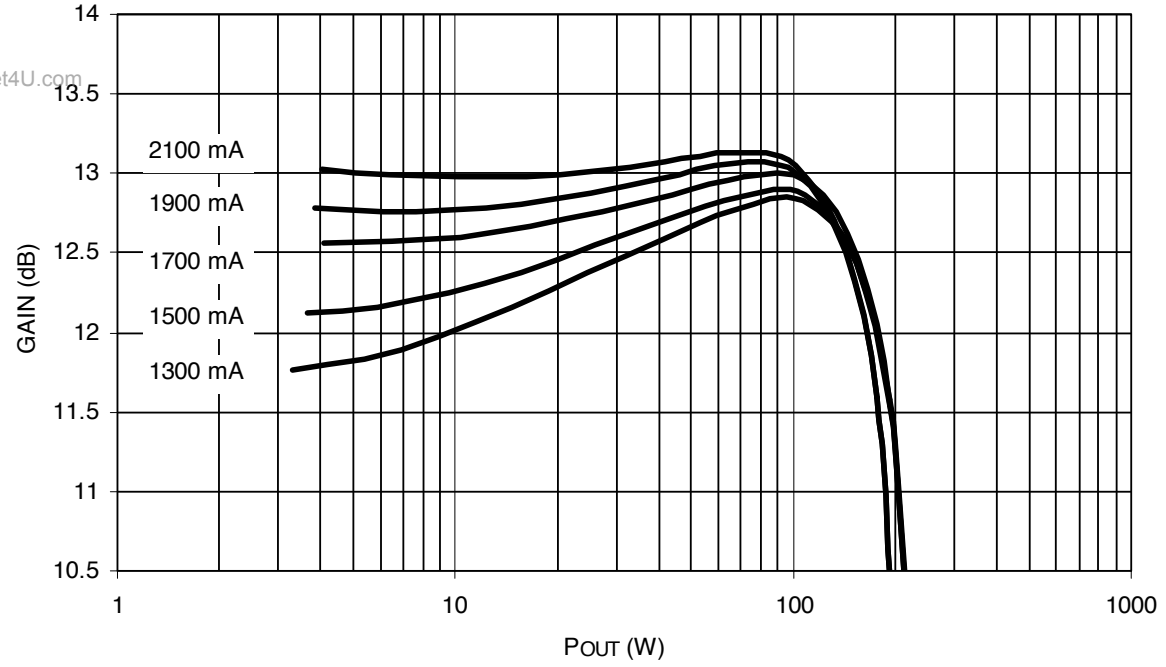
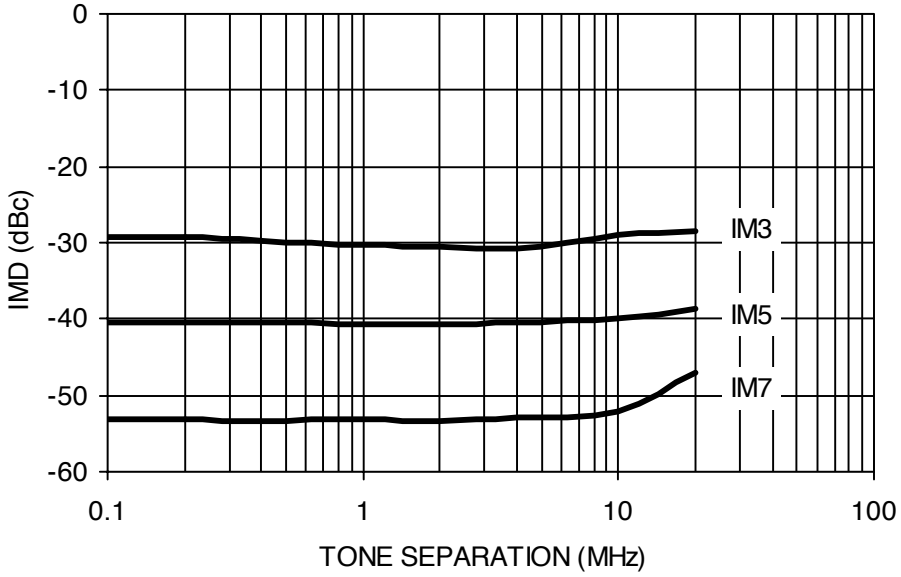


Figure 9. Power Gain vs. Output Power and I_{DQ}

Typical Performance Characteristics (continued)

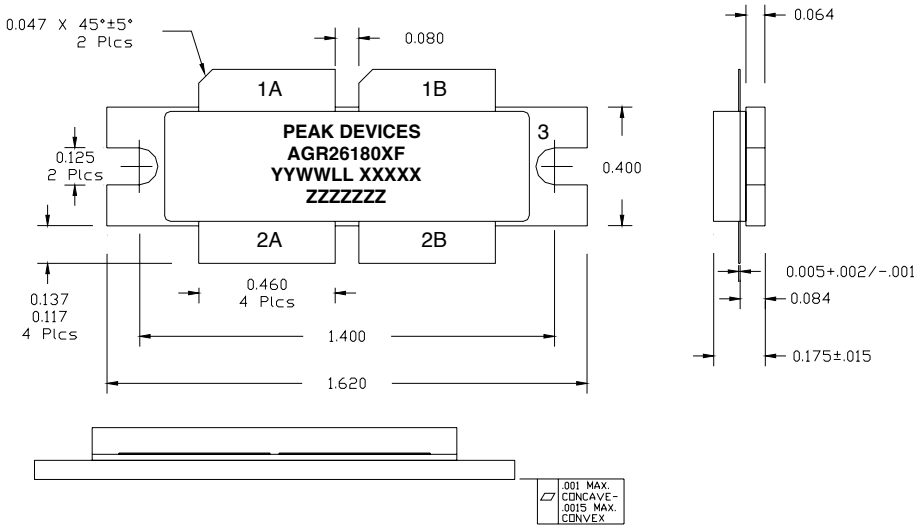


Test conditions:
Two-tone measurement @ POUT = 160 W (PEP).

Figure 10. IMD vs. Tone Separation

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.



PINS:
1A. DRAIN
1B. DRAIN
2A. GATE
2B. GATE
3. SOURCE

Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.