AH11

High Dynamic Range Dual Amplifier

Applications

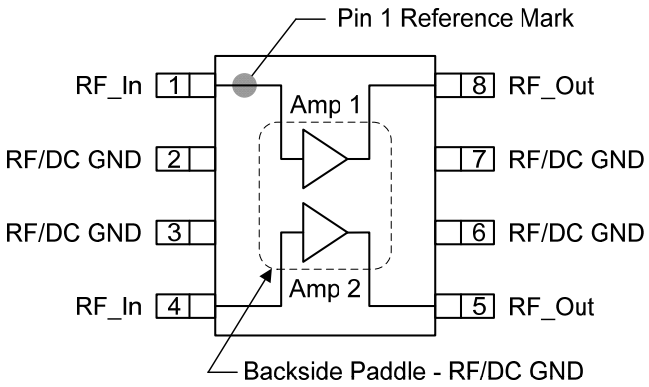
- Mobile Infrastructure
- Defense / Homeland Security
- Fixed Wireless

SOIC-8 package

Product Features

- 150 – 3000 MHz
- +44 dBm OIP3 (1900 MHz, balanced circuit)
- Single-ended performance:
  - 13.5 dB Gain
  - 2.7 dB Noise Figure
  - +21 dBm P1dB
- Single +5 Volt Supply
- Lead-free / RoHS-compliant SOIC-8 package

Functional Block Diagram



General Description

The AH11 is a high linearity amplifier for use in digital communication systems. It combines low noise figure and high intercept point into a low-cost SMT solution. This device extends the linear efficiency advantages of TriQuint's AH1 to higher power levels by combining two internally matched die. This dual-amplifier configuration allows for the optimal design of balanced or push-pull operation. The amplifier can also be used for single-ended operation in each branch of a diversity receive system.

A mature and reliable GaAs MESFET technology is employed to maximize linearity while achieving low noise figure. The SOIC-8 package is lead-free /RoHS-compliant package and is thermally enhanced to achieve an MTTF greater than 100 years at a case temperature of 85°C. All devices are 100% RF and DC tested.

Pin Configuration

Pin No.	Function
1	RF In (Amp 1)
2, 3, 6, 7	RF/DC GND
4	RF In (Amp 2)
5	RF Out (Amp 2)
8	RF Out (Amp 1)
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
AH11-G	High Dynamic Range Dual Amplifier
AH11BAL-PCB	0.6-2.1 GHz Balanced Eval Board

Standard T/R size = 500 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +125 °C
RF Input Power, CW, 50Ω,T = 25ºC	4 dB above Input P1dB
Supply Voltage	+6 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}		+5		V
T_{ch} (for >10^6 hours MTTF)			+160	ºC
Operating Temp. Range	-40		+85	ºC

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications (Single-Ended Configuration)

Test conditions unless otherwise noted: T = 25 ºC, Supply Voltage = +5 V, Frequency = 800 MHz, 50 Ω System, tested on each single-ended amplifier (there are two amplifiers in an AH11 package)

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		150		3000	MHz
Test Frequency			800		MHz
Gain		12.4	13.5		dB
Input Return Loss	See Note 1.		-8		dB
Output Return Loss			-15		dB
Output P1dB			+21		dBm
Output IP3	See Note 2.	+37	+41		dBm
Noise Figure			2.7		dB
Supply Voltage (V_{dd})			5		V
Operating Current (I_{dd})		120	150	180	mA
Thermal Resistance (jnc. to case)				29	°C/W

Notes:
1. S21 and S11 can be improved in the band of interest with some slight input tuning.
2. OIP3 measured with two tones at an output power of +5 dBm/tone separated by 10 MHz. The suppression of the largest IM3 product is used to calculate the OIP3 using a 2:1 rule. Slight OIP3 degradation of about 2 dB is expected to occur at lower temperatures (from 25 ºC to –40 ºC).

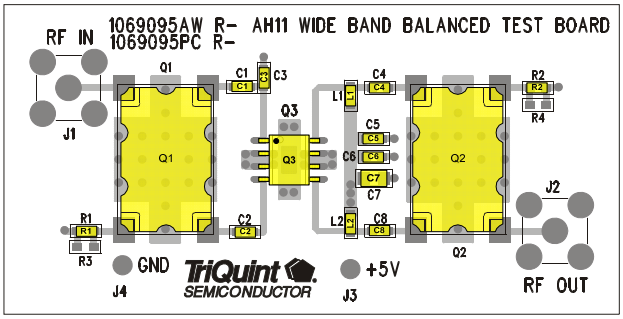
Device Characterization Data

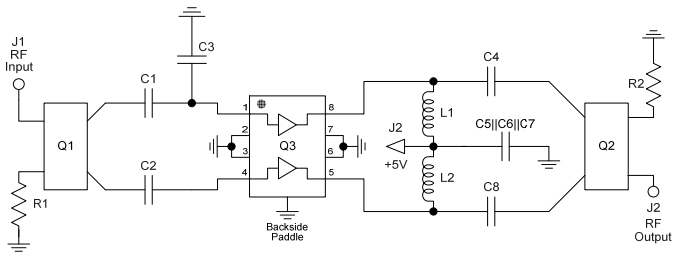
S-Parameter Data

S-Parameters, single unmatched device (2 per package): V_{dd} = +5 V, 100% I_{DSS}, T = 25 °C, 50 Ω system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (angle)	S22 (dB)	S22 (ang)
50	-2.63	-31.03	17.82	162.23	-23.39	47.82	-6.12	-36.95
250	-9.02	-47.58	14.82	156.18	-20.06	8.90	-16.47	-55.07
500	-9.98	-61.76	14.31	144.67	-20.01	-1.10	-20.37	-43.85
750	-10.09	-83.24	13.83	132.14	-20.02	-6.79	-21.92	-31.28
1000	-10.11	-102.89	13.29	119.28	-20.11	-11.57	-21.92	-23.71
1250	-9.98	-122.71	12.76	106.77	-20.25	-14.32	-22.27	-17.24
1500	-9.69	-141.39	12.18	94.43	-20.31	-18.20	-22.53	-17.00
1750	-9.28	-159.83	11.61	83.21	-20.53	-21.39	-22.93	-10.89
2000	-8.86	-175.83	11.06	72.08	-20.71	-24.33	-23.65	-9.69
2250	-8.41	169.88	10.49	61.25	-20.82	-27.30	-23.68	-13.98
2500	-7.81	155.71	9.92	50.78	-20.98	-29.62	-23.88	-1.56
2750	-7.26	143.52	9.41	41.01	-21.11	-31.71	-25.42	-1.60
3000	-6.70	133.22	8.81	31.62	-21.22	-34.23	-24.24	5.13

Reference Design 600-2100 MHz (AH11BAL-PCB)





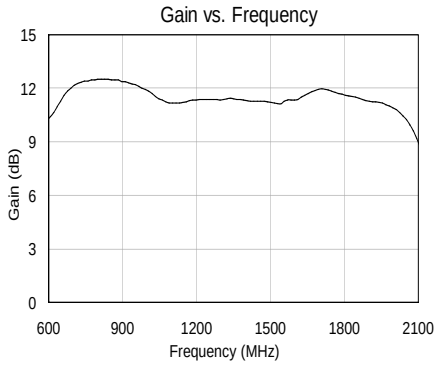
Bill of Material

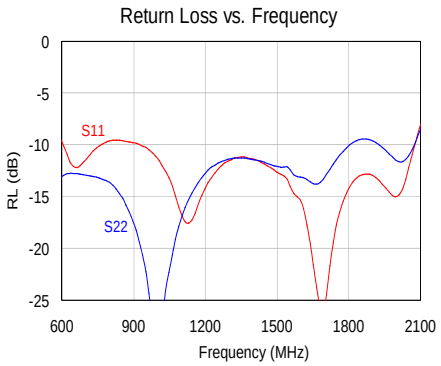
Ref. Des.	Value	Description	Manufacturer	Part Number
Q3	n/a	Dual Amplifier, SOIC-8 Package	TriQuint	AH11-G
Q1, Q2	n/a	SMT 90 deg. Hybrid Coupler	Anaren	11305-3
C1, C2, C4, C5, C8	56 pF	Cap, Chip, 0603, 5%, 50V, NPO	various	
C3	2.0 pF	Cap, Chip, 0603, +/-0.1 pF, 50V NPO	various	
C6	4700 pF	Cap, Chip, 0603, 5%, 50V, X7R	various	
C7	0.01 uF	Cap, Chip, 0805, 5%, 50V, X7R	various	
L1, L2	12 nH	Ind, Chip, 0603, 5%, Ceramic	various	
R1, R2	50 Ω	Res, Chip, 0603, 5%	various	

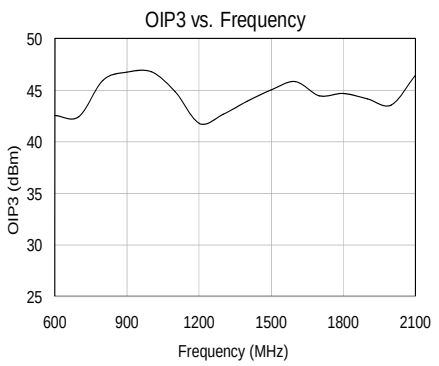
Typical Performance 600-2100 MHz (AH11BAL-PCB)

Test conditions unless otherwise noted: V_{dd} = 5V, I_{dd} = 300 mA, +25 °C

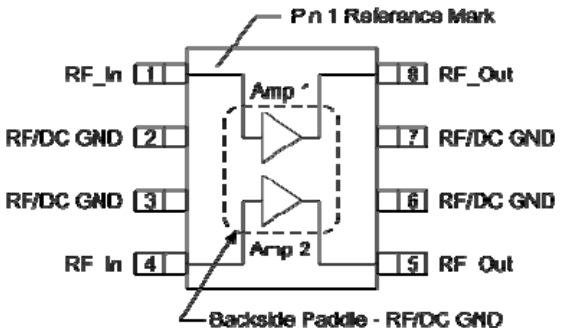
Frequency	MHz	600	900	1900	2100
Gain	dB	10.7	12.2	11.2	10.6
Input Return Loss	dB	-10	-10	-14	-10
Output Return Loss	dB	-13	-18	-10	-10
Noise Figure	dB	7.6	4.1	4.2	5.6
Output IP2	dBm	+63	+65	+65	+63
Output IP3	dBm	+42	+46	+44	+45







Pin Description



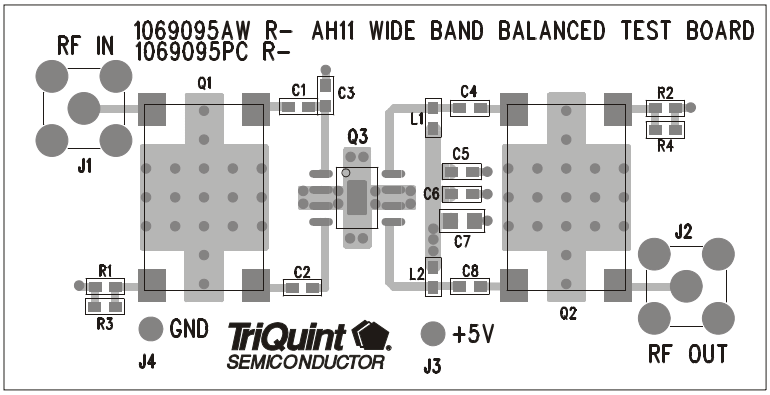
Pin	Label	Description
1	RF In (Amp 1)	RF Input. Requires matching circuit to 50 Ω. See application circuits.
2, 3, 6, 7	Ground	RF/DC ground. Provide via path to ground.
4	RF In (Amp 2)	RF Input. Requires matching circuit to 50 Ω. See application circuits.
5	RF Out (Amp 2)	RF Output. Requires DC blocking capacitor. See application circuits.
8	RF Out (Amp 1)	RF Output. Requires DC blocking capacitor. See application circuits.
n/a	Backside Paddle	Use recommended via pattern to minimize inductance and thermal resistance

Applications Information

PC Board Layouts

PCB Material (stackup):

1/2oz. Cu top layer
0.014 inch Nelco N-4000-13
1/2oz. Cu middle layer 1
Core Nelco N-4000-13
1/2 Cu middle layer 2
0.014 inch Nelco N-4000-13
1/2oz. Cu bottom layer
Finished board thickness is 0.062±.006



The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

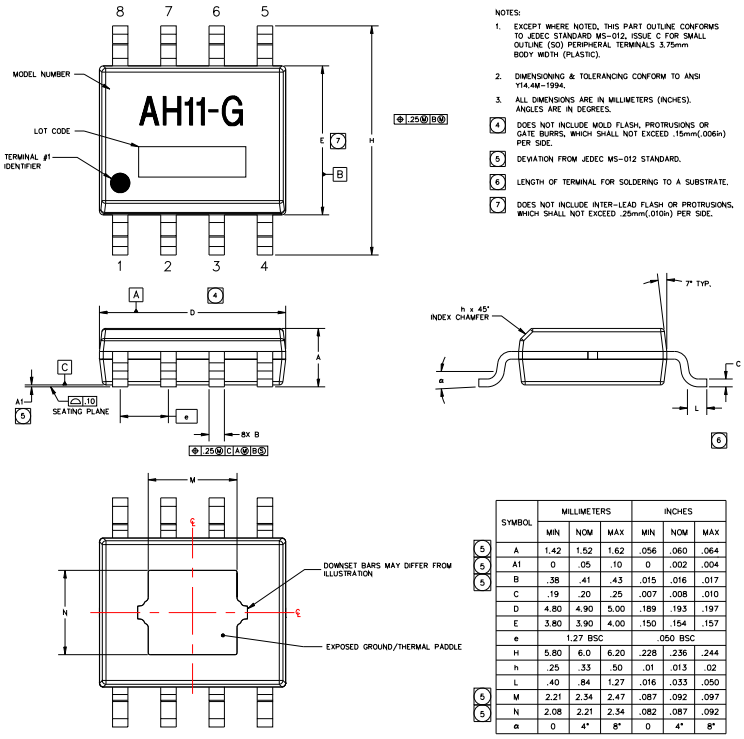
For further technical information, Refer to
http://www.triquint.com/prodserv/more_info/default.aspx?prod_id=AH11

Mechanical Information

Package Information and Dimensions

This package is lead-free/Green/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260°C reflow temperature) and lead (maximum 245°C reflow temperature) soldering processes.

The component will be marked with an "AH11-G" designator with an alphanumeric lot code on the top surface of the package.

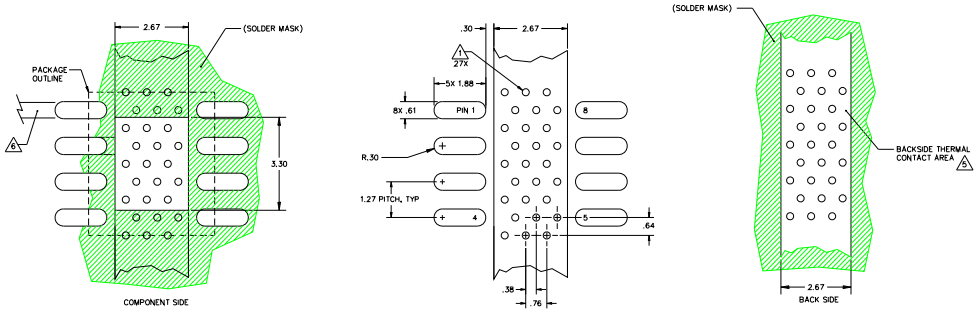


NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°	8°	0	4°	8°

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80/.0135") diameter drill and have a final plated through diameter of .25mm (.010")
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. To ensure reliable operation, device ground paddle-to-ground pad solder joint is critical.
4. Add mounting screws near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. For optimal thermal performance, expose soldermask on backside where it contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. If the PCB design rules allow, ground vias should be placed under the land pattern for better RF and thermal performance. Otherwise ground vias should be placed as close to the land pattern as possible.
9. All dimensions are in mm. Angles are in degrees.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: Passes from 500 to 1000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

The part is rated Moisture Sensitivity Level 2 at 260°C convection reflow per JEDEC standard IPC/JEDEC J-STD-020A.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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