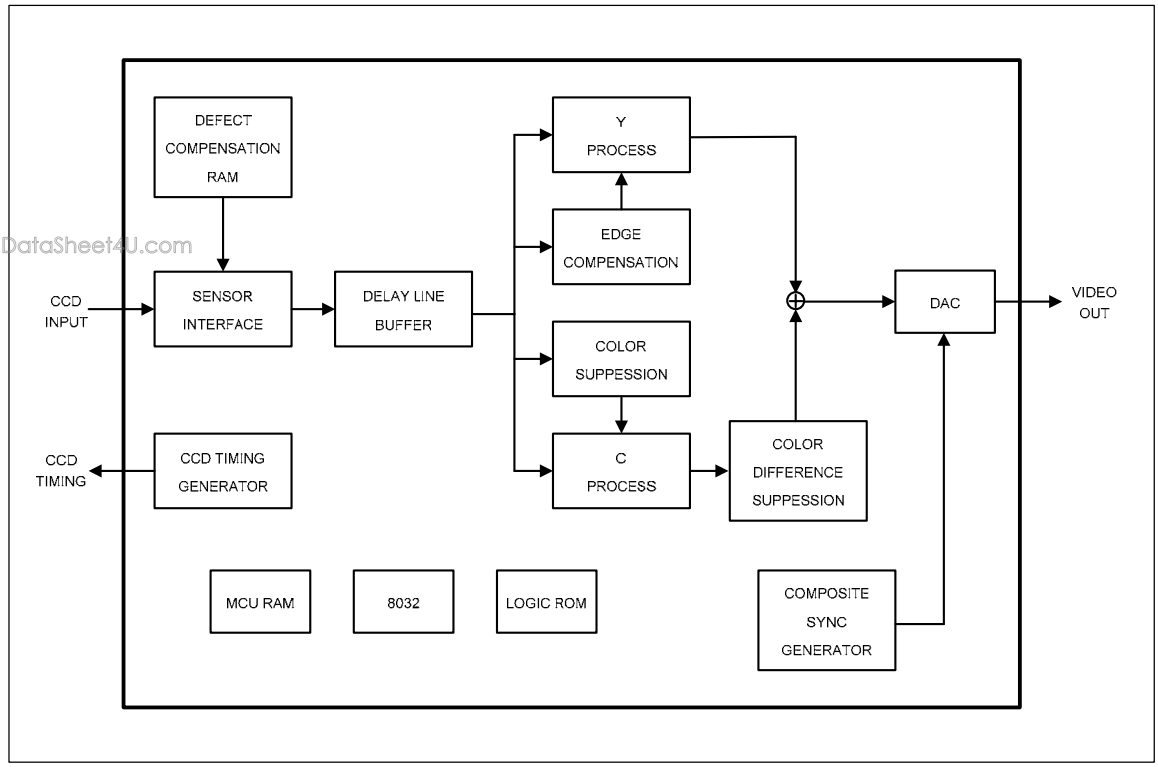
GENERAL DESCRIPTION

The Ai2152 is a digital signal-processing chip for color video camera. It includes timing generator and digital/analog output. Supports 250K/380K NTSC system CCD sensors and 290K/440K PAL system CCD sensors with complementary color filter. It also provided line lock function.

FEATURES

- Support Ye, Cyan, Magenta, Green complementary color filter CCD sensors for
  NTSC : Ai325CA(250K), Ai338CA(380K)
  PAL : Ai329CA(290K), Ai344CA(440K)
- Support external EEPROM to store parameter.
- Built-in auto white balance control.
- Built-in auto exposure control.
- Built-in 9bit digital to analog converter.
- Built-in mirror function.
- Built-in blemish compensation circuit storing the data in EEPROM, up to 200 blemish pixels.
- Support analog video output and UYVY (proprietary format) digital output.
- Built-in timing generator for vertical driver and CDS/AGC/ADC peripheral chips.
- Support line lock function.
- Single 3.3V power supply. (Horizontal drive pins can be 3.3V/5V)
- LQFP-80. (0.4mm pin pitch)
- Support user Definable GPIO.
- Programmable CCD Timing Driving Current.
- Programmable pull-up GPIO pin

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Symbol	I/O, P/G	Description
1	Reset	B	System Reset
2	OSCI	I	OSC input
3	OSCO	B	OSC output
4	V_{CC}	P	V_{DD} for Oscillator
5	GND	P	GND for Oscillator
6	ADCLK	O	Clock Output for AFE ADC
7	AFE_SCL	O	AFE 3-Wire SCL
8	AFE_SDA	O	AFE 3-Wire SDA
9	DATAIN9	I	CCD Image Data (MSB)
10	DATAIN8	I	CCD Image Data
11	DATAIN7	I	CCD Image Data
12	DATAIN6	I	CCD Image Data
13	DATAIN5	I	CCD Image Data
14	DATAIN4	I	CCD Image Data
15	V_{CC}	P	Power (+3.3V)
16	GND	P	GND
17	DATAIN3	I	CCD Image Data
18	DATAIN2	I	CCD Image Data
19	DATAIN1	I	CCD Image Data
20	DATAIN0	I	CCD Image Data (LSB)
21	CLPOB	O	Clamp Pulse Output for Optical Black
22	ADCLP	O	Clamp Pulse Output for ADC
23	PBLK	O	Blanking Pulse Output
24	SDA	B	EEPROM SDA for I2C Interface
25	GND	P	GND
26	V_{CC}	P	Power (+3.3V)
27	SCL	B	EEPROM SCL for I2C interface
28	GPIO_8	B	General Purpose I/O (I2C RDY)
29	INLL	B	Internal Sync/External Sync Selection
30	GPIO_0	B	General Purpose I/O (WB1)
31	GPIO_1	B	General Purpose I/O (WB2)

Pin	Symbol	I/O, P/G	Description
31	GPIO_1	B	General Purpose I/O (WB2)
32	GPIO_2	B	General Purpose I/O (MIR)
33	GPIO_3	B	General Purpose I/O (BLC)
34	GNDDA	P	AGND for Video DAC
35	V_{CC}	P	AV_{DD} for Video DAC
36	VDAC_REG	O	Regulator Output for Video DAC (VB)
37	VREF	O	REF for Video DAC (IREF)
38	NC		No Connection
39	GNDDA	P	Analog GND
40	Video	O	Analog Video Output
41	GPIO_4	B	General Purpose I/O (EEMDS)
42	GPIO_5	B	General Purpose I/O (EEMD1)
43	GPIO_6	B	General Purpose I/O (EEMD2)
44	GPIO_7	B	General Purpose I/O (EEMD3)
45	GND	P	GND
46	V_{CC}	P	Power (+3.3V)
47	DV_DCLK	O	Clock for Digital Output
48	TEST	I	TEST mode
49	VRI	I	Line Lock Signal Input (50/60Hz)
50	DVIO_0	B	DV I/O for Digital Output (Left Key)
51	DVIO_1	B	DV I/O for Digital Output (Right Key)
52	DVIO_2	B	DV I/O for Digital Output (Push Lock)
53	DVIO_3	B	DV I/O for Digital Output (LED)
54	GND	P	GND
55	V_{CC}	P	Power (+3.3V)
56	DVIO_4	B	DV I/O for Digital Output (ECLIPSE**)**
57	DVIO_5	B	DV I/O for Digital Output
58	DVIO_6	B	DV I/O for Digital Output
59	DVIO_7	B	DV I/O for Digital Output
60	HD	O	HSYNC for Digital Output

Pin	Symbol	I/O, P/G	Description
61	VD	O	VSYNC for Digital output
62	XV1	O	Vertical Shift Register Clock1
63	XV2	O	Vertical Shift Register Clock2
64	XV3	O	Vertical Shift Register Clock3
65	XV4	O	Vertical Shift Register Clock4
66	V_{CC}	P	Power (+3.3V)
67	GND	P	GND
68	XSG1	O	CCD Sensor Charge Readout Pulse Output TG1
69	XSG2	O	CCD Sensor Charge Readout Pulse Output TG2
70	XSUB	O	CCD Discharge Pulse Output
71	HV_{CC}	P	Power (+3.3V or +5V for H1, H2, RG)
72	HGND	P	GND
73	RG	O	Reset Gate Pulse Output
74	H1	O	H1 Clock Output for CCD Horizontal Register Drive
75	H2	O	H2 Clock Output for CCD Horizontal Register Drive
76	V_{CC}	P	Power (+3.3V)
77	GND	P	GND
78	AFE_CSN	O	AFE 3-Wire CSN
79	SHD	O	Data Sample and Hold Pulse
80	SHP	O	Pre Charge Level Sample and Hold Pulse

I : Input

O : Output

P : Power

B : Bi-direction

DSP REGISTER TABLE

ADDRESS	NAME	BIT	CONTENTS
00	STOP_EEPROM	7:0	Stop reading from EEPROM, only when EEPROM data is FF.
01	Reserved	7:0	
02 (1001h)	Reserved	1:0	
	CCD_H_DRV[1:0]	3:2	CCD_H1, CCD_H2 drive current When V_{CC}=3.3V 0:24mA,1:16mA, 2:7mA, 3:4mA When V_{CC}=5V 0:32mA, 1:21mA, 2:10mA, 3:6mA
	CCD_RG_DRV[1:0]	5:4	CCD_RG drive current When V_{CC}=3.3V 0: 24mA, 1:16mA, 2:7mA, 3:4mA When V_{CC}=5V 0:32mA, 1:21mA, 2:10mA, 3:6mA
	Reserved	7:6	
03 (1004h)	DV_MODE[2:0]	2:0	Digital video image out mode: 000: TG HSYNC/VSYNC output and DV_IO is at debug mode. if DVIO_O[0]=0 DV_IO={VRI_IN,VRI_REF,TV_VSYNC,TV_HSYNC, CLR_DSTB,AE_ACT,DEF_DSTB,OB_ACT} if DVIO_O[0]=1 DV_IO={VRI_IN,VRI_REF,TV_VSYNC,TV_HSYNC, CLR_DSTB,TV_ACT,CLR_HSYNC,CLR_VSYNC} 001: Sensor data output. (After defect/offset/gain For capture image) 010: Color data output. (After color → For capture image) 011: TV data output. (Before D/A → For connect to D/A) 100: TG HSYNC/VSYNC output and DV_IO is at GPIO mode. if DVIO_O[0]=0 ~ output TG_VSYNC with 180 Tsys_clk width if DVIO_O[0]=1 ~ output TG_VSYNC with 9 H line width 101: Sensor HSYNC/VSYNC output and DV_IO is at GPIO mode. 110: Color HSYNC/VSYNC output and DV_IO is at GPIO mode. 111: TV HSYNC/VSYNC output and DV_IO is at GPIO mode. if DVIO_O[0]=0 ~ TV HSYNC/VSYNC output if DVIO_O[0]=1 ~ CSYNC output from DV_VSYNC (DV_HSYNC is fixed to L)
	DV_EN	3	1: Enable digital image output.
	Reserved	7:4	

ADDRESS	NAME	BIT	CONTENTS
04 (1070h)	TV_TEST_Y[7:0]	7:0	Output Y when TV user defined color output mode. Note: (75% Amplitude YCbCr) White → TV_TEST_Y=BFh, TV_TEST_CB=80h, TV_TEST_CR=80h Yellow → TV_TEST_Y=AAh, TV_TEST_CB=20h, TV_TEST_CR=8Fh Cyan → TV_TEST_Y=86h, TV_TEST_CB=A0h, TV_TEST_CR=20h Green → TV_TEST_Y=70h, TV_TEST_CB=40h, TV_TEST_CR=2Fh Magenta → TV_TEST_Y=4Fh, TV_TEST_CB=BFh, TV_TEST_CR=D0h Red → TV_TEST_Y=39h, TV_TEST_CB=60h, TV_TEST_CR=E0h Blue → TV_TEST_Y=16h, TV_TEST_CB=E0h, TV_TEST_CR=9Bh Black → TV_TEST_Y=00h, TV_TEST_CB=80h, TV_TEST_CR=80h
05 (1071h)	TV_TEST_CB[7:0]	7:0	Output CB when TV user defined color output mode.
06 (1072h)	TV_TEST_CR[7:0]	7:0	Output CR when TV user defined color output mode.
07 (1066h)	TV_U_BURST[7:0]	7:0	Color burst level U for NTSC/PAL. (Format: Signed_bit+ data, Unit: 1 level for 9 bits D/A) Note: NTSC → bdh level. PAL → abh level.
08 (1067h)	TV_V_BURST[7:0]	7:0	Color burst level V for NTSC/PAL. (Format: Signed_bit+ data, Unit: 1 level for 9 bits D/A) Note: NTSC → 0h level. PAL → 2bh level.
09 (100Ch)	DVIO_O[7:0]	7:0	Output for PIN DVIO[7:0]
0A (100Dh)	DVIO_OE[7:0]	7:0	Output enable for PIN DVIO[7:0]
0B (100Eh)	GPIO_PUL_UP [7:0]	7:0	Pull up GPIO[7:0] input (high active)
0C	Reserved	7:0	
0D (1040h)	Reserved	0	
	VRI_RIS	1	0: Detect VRI at falling edge 1: Detect VRI at rising edge
	Reserved	6:2	
	VRI_DIV2	7	1: Select VRI divide 2
0E (1073h)	TV_W_CLIP[5:0]	5:0	White Clip Level
	Reserved	7:6	

ADDRESS	NAME	BIT	CONTENTS
0F (1074h)	TV_MONO[1:0]	1:0	TV color/mono display mode selection. 00:color display mode with color burst. 01:mono display mode with color burst. 10:color display mode without color burst 11:mono display mode without color burst
	Reserved	7:2	
10 (1048h)	LL_OFFSET [7:0]	7:0	Line lock offset reference to the VRI. (Unit: 512 Tsys_clk) Note: The maximum line lock offset for NTSC is 1/60s → LL_OFFSET = 932. The maximum line lock offset for PAL is 1/50s → LL_OFFSET = 1108.
11 (1049h)	LL_OFFSET [11:8]	3:0	
	Reserved	7:4	
12 (104Ah)	LL_LPF [1:0]	1:0	Line lock low pass filter. 00: line lock compensation per 1 frames 01: line lock compensation per 2 frames 1x: line lock compensation per 4 frames
	Reserved	7:2	
13 (00DCh)	TG_H_DLY	7:0	TG HSYNC delay reference from TV HSYNC
14 (00DDh)	TG_H_DLY_MIR	7:0	TG HSYNC delay reference from TV HSYNC (Mirror)
15 (1050h)	TV_PERIOD[7:0]	7:0	TV frame period when line lock function is disable. (Unit: Tsys_clk) Recommend: NTSC → 28.636MHz/29.97Hz = 955500 Tsys_clk. PAL → 28.375MHz/25Hz = 1135000 Tsys_clk.
16 (1051h)	TV_PERIOD[15:8]	7:0	
17 (1052h)	TV_PERIOD[20:16]	4:0	
	Reserved	7:5	
18 (1053h)	TG_V_DELAY[5:0]	5:0	TG VSYNC delay reference from TV VSYNC. (Unit: horizontal line)
	Reserved	7:6	
19	Reserved	7:0	
1A (1060h)	Reserved	4:0	
	V_DAC_EN	5	1: Enable video DAC.
	TV_SINC_EN	6	1: Enable sinc filter
	Reserved	7	
1B (1061h)	Reserved	0	
	TV_INV	1	1: Inverse video output

ADDRESS	NAME	BIT	CONTENTS
1B (1061h)	TV_PATTERN[2:0]	4:2	000: Normal image output. 001: Color bar output. 010: Triangle pattern 100: User defined color output. 110: User defined AC pattern output. 111: User defined grid pattern output. Others: Reserved
	Reserved	7:5	
1C (1062h)	TV_SETUP[6:0]	6:0	TV setup level for NTSC/PAL. (Unit: 2 level when 9 bits D/A) Note: NTSC → 48h level. PAL → 3ch level.
	Reserved	7	
1D (1063h)	TV_SYNC[6:0]	6:0	TV SYNC level for NTSC/PAL. (Unit: 2 level when 9 bits D/A) Note: NTSC → 3dh level. PAL → 3ch level.
	Reserved	7	
1E (1064h)	TV_Y_GAIN[6:0]	6:0	TV Y gain. (Gain = 0.5 + TV_Y_GAIN/128) Note: TV_Y_GAIN → 4ch
	Reserved	7	
1F (1065h)	TV_UV_GAIN[6:0]	6:0	TV UV gain. (Gain = 1 + TV_UV_GAIN/128)
	Reserved	7	
20 (1068h)	TV_H_START[7:0]	7:0	Horizontal active start pixel of each line. (Unit: 1 Tsys_clk) Note: NTSC → 0f7h. PAL → 0ffh.
21 (1069h)	TV_H_START[10:8]	2:0	
	Reserved	7:3	
22 (106Ah)	TV_V_START[7:0]	7:0	Vertical active start line of each field. (Unit: 1 Line) Note: NTSC → 012h. PAL → 017h.
23 (106Bh)	TV_V_START[8]	0	
	Reserved	7:1	
24 (106Ch)	TV_H_STOP[7:0]	7:0	Horizontal active stop pixel of each line. (Unit: 1 Tsys_clk) Note: NTSC → 6d4h. PAL → 6ebh.
25 (106Dh)	TV_H_STOP[10:8]	2:0	
	Reserved	7:3	

ADDRESS	NAME	BIT	CONTENTS
26 (106Eh)	TV_V_STOP[7:0]	7:0	Vertical active stop line of each field. (Unit: 1 Line) Note: NTSC → 103h. PAL → 135h.
27 (106Fh)	V_V_STOP[8]	0	
	Reserved	7:1	
28 (1080h)	CCD_SEL[1:0]	1:0	CCD Select: 00: NTSC 510X492 01: PAL 500X582 10: NTSC 768X494 11: PAL 752X582
	Reserved	5:2	
	TEST_IMG[1:0]	7:6	Test Image mode 00: Disable Test Image (normal mode) 01: Replace AFE image data to internal test Gray pattern. 10: White Image 11: Black Image
29 (1081h)	H_INV	0	H inverse. (1:inverted)
	RG_INV	1	RG inverse. (1:inverted)
	AD_LH_RIS	2	Data Latch with ADCLK edge. (0:falling edge 1:rising edge)
	Reserved	6:4	
	CCD_SEL	7	1: for A1PROs CCD
2A (1082h)	H1_DELAY[2:0]	2:0	H1 delay adjustment. (0-14ns delay)
	Reserved	3	
	H2_DELAY[2:0]	6:4	H2 delay adjustment. (0-14ns delay)
	Reserved	7	
2B (1083h)	RG_DELAY[3:0]	3:0	RG delay adjustment. (0-22ns delay)
	RG_WIDTH[2:0]	6:4	RG pulse width adjustment. (Decreasing 0-14ns)
	Reserved	7	
2C (1084h)	SHP_DELAY[3:0]	3:0	SHP delay adjustment. (0-22ns delay)
	SHP_WIDTH[2:0]	6:4	SHP pulse width adjustment. (Decreasing 0-14ns)
	Reserved	7	
2D (1085h)	SHD_DELAY[3:0]	3:0	SHD delay adjustment. (0-22ns delay)
	ADCLK_DELAY[3:0]	7:4	ADCLK delay. (0-22ns delay)
2E (1086h)	OBCLP_H_START[7:0]	7:0	Horizontal start for OBCLP. (Unit: 1 pixel)
2F (1087h)	OBCLP_H_START[9:8]	1:0	

ADDRESS	NAME	BIT	CONTENTS
2F (1087h)	Reserved	7:2	
30 (1088h)	OBCLP_H_STOP[7:0]	7:0	Horizontal stop for OBCLP. (Unit: 1 pixel) (Note: active region is not include stop pixel)
31 (1089h)	OBCLP_H_STOP[9:8]	1:0	
	Reserved	7:2	
32 (108Ah)	H_START[5:0]	5:0	Horizontal start pixel of each line. (Unit: 1 pixel)
	Reserved	7:6	
33 (108Bh)	V_START[3:0]	3:0	Vertical start line of each field. (Unit: 1 Line)
	Reserved	7:4	
34 (108Ch)	H_SIZE[7:0]	7:0	Horizontal size of each line. (Unit: 4 pixel)
35 (108Dh)	V_SIZE[7:0]	7:0	Vertical size of each field. (Unit: 2 Line)
36 (00DEh)	C_M11_MT[7:0]	7:0	C_M11 of Color matrix at middle color temperature.
37 (00DFh)	C_M12_MT[7:0]	7:0	C_M12 of Color matrix at middle color temperature.
38 (00E0h)	C_M13_MT[7:0]	7:0	C_M13 of Color matrix at middle color temperature.
39 (00E1h)	C_M21_MT[7:0]	7:0	C_M21 of Color matrix at middle color temperature.
3A (00E2h)	C_M22_MT[7:0]	7:0	C_M22 of Color matrix at middle color temperature.
3B (00E3h)	C_M23_MT[7:0]	7:0	C_M23 of Color matrix at middle color temperature.
3C (00E4h)	C_M31_MT[7:0]	7:0	C_M31 of Color matrix at middle color temperature.
3D (00E5h)	C_M32_MT[7:0]	7:0	C_M32 of Color matrix at middle color temperature.
3E (00E6h)	C_M33_MT[7:0]	7:0	C_M33 of Color matrix at middle color temperature.
3F (1098h)	ODD_OFFSET[7:0]	7:0	OFFSET compensation for ODD field. (Unit: 1 level at 8 bits) Note: It is sync with VSYNC.
40 (1099h)	EVEN_OFFSET[7:0]	7:0	OFFSET compensation for EVEN field. (Unit: 1 level at 8 bits) Note: It is sync with VSYNC.
41 (109Ah)	GLB_GAIN[4:0]	4:0	Global GAIN control → Gain = (1+GLB_GAIN/32) Note: It is sync with VSYNC.
	Reserved	7:5	

ADDRESS	NAME	BIT	CONTENTS
42	Reserved	7:0	
43 (10A4h)	AE_HB[5:0]	5:0	High band threshold for AE R, G, B histogram. (Unit: 4 level for 8 bits Y image data)
	Reserved	7:6	
44 (00ECh)	LOCK_R_GAIN	7:0	R Gain when Push Lock
45 (00EDh)	LOCK_G_GAIN	7:0	G Gain when Push Lock
46 (00EEh)	LOCK_B_GAIN	7:0	B Gain when Push Lock
47 (1125h)	HLS_THD[6:0]	6:0	High Luminance Suppress Threshold is a 2 level value. Threshold = 256 + HLS_THD[6:0] * 2. If Y ≧Threshold, Y will be suppressed to Eclipse level.
	Reserved	7	
48 (1126h)	ECLP_LVL[7:0]	7:0	Eclipse level = ECLP_LVL * 2
49 (1100h)	Reserved	0	
	AP_CTRL_EN	1	1: Enable Horizontal and Vertical aperture control.
	APKNEE_EN	2	1: Enable Aperture KNEE.
	AP_CORING_EN	3	1: Enable Aperture CORING.
	YHLPF_EN	4	1: Enable Y Horizontal Low-Pass filter.
	YGAMMA_EN	5	1: Enable Y Gamma.
	Y_LCRAWL_EN	6	1: Enable Line Crawl.
	AP_LPF_EN	7	1: Enable Aperture Low Pass Filter.
4A (1101h)	LCR_LDIF_THD	7:0	Line different threshold for Line Crawl Reduction.
4B (1102h)	LCR_HIGH_THD [7:0]	7:0	High threshold for Line Crawl Reduction
4C (1103h)	Reserved	6:0	
	HBPF_SEL	7	0: HBPF = (-1/4, 0, 1/2, 0, -1/4) 1: HBPF = (0, -1/4, 1/4, 1/4, -1/4)
4D	Reserved	7:0	
4E (1105h)	APKNEE_Y128	7:0	Y for APKNEE curve when X=128. Y= APKNEE_Y128 *2, Note: Y0=0.
4F (1106h)	APKNEE_Y256	7:0	Y for APKNEE curve when X=256. Y= APKNEE_Y256 *2
50 (1107h)	APKNEE_Y384	7:0	Y for APKNEE curve when X=384. Y= APKNEE_Y384 *2

ADDRESS	NAME	BIT	CONTENTS
51 (1108h)	APKNEE_Y512	7:0	Y for APKNEE curve when X=512. Y= APKNEE_Y512 *2
52 (1109h)	APKNEE_Y640	7:0	Y for APKNEE curve when X=640. Y= APKNEE_Y640 *2
53 (110Ah)	APKNEE_Y768	7:0	Y for APKNEE curve when X=768. Y= APKNEE_Y768 *2
54 (110Bh)	APKNEE_Y896	7:0	Y for APKNEE curve when X=896. Y= APKNEE_Y896 *2
55 (110Ch)	APKNEE_Y1024	7:0	Y for APKNEE curve when X=1024. Y= APKNEE_Y1024 *2
56 (110Dh)	AP_CORN[5:0]	5:0	Aperture corn control → Corn = AP_CORN * 2
	Reserved	7:6	
57 (110Eh)	AP_GAIN_P[3:0]	3:0	Global Aperture gain for positive AP → Gain= (AP_GAIN_P/4)
	AP_GAIN_N[3:0]	7:4	Global Aperture gain for negative AP → Gain= (AP_GAIN_N/4)
58 (110Fh)	Y_GAIN[4:0]	4:0	Y GAIN control → Gain = (1+Y_GAIN/32)
	Reserved	7:5	
59 (0082h)	GAM_Y0	7:0	Y when X=0. (BLC OFF)
5A (0083h)	GAM_Y32	7:0	Y when X=32. (BLC OFF)
5B (0084h)	GAM_Y64	7:0	Y when X=64. (BLC OFF)
5C (0085h)	GAM_Y96	7:0	Y when X=96. (BLC OFF)
5D (0086h)	GAM_Y128	7:0	Y when X=128. (BLC OFF)
5E (0087h)	GAM_Y160	7:0	Y when X=160. (BLC OFF)
5F (0088h)	GAM_Y192	7:0	Y when X=192. (BLC OFF)
60 (0089h)	GAM_Y224	7:0	Y when X=224. (BLC OFF)
61 (008Ah)	GAM_Y256	7:0	Y when X=256. (BLC OFF)
62 (008Bh)	GAM_Y320	7:0	Y when X=320. (BLC OFF)
63 (008Ch)	GAM_Y384	7:0	Y when X=384. (BLC OFF)
64 (008Dh)	GAM_Y448	7:0	Y when X=448. (BLC OFF)

ADDRESS	NAME	BIT	CONTENTS
65 (008Eh)	GAM_Y512	7:0	Y when X=512. (BLC OFF)
66 (008Fh)	GAM_Y576	7:0	Y when X=576. (BLC OFF)
67 (0090h)	GAM_Y640	7:0	Y when X=640. (BLC OFF)
68 (0091h)	GAM_Y704	7:0	Y when X=704. (BLC OFF)
69 (0092h)	GAM_Y768	7:0	Y when X=768. (BLC OFF)
6A (0093h)	GAM_Y832	7:0	Y when X=832. (BLC OFF)
6B (0094h)	GAM_Y896	7:0	Y when X=896. (BLC OFF)
6C (0095h)	GAM_Y960	7:0	Y when X=960. (BLC OFF)
6D (0096h)	GAM_Y1024	7:0	Y when X=1024. (BLC OFF)
6E (1128h)	CLPF_EN	0	Color low-pass filter enable
	ITP_EN	1	Interpolation enable
	CLR_MTX_EN	2	Color matrix enable
	RGB_GAMMA_EN	3	RGB gamma enable
	LINER_MTX_EN	4	Liner matrix enable
	YH_SPRS_EN	5	YH color suppress enable
	AP_SPRS_EN	6	Aperture color suppress enable
	Reserved	7	
6F	Reserved	7:0	
70 (00E7h)	MT_LB_RGAIN[7:0]	7:0	Middle color temp low bound R Gain
71 (00E8h)	MT_LB_BGAIN[7:0]	7:0	Middle color temp low bound B Gain
72 (00E9h)	LT_HB_RGAIN[7:0]	7:0	Low color temp high bound R Gain
73 (00EAh)	LT_HB_BGAIN[7:0]	7:0	Low color temp high bound B Gain
74	Reserved	7:0	
75	Reserved	7:0	
76	Reserved	7:0	

ADDRESS	NAME	BIT	CONTENTS
77	Reserved	7:0	
78 (1132h)	OFFSET_R	7:0	R offset for Color matrix. OFFSET_R is a signed value.
79 (1133h)	OFFSET_B	7:0	B offset for Color matrix. OFFSET_B is a signed value.
7A	Reserved	7:0	
7B	Reserved	7:0	
7C	Reserved	7:0	
7D (1138h)	RGB_GAMMA_Y0	7:0	Y for RGB gamma when X=0. Y = RGB_GAMMA_Y0 *2
7E (1139h)	RGB_GAMMA_Y32	7:0	Y for RGB gamma when X=32. Y = RGB_GAMMA_ Y32 *2
7F (113Ah)	RGB_GAMMA_Y64	7:0	Y for RGB gamma when X=64. Y = RGB_GAMMA_Y64 *2
80 (113Bh)	RGB_GAMMA_Y96	7:0	Y for RGB gamma when X=96. Y = RGB_GAMMA_Y96 *2
81 (113Ch)	RGB_GAMMA_Y12	7:0	Y for RGB gamma when X=128. Y = RGB_GAMMA_Y128 *2
82 (113Dh)	RGB_GAMMA_Y160	7:0	Y for RGB gamma when X=160. Y = RGB_GAMMA_Y160 *2
83 (113Eh)	RGB_GAMMA_Y192	7:0	Y for RGB gamma when X=192. Y = RGB_GAMMA_Y192 *2
84 (113Fh)	RGB_GAMMA_Y224	7:0	Y for RGB gamma when X=224. Y = RGB_GAMMA_Y224 *2
85 (1140h)	RGB_GAMMA_Y256	7:0	Y for RGB gamma when X=256. Y = RGB_GAMMA_Y256 *2
86 (1141h)	RGB_GAMMA_Y320	7:0	Y for RGB gamma when X=320. Y = RGB_GAMMA_Y320 *2
87 (1142h)	RGB_GAMMA_Y384	7:0	Y for RGB gamma when X=384. Y = RGB_GAMMA_Y384 *2
88 (1143h)	RGB_GAMMA_Y448	7:0	Y for RGB gamma when X=448. Y = RGB_GAMMA_Y448 *2
89 (1144h)	RGB_GAMMA_Y512	7:0	Y for RGB gamma when X=512. Y = RGB_GAMMA_Y512 *2
8A (1145h)	RGB_GAMMA_Y576	7:0	Y for RGB gamma when X=576. Y = RGB_GAMMA_Y576 *2
8B (1146h)	RGB_GAMMA_Y640	7:0	Y for RGB gamma when X=640. Y = RGB_GAMMA_Y640 *2
8C (1147h)	RGB_GAMMA_Y704	7:0	Y for RGB gamma when X=704. Y = RGB_GAMMA_Y704*2

ADDRESS	NAME	BIT	CONTENTS
8D (1148h)	RGB_GAMMA_Y768	7:0	Y for RGB gamma when X=768. Y = RGB_GAMMA_Y768 *2
8E (1149h)	RGB_GAMMA_Y832	7:0	Y for RGB gamma when X=832. Y = RGB_GAMMA_Y832 *2
8F (114Ah)	RGB_GAMMA_Y896	7:0	Y for RGB gamma when X=896. Y = RGB_GAMMA_Y896 *2
90 (114Bh)	RGB_GAMMA_Y960	7:0	Y for RGB gamma when X=960. Y = RGB_GAMMA_Y960 *2
91 (114Ch)	RGB_GAMMA_Y1024	7:0	Y for RGB gamma when X=1024. Y = RGB_GAMMA_Y1024 *2 +1 Note: Y1024≧Y960≧Y896≧Y832≧Y768≧Y704≧Y640≧Y576 ≧Y512≧Y448≧Y384≧Y320≧Y256≧Y224≧Y192≧Y160 ≧Y128≧Y96≧Y64≧Y32≧Y0.
92 (0076h)	L_M21_HT[7:0]	7:0	L_M21 of Liner matrix at High temperature. A signed value.
93 (0077h)	L_M21_HT[9:8]	1:0	
	Reserved	7:2	
94 (0078h)	L_M22_HT[7:0]	7:0	L_M22 of Liner matrix at High temperature. A signed value.
95 (0079h)	L_M22_HT[9:8]	1:0	
	Reserved	7:2	
96 (007Ah)	L_M23_HT[7:0]	7:0	L_M23 of Liner matrix at High temperature. A signed value.
97 (007Bh)	L_M23_HT[9:8]	1:0	
	Reserved	7:2	
98 (007Ch)	L_M31_HT[7:0]	7:0	L_M31 of Liner matrix at High temperature. A signed value.
99 (007Dh)	L_M31_HT[9:8]	1:0	
	Reserved	7:2	
9A (007Eh)	L_M32_HT[7:0]	7:0	L_M32 of Liner matrix at High temperature. A signed value.
9B (007Fh)	L_M32_HT[9:8]	1:0	
	Reserved	7:2	
9C (0080h)	L_M33_HT[7:0]	7:0	L_M33 of Liner matrix at High temperature. A signed value.
9D (0081h)	L_M33_HT[9:8]	1:0	
	Reserved	7:2	

ADDRESS	NAME	BIT	CONTENTS
9E (1159h)	LY_SPRS_START	7:0	Color suppress start level for low luminance.
9F (115Ah)	LY_SPRS_SLOPE	4:0	Color suppress slope for low luminance.
	Reserved	7:5	
A0 (115Bh)	HY_SPRS_START	7:0	Color suppress start level for high luminance.
A1 (115Ch)	HY_SPRS_SLOPE	4:0	Color suppress slope for high luminance.
	Reserved	7:5	
A2 (115Dh)	AP_SPRS_START	5:0	Color suppress start level for aperture.
	Reserved	7:6	
A3 (115Eh)	AP_SPRS_SLOPE	3:0	Color suppress slope for aperture.
	Reserved	7:4	
A4 (115Fh)	U_SLICE	3:0	Slice = U_SLICE * 2
	V_SLICE	7:4	Slice = V_SLICE * 2
A5 (1161h)	Y_MAX[5:0]	5:0	Maximum Y for AWB report. (Unit: 4 level for 8 bits image data)
	Reserved	7:6	
A6 (1162h)	Y_MIN[5:0]	5:0	Minimum Y for AWB report. (Unit: 4 level for 8 bits image data)
	Reserved	7:6	
A7 (1163h)	C_MAX[7:0]	7:0	Maximum C for AWB report. (Unit: 16 level for 7 bits image data) Note : C_MIN ≦(U2 + V2) < C_MAX
A8 (1164h)	C_MAX[9:8]	1:0	
	Reserved	7:2	
A9 (1165h)	C_MIN[7:0]	7:0	Minimum C for AWB report. (Unit: 4 level for 7 bits image data)
AA (1166h)	UV_plane[3:0]	3:0	UV_plane region enable select for AWB report. UV_plane[0] : 0: region 1 disable. 1: region 1 enable. UV_plane[1] : 0: region 2 disable. 1: region 2 enable. UV_plane[2] : 0: region 3 disable. 1: region 3 enable. UV_plane[3] : 0: region 4 disable. 1: region 4 enable.
	Reserved	7:4	

ADDRESS	NAME	BIT	CONTENTS
AB (1167h)	UV_SIN[5:0]	5:0	SIN value for IQ transform. (Format: Unsigned, Value=UV_SIN/64) Note: I = -U*SIN + V*COS, Q = U*COS + V*SIN
	Reserved	7:6	
AC (1168h)	UV_COS[5:0]	5:0	COS value for IQ transform. (Format: Unsigned, Value=UV_COS/64)
	Reserved	7:6	
AD (1169h)	I0_MAX	7:0	{(I0_MAX, I0_MIN),(Q0_MAX,Q0_MIN)} for AWB IQ windows 0 report. (Format: signed, 1 level for 8 bits limited signed image data.)
AE (116Ah)	I0_MIN	7:0	
AF (116Bh)	Q0_MAX	7:0	
B0 (116Ch)	Q0_MIN	7:0	
B1 (003Bh)	H_Y_AWB_STOP	3:0	Upper limit of Ysum of AWB Upper limit = H_Y_AWB_STOP * 1024
	L_Y_AWB_STOP	7:4	Lower limit of Ysum of AWB Lower limit = L_Y_AWB_STOP * 256 AWB is active when (Upper limit > Lower limit), otherwise stop AWB
B2	Reserved	7:0	
B3	Reserved	7:0	
B4	Reserved	7:0	
B5	Reserved	7:0	
B6	Reserved	7:0	
B7	Reserved	7:0	
B8	Reserved	7:0	
B9	Reserved	7:0	
BA (1180h)	RS_MODE	0	0:GPIO, 1:RS232 mode
	RS_STOP_BIT	1	RS232 stop bit number selection. (0 → 1 bits, 1 → 2 bits)
	Reserved	7:2	

ADDRESS	NAME	BIT	CONTENTS
BB (0000h)	WB_MODE[1:0]	1:0	White balance mode 00: Auto 01: WB1 (3100^{o}K) 10: WB2 (5100^{o}K) 11: WB3 (6500^{o}K)
	MIR	2	Mirror 0: Disable 1: Enable
	BLC	3	Back light compensation 0: Disable 1: Enable
	SHUTTER_MODE[4:0]	7:4	Shutter speed select 0000: 1/60s (1/50s) 0001: 1/120s (1/100s) 0010: 1/250s 0011: 1/500s 0100: 1/1000s 0101: 1/2000s 0110: 1/5000s 0111: 1/10000s 1000: 1/20000s 1001: 1/50000s 1010: 1/100000s 1011: Auto 1100: Auto 1101: Auto 1110: Auto 1111: Auto
BC (0001h)	MCRDIP	0	1: Enable microcontroller DIP switch scan
	FLKLESS	1	1: Enable flickless
	AGC_OFF	2	AGC control, 0:ON, 1:OFF
	INIT_SHUTTER_FLAG	3	Initial shutter speed at power on, 0: Min shutter speed, 1: Max shutter speed
	AE_SPEED[2:0]	6:4	Speed of AE control operation 000: Per 1 frames 001: Per 2 frames 010: Per 4 frames 011: Per 8 frames 100: Per 12 frames
	AE_STOP	7	Stop AE_Control
BD (0002h)	YSUM_TGT[15:8]	7:0	Target Y value when auto exposure (BLC OFF)
BE (0003h)	YSUM_TGT[7:0]	7:0	

ADDRESS	NAME	BIT	CONTENTS
BF (0004h)	BLC_YSUM_TGT[15:8]	7:0	Target Y value when auto exposure (BLC ON)
C0 (0005h)	BLC_YSUM_TGT[7:0]	7:0	
C1 (0006h)	AE_STEP_SIZE[4:0]	4:0	AE step size (12~31)
	ADCK_INV	5	Ai4100 0: Normal ADCK Operation 1: ADCK clock inversion AD9943 0: ADCK active low 1: ADCK active high
	MON_SEL[1:0]	7:6	Monitor selection (Only for Ai4100) 00: Monitor OFF 01: CDS signal to monitor 10: PGA output monitor 11: Output REFIN and CCDIN (for calibration)
C2 (0007h)	MAX_SH[3:0]	3:0	Maximum shutter speed (When SHUTTER_MODE = Auto)
	MIN_SH_SEL	4	Select minimum shutter speed, 0: 1/60(1/50) 1: 1/120(1/100)
	AFE_CDS_GAIN[1:0]	6:5	AFE CDS gain select, 00:0dB, 01:6dB, 10:12dB, 11:-2dB (Only for Ai4100)
	AFE_SEL	7	0 : Ai4100 , 1 : AD9943
C3 (0008h)	AE_STA_RANGE[7:0]	7:0	Stable range at auto exposure
C4 (0009h)	AE_OSC_RANGE[7:0]	7:0	Oscillation range at auto exposure
C5 (000Ah)	MAX_AFE_GAIN[7:0]	7:0	Max AFE analog gain when AGC
C7 (000Ch)	FIX_GAIN[7:0]	7:0	Gain value when AGC off
C8 (000Dh)	AFE_OFFSET[7:0]	7:0	AFE offset value when fixed Ai4100 : 0 ~127 AD9943 : 0 ~ 255
C9 (000Eh)	AWB1_R_GAIN [7:0]	7:0	R gain for AWB1(3100°K) adjustment. GAIN=(R_GAIN/64)
CA (000Fh)	AWB1_G_GAIN [7:0]	7:0	G gain for AWB1(3100°K) adjustment. GAIN=(G_GAIN/64)
CB (0010h)	AWB1_B_GAIN [7:0]	7:0	B gain for AWB1(3100°K) adjustment. GAIN=(B_GAIN/64)

ADDRESS	NAME	BIT	CONTENTS
CC (0011h)	AWB2_R_GAIN [7:0]	7:0	R gain for AWB2(5100°K) adjustment. GAIN=(R_GAIN/64)
CD (0012h)	AWB2_G_GAIN [7:0]	7:0	G gain for AWB2(5100°K) adjustment. GAIN=(G_GAIN/64)
CE (0013h)	AWB2_B_GAIN [7:0]	7:0	B gain for AWB2(5100°K) adjustment. GAIN=(B_GAIN/64)
CF (0014h)	AWB3_R_GAIN [7:0]	7:0	R gain for AWB3(6500°K) adjustment. GAIN=(R_GAIN/64)
D0 (0015h)	AWB3_G_GAIN [7:0]	7:0	G gain for AWB3(6500°K) adjustment. GAIN=(G_GAIN/64)
D1 (0016h)	AWB3_B_GAIN [7:0]	7:0	B gain for AWB3(6500°K) adjustment. GAIN=(B_GAIN/64)
D2 (0017h)	COL_S [7:0]	7:0	Start point of low luminance color suppression (AGC gain).
D3 (0018h)	COL_E [7:0]	7:0	End point of low luminance color suppression (AGC gain)
D4 (0019h)	APT_S [7:0]	7:0	Start point of edge signal suppression curve (AGC gain)
D5 (001Ah)	APT_H [5:0]	5:0	Slope of edge signal suppression curve (AGC gain)
	Reserved	6	
	PBLKLVL	7	0: Blank out to zero 1: Blank to ob-clamp level (Only for AD9943)
D6 (001Bh)	AP_HGA [4:0]	4:0	Initial value of APT_HGA (gain of horizontal edge signal)
	AWB_SPEED[1:0]	6:5	Speed of AWB Control 00: per 1 frame 01: per 2 frame 10: per 4 frame 11: per 8 frame
	AWB_LOCK	7	0: Unlock 1: Locked
D7 (001Ch)	AP_VGA [4:0]	4:0	Initial value of APT_VGA (gain of vertical edge signal)
	AWB_STEPSIZE[2:0]	7:5	AWB Step Size
D8 (001Dh)	W0 [3:0]	3:0	Y Sum weight at window 0 when BLC Off
	BLC_W0 [3:0]	7:4	Y Sum weight at window 0 when BLC On
D9 (001Eh)	W1 [3:0]	3:0	Y Sum weight at window 1 when BLC Off
	BLC_W1 [3:0]	7:4	Y Sum weight at window 1 when BLC On
DA (001Fh)	W2 [3:0]	3:0	Y Sum weight at window 2 when BLC Off
	BLC_W2 [3:0]	7:4	Y Sum weight at window 2 when BLC On

ADDRESS	NAME	BIT	CONTENTS
DA (001Fh)	W2 [3:0]	3:0	Y Sum weight at window 2 when BLC Off
	BLC_W2 [3:0]	7:4	Y Sum weight at window 2 when BLC On
DB (0020h)	W3 [3:0]	3:0	Y Sum weight at window 3 when BLC Off
	BLC_W3 [3:0]	7:4	Y Sum weight at window 3 when BLC On
DC (0021h)	W4 [3:0]	3:0	Y Sum weight at window 4 when BLC Off
	BLC_W4 [3:0]	7:4	Y Sum weight at window 4 when BLC On
DD (0022h)	W5 [3:0]	3:0	Y Sum weight at window 5 when BLC Off
	BLC_W5 [3:0]	7:4	Y Sum weight at window 5 when BLC On
DE (0023h)	W6 [3:0]	3:0	Y Sum weight at window 6 when BLC Off
	BLC_W6 [3:0]	7:4	Y Sum weight at window 6 when BLC On
DF (0024h)	W7 [3:0]	3:0	Y Sum weight at window 7 when BLC Off
	BLC_W7 [3:0]	7:4	Y Sum weight at window 7 when BLC On
E0 (0025h)	W8 [3:0]	3:0	Y Sum weight at window 8 when BLC Off
	BLC_W8 [3:0]	7:4	Y Sum weight at window 8 when BLC On
E1 (0026h)	W9 [3:0]	3:0	Y Sum weight at window 9 when BLC Off
	BLC_W9 [3:0]	7:4	Y Sum weight at window 9 when BLC On
E2 (0027h)	W10 [3:0]	3:0	Y Sum weight at window 10 when BLC Off
	BLC_W10 [3:0]	7:4	Y Sum weight at window 10 when BLC On
E3 (0028h)	YSUM_W22 [3:0]	3:0	Y Sum weight at window 11 when BLC Off
	YSUM_W23 [3:0]	7:4	Y Sum weight at window 11 when BLC On
E4 (0029h)	YSUM_W24 [3:0]	3:0	Y Sum weight at window 12 when BLC Off
	BLC_YSUM_W0 [3:0]	7:4	Y Sum weight at window 12 when BLC On
E5 (002Ah)	BLC_YSUM_W1 [3:0]	3:0	Y Sum weight at window 13 when BLC Off
	BLC_YSUM_W2 [3:0]	7:4	Y Sum weight at window 13 when BLC On
E6 (002Bh)	W14 [3:0]	3:0	Y Sum weight at window 14 when BLC Off
	BLC_W14 [3:0]	7:4	Y Sum weight at window 14 when BLC On
E7 (002Ch)	W15 [3:0]	3:0	Y Sum weight at window 15 when BLC Off
	BLC_W15 [3:0]	7:4	Y Sum weight at window 15 when BLC On
E8 (002Dh)	W16 [3:0]	3:0	Y Sum weight at window 16 when BLC Off
	BLC_W16 [3:0]	7:4	Y Sum weight at window 16 when BLC On

ADDRESS	NAME	BIT	CONTENTS
E9 (002Eh)	W17 [3:0]	3:0	Y Sum weight at window 17 when BLC Off
	BLC_W17 [3:0]	7:4	Y Sum weight at window 17 when BLC On
EA (002Fh)	W18 [3:0]	3:0	Y Sum weight at window 18 when BLC Off
	BLC_W18 [3:0]	7:4	Y Sum weight at window 18 when BLC On
EB (0030h)	W19 [3:0]	3:0	Y Sum weight at window 19 when BLC Off
	BLC_W19 [3:0]	7:4	Y Sum weight at window 19 when BLC On
EC (0031h)	W20 [3:0]	3:0	Y Sum weight at window 20 when BLC Off
	BLC_W20 [3:0]	7:4	Y Sum weight at window 20 when BLC On
ED (0032h)	W21 [3:0]	3:0	Y Sum weight at window 21 when BLC Off
	BLC_W21 [3:0]	7:4	Y Sum weight at window 21 when BLC On
EE (0033h)	W22 [3:0]	3:0	Y Sum weight at window 22 when BLC Off
	BLC_W22 [3:0]	7:4	Y Sum weight at window 22 when BLC On
EF (0034h)	W23 [3:0]	3:0	Y Sum weight at window 23 when BLC Off
	BLC_W23 [3:0]	7:4	Y Sum weight at window 23 when BLC On
F0 (0035h)	W24 [3:0]	3:0	Y Sum weight at window 24 when BLC Off
	BLC_YSUM_W24 [3:0]	7:4	Y Sum weight at window 24 when BLC On
F1 (0036h)	BY_ORITNT [7:0]	7:0	U direct shift value of orientation on UV plane
F2 (0037h)	RY_ORITNT [7:0]	7:0	V direct shift value of orientation on UV plane
F3 (0038h)	COL_M [4:0]	4:0	Min suppress gain of low luminance color suppression (AGC gain)
	Reserved	5	
	LOCK_STATE	7:6	AWB Lock state 01: High color temp 10: Middle color temp 11: Low color temp
F4 (0039h)	PRE_R_GAIN [7:0]	7:0	Pre-R gain for AWB
F5 (003Ah)	PRE_B_GAIN [7:0]	7:0	Pre-B gain for AWB
F6 (1181h)	RS_RATE [4:0]	4:0	RS232 transition rate. (Speed=115200/RS_RATE bps)
	Reserved	7:5	

ADDRESS	NAME	BIT	CONTENTS
F7 (0101h)	Y_MIN_CNT[15;8]	7:0	Minimum Y count
F8 (0102h)	PRINT_FLAG [7:0]	7:0	
F9 (003Dh)	LL_STEP_SIZE [7:0]	7:0	Step size of line-lock comp
FA (003Eh)	LL_FREQ_MAX [3:0]	3:0	Maximum Line-Lock frequency 1/60 (1/50) – (LL_FREQ_MAX * 2048 Tsys_clk)
	LL_FREQ_MIN [3:0]	7:4	Minimum Line-Lock frequency 1/60 (1/50) + (LL_FREQ_MIN * 2048 Tsys_clk)
FB (003Fh)	HLS_MODE [1:0]	1:0	High Light suppression mode. (switch data at AE,Y) 0: Disable 1: AE switch on. 2: Y switch on. 3: AE, Y switch on. (Active while MCRDIP = 1 or HLI_EN = 'H')
	AWB_RANGE	4:2	000: 2500^{o}K~9500^{o}K 001: 3100^{o}K~5100^{o}K 010: 3100^{o}K~6500^{o}K 011: 2800^{o}K~4700^{o}K 100: 2500^{o}K~15000^{o}K
	Reserved	7:5	
FC~FF	Reserved	7:0	
100 (0040h)	C_M11_LT[7:0]	7:0	C_M11 of color matrix at low color temperature.
101 (0041h)	C_M12_LT[7:0]	7:0	C_M12 of color matrix at low color temperature.
102 (0042h)	C_M13_LT[7:0]	7:0	C_M13 of color matrix at low color temperature.
103 (0043h)	C_M21_LT[7:0]	7:0	C_M21 of color matrix at low color temperature.
104 (0044h)	C_M22_LT[7:0]	7:0	C_M22 of color matrix at low color temperature.
105 (0045h)	C_M23_LT[7:0]	7:0	C_M23 of color matrix at low color temperature.
106 (0046h)	C_M31_LT[7:0]	7:0	C_M31 of color matrix at low color temperature.
107 (0047h)	C_M32_LT[7:0]	7:0	C_M32 of color matrix at low color temperature.
108 (0048h)	C_M33_LT[7:0]	7:0	C_M33 of color matrix at low color temperature.

ADDRESS	NAME	BIT	CONTENTS
109 (0049h)	C_M11_LT[7:0]	7:0	C_M11 of color matrix at high color temperature.
10A (004Ah)	C_M12_LT[7:0]	7:0	C_M12 of color matrix at high color temperature.
10B (004Bh)	C_M13_LT[7:0]	7:0	C_M13 of color matrix at high color temperature.
10C (004Ch)	C_M21_HT[7:0]	7:0	C_M21 of Color Matrix at high color temperature.
10D (004Dh)	C_M22_HT[7:0]	7:0	C_M22 of Color Matrix at high color temperature.
10E (004Eh)	C_M23_HT[7:0]	7:0	C_M23 of Color Matrix at high color temperature.
10F (004Fh)	C_M31_HT[7:0]	7:0	C_M31 of Color Matrix at high color temperature.
110 (0050h)	C_M32_HT[7:0]	7:0	C_M32 of Color Matrix at high color temperature.
111 (0051h)	C_M33_HT[7:0]	7:0	C_M33 of Color Matrix at high color temperature.
112 (0052h)	L_M21_LT[7:0]	7:0	L_M21 of Liner matrix at Low temperature. A signed value.
113 (0053h)	L_M21_LT[9:8]	1:0	
	Reserved	7:2	
114 (0054h)	L_M22_LT[7:0]	7:0	L_M22 of Liner matrix at Low temperature. A signed value.
115 (0055h)	L_M22_LT[7:0]	7:0	
	Reserved		
116 (0056h)	L_M23_LT[7:0]	7:0	L_M23 of Liner matrix at Low temperature. A signed value.
117 (0057h)	L_M23_LT[9:8]	1:0	
	Reserved	7:2	
118 (0058h)	L_M31_LT[7:0]	7:0	L_M31 of Liner matrix at Low temperature. A signed value.
119 (0059h)	L_M31_LT[9:8]	1:0	
	Reserved	7:2	
11A (005Ah)	L_M32_LT[7:0]	7:0	L_M32 of Liner matrix at Low temperature. A signed value.
11B (005Bh)	L_M32_LT[9:8]	1:0	
	Reserved	7:2	

ADDRESS	NAME	BIT	CONTENTS
11C (005Ch)	L_M33_LT[7:0]	7:0	L_M33 of Liner matrix at Low temperature. A signed value.
11D (005Dh)	L_M33_LT[9:8]	1:0	
	Reserved	7:2	
11E (005Eh)	AWBRAG1_RMA[7:0]	7:0	Max R Gain for AWB Range 1
11F (005Fh)	AWBRAG1_RMI[7:0]	7:0	Max R Gain for AWB Range 1
120 (0060h)	AWBRAG1_BMA[7:0]	7:0	Max B Gain for AWB Range 1
121 (0061h)	AWBRAG1_BMI[7:0]	7:0	Max B Gain for AWB Range 1
122 (0062h)	AWBRAG2_RMA[7:0]	7:0	Max R Gain for AWB Range 2
123 (0063h)	AWBRAG2_RMI[7:0]	7:0	Max R Gain for AWB Range 2
124 (0064h)	AWBRAG2_BMA[7:0]	7:0	Max B Gain for AWB Range 2
125 (0065h)	AWBRAG2_BMI[7:0]	7:0	Max B Gain for AWB Range 2
126 (0066h)	AWBRAG3_RMA[7:0]	7:0	Max R Gain for AWB Range 3
127 (0067h)	AWBRAG3_RMI[7:0]	7:0	Min R Gain for AWB Range 3
128 (0068h)	AWBRAG3_BMA[7:0]	7:0	Max B Gain for AWB Range 3
129 (0069h)	AWBRAG3_BMI[7:0]	7:0	Min B Gain for AWB Range 3
12A (006Ah)	AWBRAG4_RMA[7:0]	7:0	Max R Gain for AWB Range 4
12B (006Bh)	AWBRAG4_RMI[7:0]	7:0	Max R Gain for AWB Range 4
12C (006Ch)	AWBRAG4_BMA[7:0]	7:0	Max B Gain for AWB Range 4
12D (006Dh)	AWBRAG4_BMI[7:0]	7:0	Max B Gain for AWB Range 4
12E (006Eh)	AWBRAG5_RMA[7:0]	7:0	Max R Gain for AWB Range 5
12F (006Fh)	AWBRAG5_RMI[7:0]	7:0	Max R Gain for AWB Range 5

ADDRESS	NAME	BIT	CONTENTS
130 (0070h)	AWBRAG5_BMA[7:0]	7:0	Max B Gain for AWB Range 5
131 (0071h)	AWBRAG5_BMI[7:0]	7:0	Max B Gain for AWB Range 5
132 (0072h)	HT_LB_RGAIN[7:0]	7:0	High color temp low bound R Gain
133 (0073h)	HT_LB_BGAIN[7:0]	7:0	High color temp low bound B Gain
134 (0074h)	MT_LB_RGAIN[7:0]	7:0	Middle color temp high bound R Gain
135 (0075h)	MT_LB_BGAIN[7:0]	7:0	Middle color temp high bound B Gain
136 (0097h)	BLC_GAM_Y0	7:0	Y when X=0. (BLC ON)
137 (0098h)	BLC_GAM_Y32	7:0	Y when X=32. (BLC ON)
138 (0099h)	BLC_GAM_Y64	7:0	Y when X=64. (BLC ON)
139 (009Ah)	BLC_GAM_Y96	7:0	Y when X=96. (BLC ON)
13A (009Bh)	BLC_GAM_Y128	7:0	Y when X=128. (BLC ON)
13B (009Ch)	BLC_GAM_Y160	7:0	Y when X=160. (BLC ON)
13C (009Dh)	BLC_GAM_Y192	7:0	Y when X=192. (BLC ON)
13D (009Eh)	BLC_GAM_Y224	7:0	Y when X=224. (BLC ON)
13E(009Fh)	BLC_GAM_Y256	7:0	Y when X=256. (BLC ON)
13F (00A0)	BLC_GAM_Y320	7:0	Y when X=320. (BLC ON)
140 (00A1h)	BLC_GAM_Y384	7:0	Y when X=384. (BLC ON)
141 (00A2h)	BLC_GAM_Y448	7:0	Y when X=448. (BLC ON)
142 (00A3h)	BLC_GAM_Y512	7:0	Y when X=512. (BLC ON)
143 (00A4h)	BLC_GAM_Y576	7:0	Y when X=576. (BLC ON)
144 (00A5h)	BLC_GAM_Y640	7:0	Y when X=640. (BLC ON)

ADDRESS	NAME	BIT	CONTENTS
145 (00A6h)	BLC_GAM_Y704	7:0	Y when X=704. (BLC ON)
146 (00A7h)	BLC_GAM_Y768	7:0	Y when X=768. (BLC ON).
147 (00A8h)	BLC_GAM_Y832	7:0	Y when X=832. (BLC ON)
148 (00A9h)	BLC_GAM_Y896	7:0	Y when X=896. (BLC ON)
149 (00AAh)	BLC_GAM_Y960	7:0	Y when X=960. (BLC ON)
14A (00ABh)	BLC_GAM_Y1024	7:0	Y when X=1024. (BLC ON)
14B (00ACh)	G0_ADR_1[7:0]	7:0	GPIO0 Mapping Address 1, If Address = 0x00 -> Disable
14C (00ADh)	G0_ADR_1[8]	0	
	G0_STABIT_1[2:0]	3:1	GPIO0 Mapping Start Bit 1 (0~7)
	Reserved	4	
	AWB_GAP	7:5	Gap between each color temp
14D (00AEh)	G0_ADR_2[7:0]	7:0	GPIO0 Mapping Address 2, If Address = 0x00 -> Disable
14E (00AFh)	G0_ADR_2[8]	0	
	G0_STABIT_2[2:0]	3:1	GPIO0 Mapping Start Bit 2 (0~7)
	G0_BITNUM_2[3:0]	7:4	GPIO0 Mapping Bit Num 2 (1~8)
14F (00B0h)	G0_ADR_1[7:0]	7:0	GPIO1 Mapping Address 1, If Address = 0x00 -> Disable
150 (00B1h)	G0_ADR_1[8]	0	
	G0_STABIT_1[2:0]	3:1	GPIO1 Mapping Start Bit 1 (0~7)
	Reserved	7:4	
151 (00B2h)	G1_ADR_2[7:0]	7:0	GPIO1 Mapping Address 2, If Address = 0x00 -> Disable
152 (00B3h)	G1_ADR_2[8]	0	
	G1_STABIT_2[2:0]	3:1	GPIO1 Mapping Start Bit 2 (0~7)
	G1_BITNUM_2[3:0]	7:4	GPIO1 Mapping Bit Num 2 (1~8)

ADDRESS	NAME	BIT	CONTENTS
153 (00B4h)	G2_ADR_1[7:0]	7:0	GPIO2 Mapping Address 1, If Address = 0x00 -> Disable
154 (00B5h)	G2_ADR_1[8]	0	
	G2_STABIT_1[2:0]	3:1	GPIO2 Mapping Start Bit 1 (0~7)
	Reserved	7:4	
155 (00B6h)	G2_ADR_2[7:0]	7:0	GPIO2 Mapping Address 2, If Address = 0x00 -> Disable
156 (00B7h)	G2_ADR_2[8]	0	
	G2_STABIT_2[2:0]	3:1	GPIO2 Mapping Start Bit 2 (0~7)
	G2_BITNUM_2[3:0]	7:4	GPIO2 Mapping Bit Num 2 (1~8)
157 (00B8h)	G3_ADR_1[7:0]	7:0	GPIO3 Mapping Address 1, If Address = 0x00 -> Disable
158 (00B9h)	G3_ADR_1[8]	0	
	G3_STABIT_1[2:0]	3:1	GPIO3 Mapping Start Bit 1 (0~7)
	Reserved	7:4	
159 (00BAh)	G3_ADR_2[7:0]	7:0	GPIO3 Mapping Address 2, If Address = 0x00 -> Disable
15A (00BBh)	G3_ADR_2[8]	0	
	G3_STABIT_2[2:0]	3:1	GPIO3 Mapping Start Bit 2 (0~7)
	G3_BITNUM_2[3:0]	7:4	GPIO3 Mapping Bit Num 2 (1~8)
15B (00BCh)	G4_ADR_1[7:0]	7:0	GPIO4 Mapping Address 1, If Address = 0x00 -> Disable
15C (00BDh)	G4_ADR_1[8]	0	
	G4_STABIT_1[2:0]	3:1	GPIO4 Mapping Start Bit 2 (0~7)
	Reserved	7:4	
15D (00BEh)	G4_ADR_2[7:0]	7:0	GPIO4 Mapping Address 2, If Address = 0x00 -> Disable
15E (00BFh)	G4_ADR_2[8]	0	
	G4_STABIT_2[2:0]	3:1	GPIO4 Mapping Start Bit 1 (0~7)
	G4_BITNUM_2[3:0]	7:4	GPIO4 Mapping Bit Num 2 (1~8)
15F (00C0h)	G5_ADR_1[7:0]	7:0	GPIO5 Mapping Address 1, If Address = 0x00 -> Disable
160 (00C1h)	G5_ADR_1[8]	0	
	G5_STABIT_1[2:0]	3:1	GPIO5 Mapping Start Bit 1 (0~7)
	Reserved	7:4	

ADDRESS	NAME	BIT	CONTENTS
161 (00C2h)	G5_ADR_2[7:0]	7:0	GPIO5 Mapping Address 2, If Address = 0x00 -> Disable
162 (00C3h)	G5_ADR_2[8]	0	
	G5_STABIT_2[2:0]	3:1	GPIO5 Mapping Start Bit 2 (0~7)
	G5_BITNUM_2[3:0]	7:4	GPIO5 Mapping Bit Num 2 (1~8)
163 (00C4h)	G6_ADR_1[7:0]	7:0	GPIO6 Mapping Address 1, If Address = 0x00 -> Disable
164 (00C5h)	G6_ADR_1[8]	0	
	G6_STABIT_1[2:0]	3:1	GPIO6 Mapping Start Bit 1 (0~7)
	Reserved	7:4	
165 (00C6h)	G6_ADR_2[7:0]	7:0	GPIO6 Mapping Address 2, If Address = 0x00 -> Disable
166 (00C7h)	G6_ADR_2[8]	0	
	G6_STABIT_2[2:0]	3:1	GPIO6 Mapping Start Bit 2 (0~7)
	G6_BITNUM_2[3:0]	7:4	GPIO6 Mapping Bit Num 2 (1~8)
167 (00C8h)	G7_ADR_1[7:0]	7:0	GPIO7 Mapping Address 1, If Address = 0x00 -> Disable
168 (00C9h)	G7_ADR_1[8]	0	
	G7_STABIT_1[2:0]	3:1	GPIO7 Mapping Start Bit 1 (0~7)
	Reserved	7:4	
169 (00CAh)	G7_ADR_2[7:0]	7:0	GPIO7 Mapping Address 2, If Address = 0x00 -> Disable
16A (00CBh)	G7_ADR_2[8]	0	
	G7_STABIT_2[2:0]	3:1	GPIO7 Mapping Start Bit 2 (0~7)
	G7_BITNUM_2[3:0]	7:4	GPIO7 Mapping Bit Num 2 (1~8)
16B (00CCh)	G0_L_DATA	7:0	DATA Setting when GPIO 0 = L
16C (00CDh)	G0_H_DATA	7:0	DATA Setting when GPIO 0 = H
16D (00CEh)	G1_L_DATA	7:0	DATA Setting when GPIO 1 = L
16E (00CFh)	G1_H_DATA	7:0	DATA Setting when GPIO 1 = H
16F (00D0h)	G2_L_DATA	7:0	DATA Setting when GPIO 2 = L
170 (00D1h)	G2_H_DATA	7:0	DATA Setting when GPIO 2 = H

ADDRESS	NAME	BIT	CONTENTS
170 (00D1h)	G2_H_DATA	7:0	DATA Setting when GPIO 2 = H
171 (00D2h)	G3_L_DATA	7:0	DATA Setting when GPIO 3 = L
172 (00D3h)	G3_H_DATA	7:0	DATA Setting when GPIO 3 = H
173 (00D4h)	G4_L_DATA	7:0	DATA Setting when GPIO 4 = L
174 (00D5h)	G4_H_DATA	7:0	DATA Setting when GPIO 4 = H
175 (00D6h)	G5_L_DATA	7:0	DATA Setting when GPIO 5 = L
176 (00D7h)	G5_H_DATA	7:0	DATA Setting when GPIO 5 = H
177 (00D8h)	G6_L_DATA	7:0	DATA Setting when GPIO 6 = L
178 (00D9h)	G6_H_DATA	7:0	DATA Setting when GPIO 6 = H
179 (00DAh)	G7_L_DATA	7:0	DATA Setting when GPIO 7 = L
17A (00DBh)	G7_H_DATA	7:0	DATA Setting when GPIO 7 = H
17B~1A1	Reserved		
1A2~3FF	Defect compensation		For defect compensation use

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply	V_{CC}	-0.3 to +4.3	V
	V_{CC55}	-0.3 to +5.5	
Input Voltage	V_{IN}	-0.3 to V_{CC} + 0.3	
Output Voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	
Storage Temperature	T_{STG}	-55 ~ +150	°C

RECOMMEND OPERATING CONDITIONS

Characteristics	Symbol	MIN.	TYP.	MAX	Unit
Power Supply	V_{CC}	3	3.3	3.6	V
	V_{CC55}	3		5.25	
Input Voltage	V_{IN}	0		V_{CC}	
Operation Temperature	T_{OP}	-20	+25	+70	°C

DC ELECTRICAL CHARACTERISTICS

(Under Recommended Operating condition and V_{CC} = 3.0 ~ 3.6V)

Characteristics	Symbol	CONDITIONS	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}	LV-TTL			0.8	V
Input high voltage	V_{IH}	LV-TTL	2			
Output low voltage	V_{OL}	I_{OL}= 4, 8 mA			0.4	
Output high voltage	V_{OH}	I_{OH}= 4, 8 mA	2.4			
Input pull-up/down resistance	R_I	V_{IL} = 0 V or V_{IH} = V_{CC}		70		KΩ
Power supply current of AV_{DD}	I_{CCA}			37		mA
Power supply current of DV_{DD}	I_{CCD}		65		72	
Power supply current of H1, H2, RG output	I_{CC-CCD}		4		32	
Output current	I_{OUT1}	PSB04RTC		4		
Output current	I_{OUT2}	PDO08		8		

PACKAGE DIMENSION

UQFP80 (10mm X 10mm)

(Units : mm)