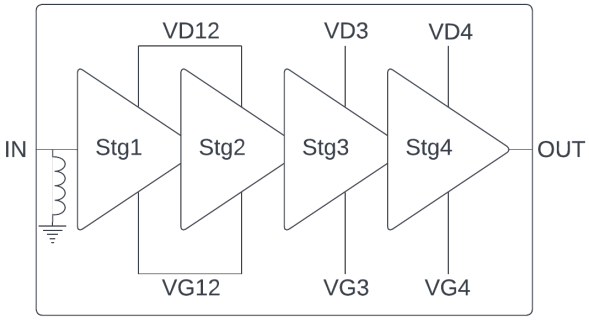
Advanced Information: AI2228

39.5-42.5GHz Q Band 8W High Power Amplifier

GaN Monolithic Microwave IC



UMS develops a four stages High Power Amplifier operating between 39.5 and 42.5 GHz and providing more than 8W of saturated output power and 24% of power added efficiency. The typical power supply is 20V/290mA (quiescent current). For these supply conditions, the CHA7455-99F provides a junction temperature below 160°C, even in saturation. The circuit is manufactured on a space evaluated 0.15µm gate length GaN-on-SiC HEMT process and is available in bare die form. It is well suited for SATCOM downlink and 5G applications.

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Electrical Characteristics

Tcase= +25°C, Vd = 20V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	39.5		42.5	GHz
Gain	Linear Gain		32		dB
Pout	Saturated Output Power		39.5		dBm
PAE	Power Added Efficiency		24		%
Id	Drain current at saturation		1.9		A
S11	Input Return Loss		-12		dB
S22	Output return loss		-15		dB
Idq	Quiescent current		290		mA
Vd	Drain Voltage		20		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tcase= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Small Signal drain bias current	800	mA
Vg	Gate bias voltage	-7 to -1	V
Tj	Maximum Junction temperature (2) (3)	230	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s
(3) Same as Recommended Operating Range

Recommended Operating Range (3)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Small signal drain bias current	100 to 450	mA
Vg	Gate bias voltage	-3.5 to -2.5	V
Tj	Maximum Junction temperature	200	°C

(3) Electrical performances are not guaranteed over all recommended operating conditions

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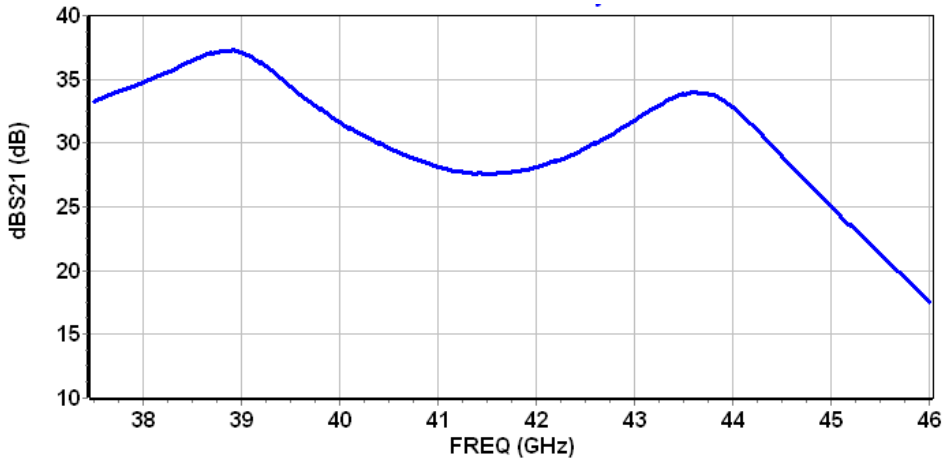
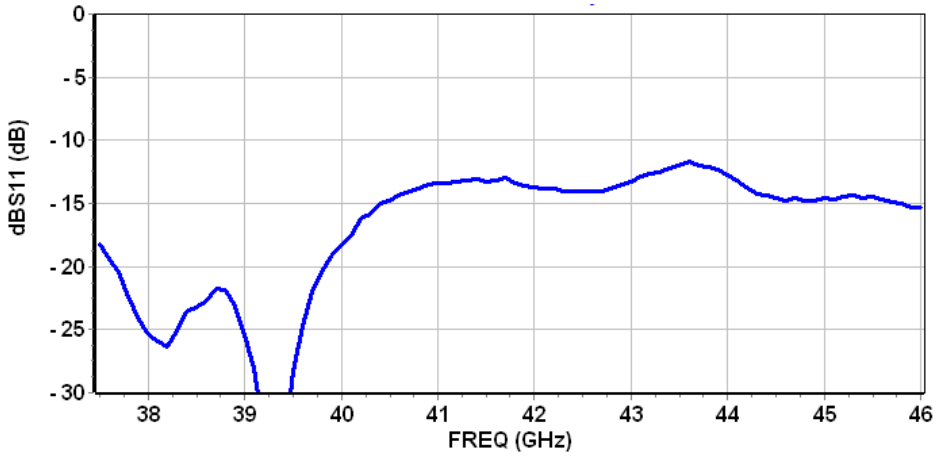
Typical Board Measurements

Tcase= +25°C, Vd = +20V, Id = 290mA

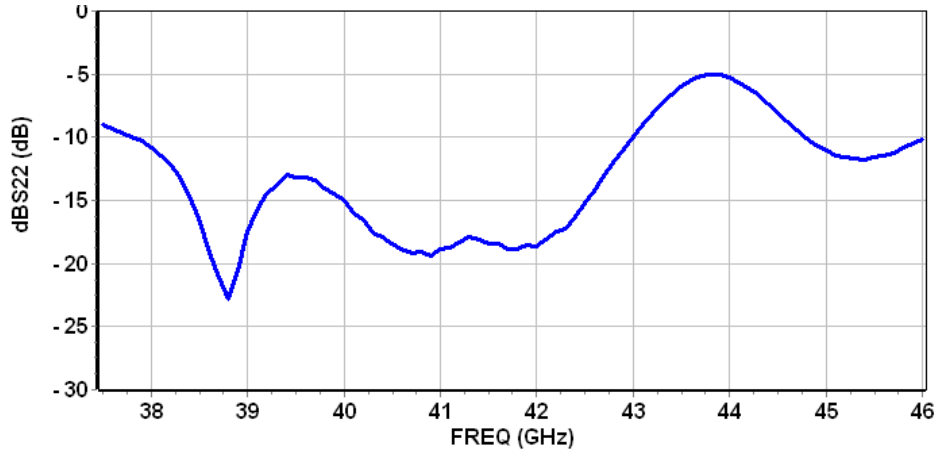
Linear Gain



Input Reflexion Coefficient



Output Reflexion Coefficient



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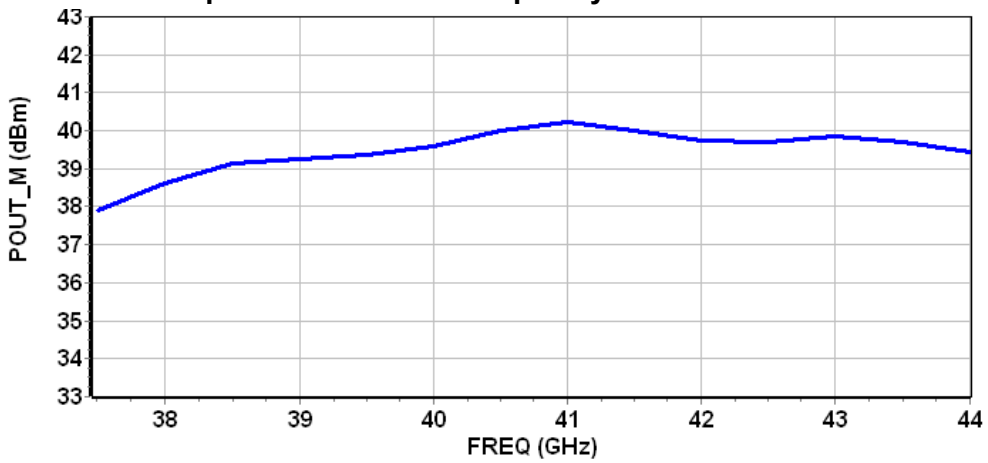
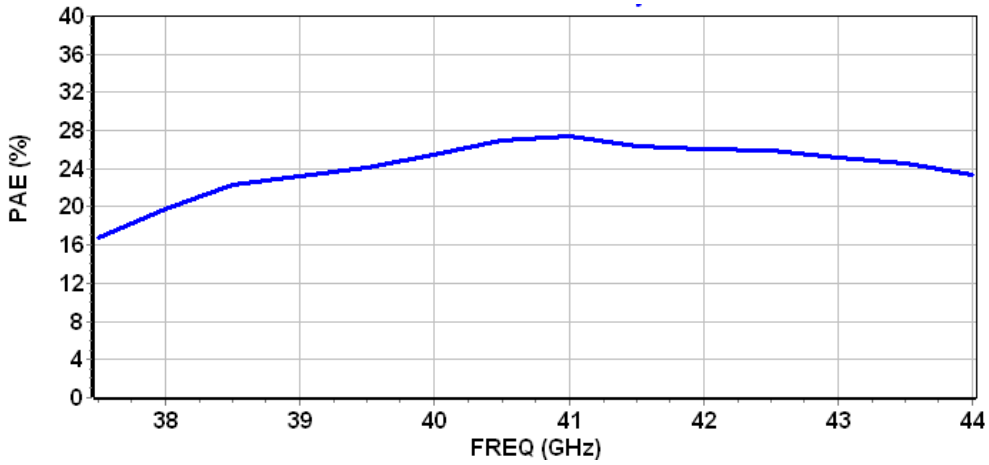
Typical Board Measurements : Large Signal Performances

Tcase= +25°C, Vd = +20V, Id = 290mA

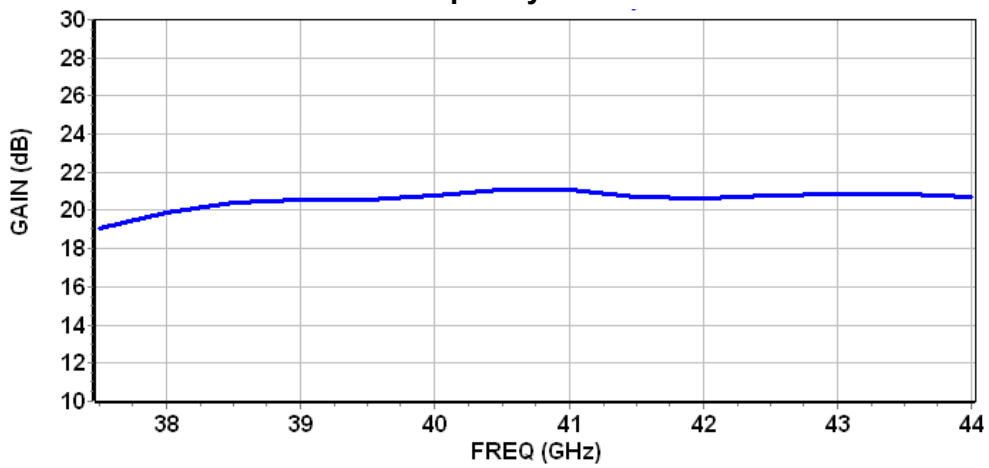
Output Power versus Frequency at Pin = 21 dBm



PAE versus Frequency at Pin = 18 dBm



Gain versus Frequency at Pin = 18 dBm



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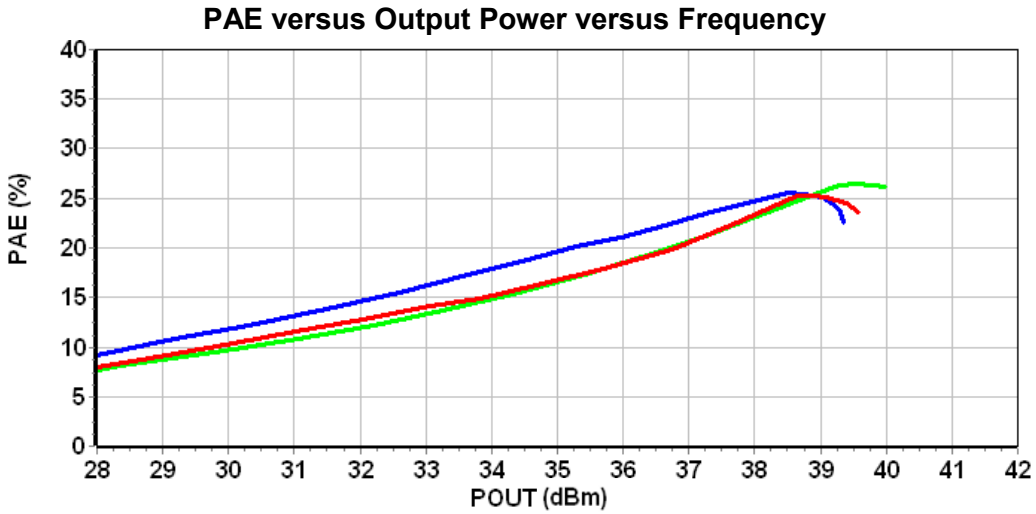
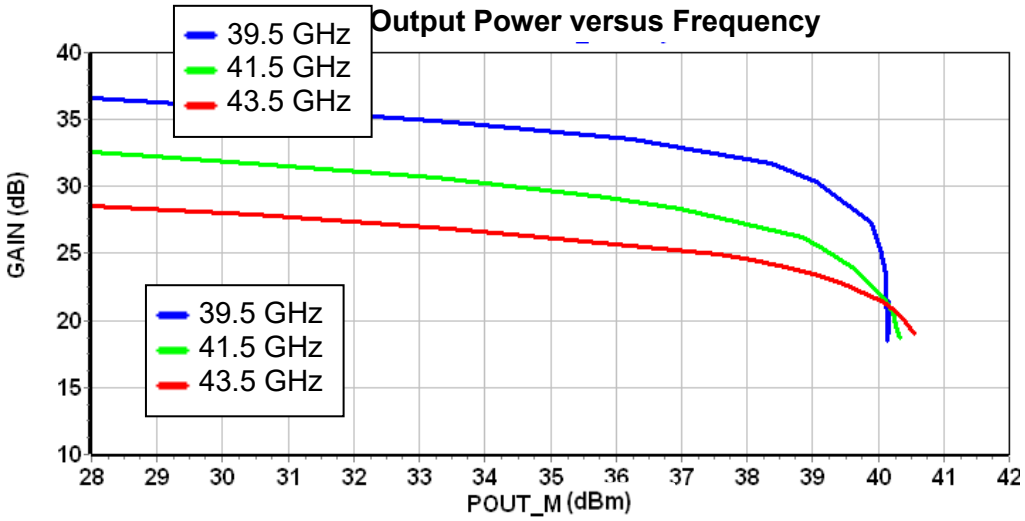
Typical Board Measurements : Large Signal Performances

Tcase= +25°C, Vd = +20V, Id = 290mA, Pin = 18dBm





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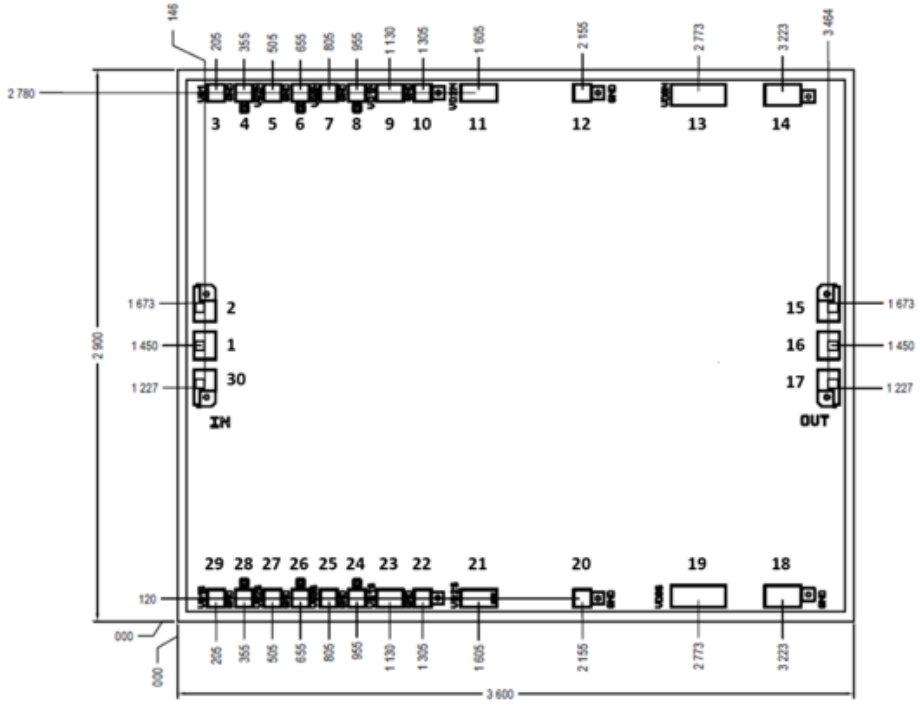
Mechanical data



PAD Number	Name	Description	Pad size (BCB Opening)
1	RF IN	Input RF port	186µm x 105µm
3	G12	DC Gate voltage, 1st & 2st stage, North	96µm x 96µm
5	G3	DC Gate voltage 3d stage, North	96µm x 96µm
7	G4	DC Gate voltage 4th stage, North	96µm x 96µm
9	D12	DC Drain voltage, 1st & 2st stage, North	146µm x 96µm
11	D3	DC Drain voltage 3d stage, North	196µm x 96µm
13	D4	DC Drain voltage 4th stage, North	296µm x 116µm
16	RF OUT	Output RF port	118 µm x146 µm
19	D4	DC Drain voltage 4th stage, South	296µm x 116µm
21	D3	DC Drain voltage 3d stage, South	196µm x 96µm
23	D12	DC Drain voltage, 1st & 2st stage, South	146µm x 96µm
25	G4	DC Gate voltage 4th stage, South	96µm x 96µm
27	G3	DC Gate voltage 3d stage, South	96µm x 96µm
29	G12	DC Gait voltage, 1st & 2st stage, South	96µm x 96µm
2,4,6,8,10,12,14, 15,17,18,20,22,2 4,26,28,30	GND	NC (Ground)	96µm x 96µm

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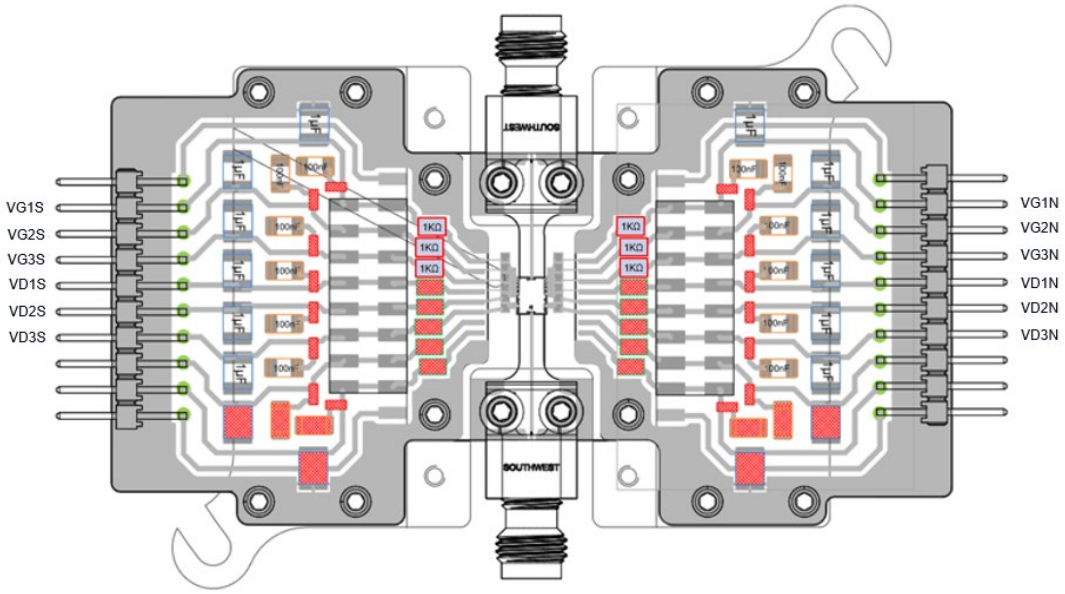
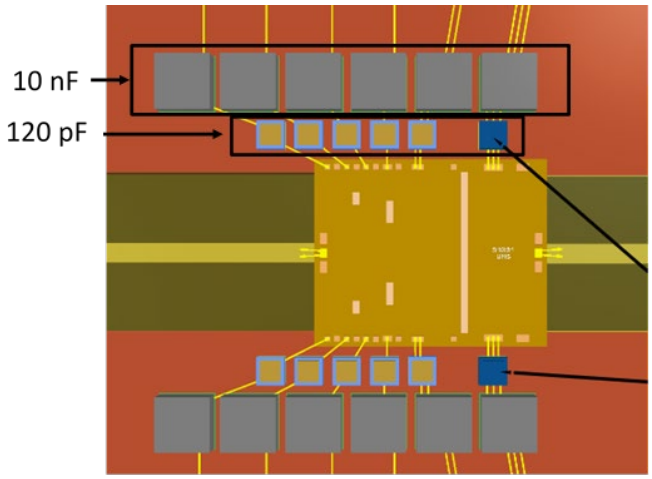
Recommended Evaluation Board



Recommended Assembly Plan



4 levels of decoupling capacitor have been used, 2 on the tab and 2 on the board.
The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 100nF SMD 1210 capacitors and the fourth stage is composed of 1µF SMD 1206 capacitors. The first two levels should be as close as possible to the die. A 1KΩ resistor was added in series on each gate supply.

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Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Maturity Level

Maturity Level	Product status	Documentation	Reliability	Usage in a system
Lab Sample (LS)	Decision to develop the product is not confirmed	Technical Information	No commitment	Lab demonstrator
Engineering Sample (ES)	**Design may change**	**Advanced Information**	**The design is within the recommended temperature, current and voltage ranges as regards the technology used.**	**Engineering demonstrator**
Product Representative Unit (PRU)	Design is frozen	Data-sheet	Tests results are available on the foreseen product or on an similar one	Production

Sampling request reference

Die: ES-CHA7455-99F

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