A1 PROs

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Ai3152

Digital Signal Processor for Color CCD Camera

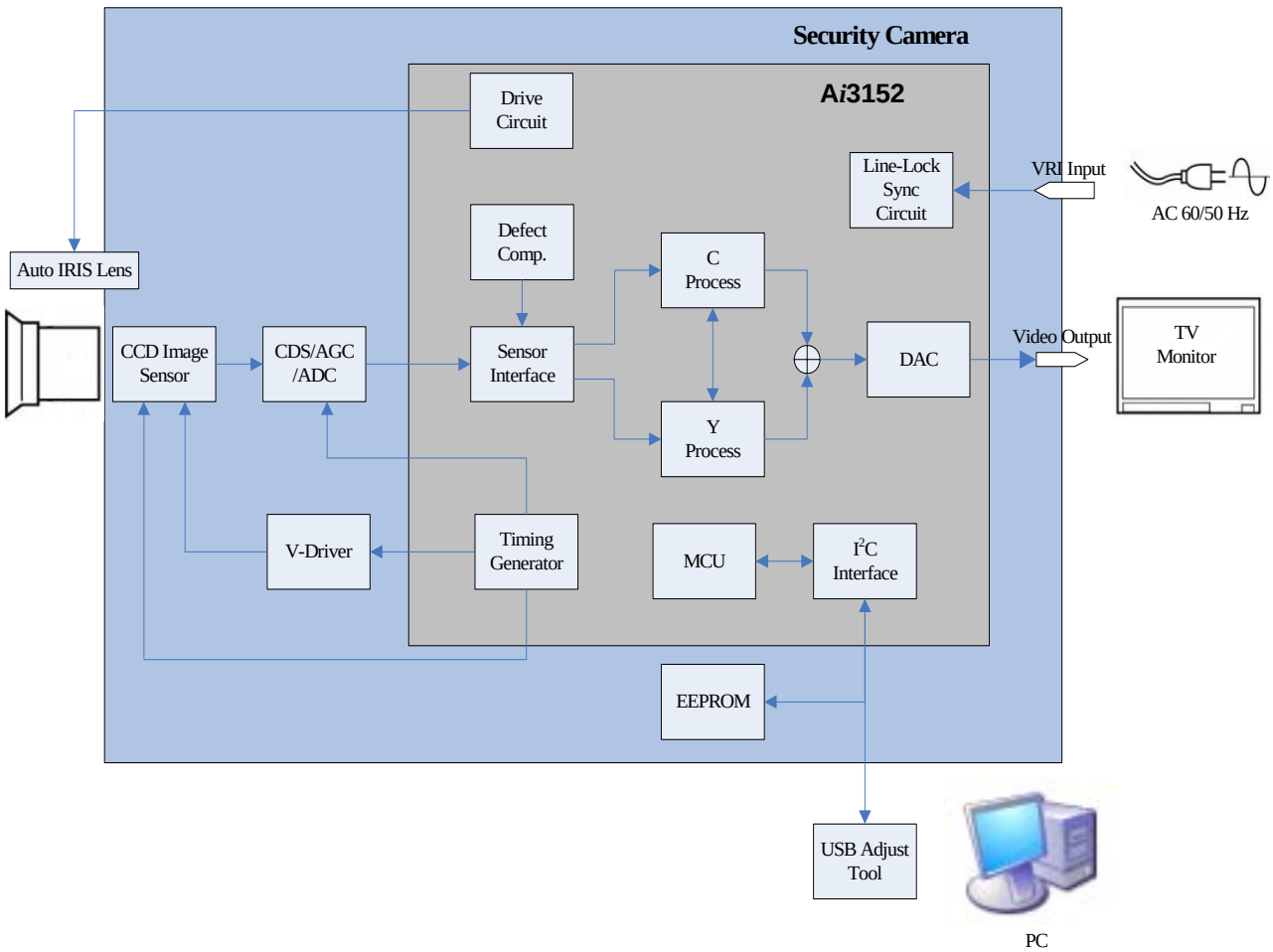
General Description

The Ai3152 is the digital signal-processing chip for color video camera. It includes timing generator and digital/analog output. Supports 250K / 380K NTSC system CCD sensors and 290K / 440K PAL system CCD sensors with complementary color filter. It also provided line lock function.

Features

- Support Ye, Cyan, Magenta, Green complementary color filter CCD sensors for
  NTSC : A*i*325CA(250K), A*i*338CA(380K)
  PAL : A*i*329CA(290K), A*i*344CA(440K)
- Flexible Color Adjustment.
- Digital Noise Reduction.
- High performance AWB (5 set linear matrix).
- IRIS coexists with AES and AGC.
- Day or Night notice output.
- Timing adjustment by 1 ns delay
- White clip / Setup level / Sync level adjustment independent.
- Build-in blemish compensation circuit to store the data in EEPROM, the blemish pixel can up to 176 pixels.
- Programmable pull-up / pull-down GPIO and DVIO pin.
- Horizontal resolution up to 500 TVL
- Video drive for IRIS lens is possible by simple drive circuit even no CCD signal pin (CCDLEVEL or Mon_out) from AFE.
- Hi-speed AE.
- Support external EEPROM to store parameter.
- Build-in auto white balance control.
- Build-in auto exposure control.
- Build-in backlight compensation.
- Build-in 10bit digital to analog converter.
- Build-in mirror function.
- Support NTSC/PAL analog composite video output.
- Build-in timing generator for vertical driver and CDS/AGC/ADC peripheral chips.
- Single 3.3V power supply. (Horizontal drive pins can be 3.3V/5V)
- Support GPIO pin Define function.
- Programmable CCD Timing and Driving Current.
- Support Digital Line Lock function.
- LQFP-80 (10x10mm ; 0.4mm pin pitch)

Functional Block Diagram



Pin Description

PIN NO	SYMBOL	DIR	DESCRIPTION
1	VSSA_DAC	G	Ground
2	VDDA_DAC	P	Analog Power
3	VDAC_REG	O	Regulator output for video DAC (VB)
4	VREF	O	REF for video DAC (IREF)
5	I_OUTB	O	IOUTB for video DAC ~ analog ground (GNDDA)
6	I_OUT	O	IOUT for video DAC ~ analog signal (VIDEO)
7	GPIO_3	B	General purpose I/O
8	GPIO_4	B	General purpose I/O
9	GPIO_5	B	General purpose I/O
10	GPIO_6	B	General purpose I/O
11	GPIO_7	B	General purpose I/O
12	DV_DCLK	O	Clock for digital output
13	VRI	B	Line lock signal input (50/60Hz)
14	DVIO_0	B	DV I/O for digital output
15	DVIO_1	B	DV I/O for digital output
16	VDD18	P	1.8v Digital Power
17	VSS	G	Ground
18	VDD33	P	3.3v Digital Power
19	DVIO_2	B	DV I/O for digital output
20	DVIO_3	B	DV I/O for digital output
21	DVIO_4	B	DV I/O for digital output
22	DVIO_5	B	DV I/O for digital output
23	DVIO_6	B	DV I/O for digital output
24	DVIO_7	B	DV I/O for digital output
25	DV_HSYNC	O	HSYNC for digital output
26	DV_VSYNC	O	VSYNC for digital output
27	CCD_V1X	O	Vertical shift register clock1

PIN NO	SYMBOL	DIR	DESCRIPTION
28	CCD_V2X	O	Vertical shift register clock3
29	CCD_V3X	O	Vertical shift register clock3
30	VDD33	P	3.3v Digital Power
31	VDDA_LDO	P	3.3v Analog Power
32	VDDAL_LDO	O	1.8v Core Power out
33	VSS	G	Ground
34	VDD18	P	1.8v Digital Power
35	CCD_V4X	O	Vertical shift register clock4
36	AFE_CSN	O	AFE 3-wire CSN
37	SDA	B	EEPROM SDA for I2C interface
38	SCL	B	EEPROM SCL for I2C interface
39	CCD_VH1X	O	Readout pulse H1
40	CCD_VH3X	O	Readout pulse H3
41	CCD_OFDX	O	OFD pulse output
42	TEST	I	Chip test pin
43	VSSA	G	Ground
44	VDDA_18	P	1.8v Analog Power
45	VDDA_PLL_IO	P	3.3v Analog Power
46	XIN	I	OSC input (NTSC:28.636, PAL:28.375MHz)
47	XOUT	O	OSC output
48	N_RST	B	System reset (PORM)
49	I2C_RDY	B	I2C Bus Ready
50	AFE_SCL	O	AFE 3-wire SCL
51	AFE_SDA	O	AFE 3-wire SDA
52	VDD33	P	3.3v Digital Power
53	VSS	G	Ground
54	AFE_IMG_9	I	CCD image data (MSB)
55	AFE_IMG_8	I	CCD image data
56	AFE_IMG_7	I	CCD image data
57	AFE_IMG_6	I	CCD image data
58	AFE_IMG_5	I	CCD image data

PIN NO	SYMBOL	DIR	DESCRIPTION
59	AFE_IMG_4	I	CCD image data
60	AFE_IMG_3	I	CCD image data
61	AFE_IMG_2	I	CCD image data
62	AFE_IMG_1	I	CCD image data
63	AFE_IMG_0	I	CCD image data (LSB)
64	VDD33	P	3.3v Digital Power
65	VSS	G	Ground
66	VDD18	P	1.8v Digital Power
67	AFE_OBCP	O	Clamp pulse output for optical black
68	AFE_ADCLP	O	Clamp pulse output for ADC
69	AFE_BLKX	O	Blanking pulse output
70	AFE_ADCK	O	Clock output for AFE A/D converter
71	AFE_FCDS	O	Sample hold pulse output (reference)
72	AFE_FS	O	Sample hold pulse output (data)
73	GPIO_0	B	General purpose I/O / PWM
74	GPIO_1	B	General purpose I/O
75	GPIO_2	B	General purpose I/O
76	CCD_FR	O	Reset pulse output
77	VDD5	P	3.3v/5V Digital Power (for FR、FH1、FH2 pulse)
78	VSS5	G	Ground (for FR、FH1、FH2 pulse)
79	CCD_FH1	O	Horizontal shift register clock1
80	CCD_FH2	O	Horizontal shift register clock2

Item	Description	Item	Description
I	Input	P	Power
O	Output	G	Ground
B	Bi-direction		

DSP Register Table

EEP Adr.	Start Bit	Bit Num	Data L (HEX)	Data H (HEX)	Bit	Symbol	Description
0F	0	2			1:0	TV_MONO[1:0]	TV color/mono display mode selection. 00: color display mode with color burst. 01: mono display mode with color burst. 10: color display mode without color burst. 11: mono display mode without color burst.
42	0	5			4:0	AP_FIRGA[4:0]	Initial value of APT_FIRGA (gain of FIR horizontal edge signal)
49	1	1			1	AP_CTRL_EN	1: Enable Horizontal and Vertical aperture control.
	2	1			2	APKNEE_EN	1: Enable Aperture KNEE.
	3	1			3	AP_CORING_EN	1: Enable Aperture CORING.
	5	1			5	YGAMMA_EN	1: Enable Y Gamma.
	6	1			6	Y_LCRAWL_EN	1: Enable Line Crawl.
4D	5	1			5	DENOISE	DENOISE enable 0: Disable 1: Enable
	6	1			6	NONLINEAR	NONLINEAR enable 0: Disable 1: Enable
	7	1			7	RGB_GAMMA_EN	RGB gamma enable 0: Disable 1: Enable
4E	0	8			7:0	APKNEE_Y128	Y for APKNEE curve when X=128. Y= APKNEE_Y128 *2, Note: Y0=0.
4F	0	8			7:0	APKNEE_Y256	Y for APKNEE curve when X=256. Y= APKNEE_Y256 *2
50	0	8			7:0	APKNEE_Y384	Y for APKNEE curve when X=384. Y= APKNEE_Y384 *2
51	0	8			7:0	APKNEE_Y512	Y for APKNEE curve when X=512. Y= APKNEE_Y512 *2
52	0	8			7:0	APKNEE_Y640	Y for APKNEE curve when X=640. Y= APKNEE_Y640 *2
53	0	8			7:0	APKNEE_Y768	Y for APKNEE curve when X=768. Y= APKNEE_Y768 *2
54	0	8			7:0	APKNEE_Y896	Y for APKNEE curve when X=896. Y= APKNEE_Y896 *2
55	0	8			7:0	APKNEE_Y1024	Y for APKNEE curve when X=1024. Y= APKNEE_Y1024 *2
56	0	8			5:0	AP_CORN[5:0]	Aperture corn control -> Corn = AP_CORN * 2

EEP Adr.	Start Bit	Bit Num	Data L (HEX)	Data H (HEX)	Bit	Symbol	Description
73	5	1			5	LL_ENABLE	Line lock enable 0: Disable 1: Enable Line Lock
B2	0	1			0	PWM_EN	0: PWM disable. 1: PWM enable. DVIO_3 output PWM.
BB	0	2			1:0	WB_MODE[1:0]	White balance mode 00: Auto 01: AWB1 (3100^{o}K) 10: AWB2 (5100^{o}K) 11: AWB3 (6500^{o}K)
	2	1			2	MIRROR	Mirror 0: Disable 1: Enable
	3	1			3	Back Light Compensation	Back light compensation 0: Disable 1: Enable
	4	4			7:4	SHUTTER_MODE [4:0]	Shutter speed select 0000: 1/60 (1/50) 0001: 1/120 (1/100) 0010: 1/250 0011: 1/500 0100: 1/1000 0101: 1/2000 0110: 1/5000 0111: 1/10000 1000: 1/20000 1001: 1/50000 1010: 1/100000 1011 ~ 1111: Auto
BC	0	1			0	MCRDIP (High Light Invert)	0: Disable 1: Enable microcontroller DIP switch scan
	1	1			1	Flickless	0: Disable 1: Enable flickless
	2	1			2	AGC_OFF	AGC control 0: ON 1: OFF
	7	1			7	AE_STOP	Stop AE_Control 0: AE Control ON 1: Stop
C2	4	1			4	AWB_STOP	AWB_STOP 0: AWB ON 1: AWB Stop
FB	2	3			4:2	AWB_RANGE [2:0]	000: AWB Range 1 001: AWB Range 2 010: AWB Range 3 011: AWB Range 4 100: AWB Range 5
1C7	0	1			0	DAY_NIGHT _MODE_EN	0 : Disable 1 : Enable

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Power supply	V_{CC}	-0.3	4.3	V
	V_{CC55}	-0.3	5.5	V
Input voltage	V_{IN}	-0.3	V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3	V_{CC} + 0.3	V
Storage temperature	T_{STG}	-55	150	℃

Recommend Operating Conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply	V_{CC}	3.0	3.3	3.6	V
	V_{CC55}	3		5.25	V
Input voltage	V_{IN}	0		V_{CC}	V
Operation temperature	T_{OP}	-20	+25	+70	℃

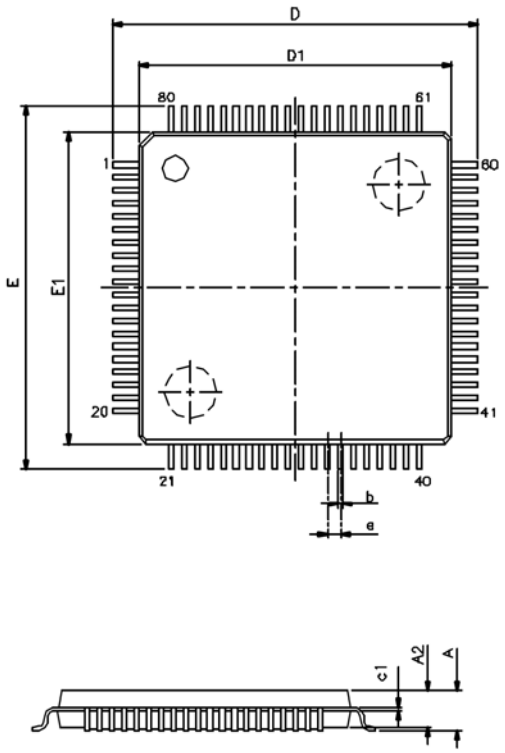
DC Electrical Characteristics

(Under Recommended Operating Conditions and VCC=3.0 ~ 3.6V)

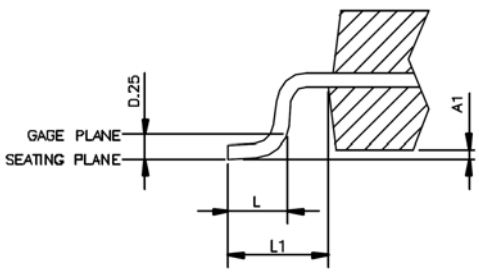
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input low voltage	V_{IL}	LV-TTL			0.8	V
Input high voltage	V_{IH}	LV-TTL	2			V
Output low voltage	V_{OL}	I_{OL} = 4, 8 mA			0.4	V
Output high voltage	V_{OH}	I_{OH} = 4, 8 mA	2.4			V
Input pull-up/down resistance	R_I	V_{IL} = 0 V or V_{IH} = V_{CC}		70		KΩ
Power supply current of AVDD	I_{CCA}			37		mA
Power supply current of DVDD	I_{CCD}		65		72	mA
Power supply current of FH1, FH2, FR output	I_{CC-CCD}		4		32	mA
Output current	I_{OUTPUT}			4		mA

Package Dimension

LQFP80 (10mm X 10mm)



Unit: mm



SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	12 BSC	
D1	10 BSC	
E	12 BSC	
E1	10 BSC	
e	0.4 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	