



## Description

The Ai325 is a 250K pixels CCD area sensor for EIA 1/3inch video cameras. Buried photodiode and micro lens are adopted for low noise, low smear and high sensitivity. This chip also features a strong anti-blooming and electronic shutter with variable charge-storage time.

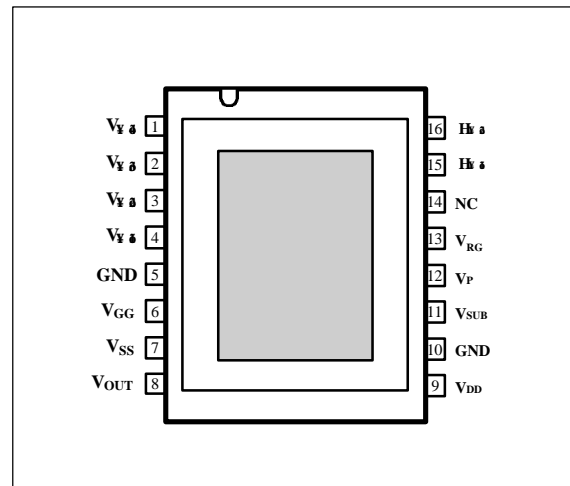
## Feature

- Micro Lens for high sensitivity
- Image-lag is negligible and excellent blooming suppression is performed.
- TTL level(5V) operation on HCCD & RG electrodes.
- 16 pin plastic-DIP.
- Variable electronic shutter of 1/60 to 1/100,000 sec.
- High sensitivity and low smear.

## Structure

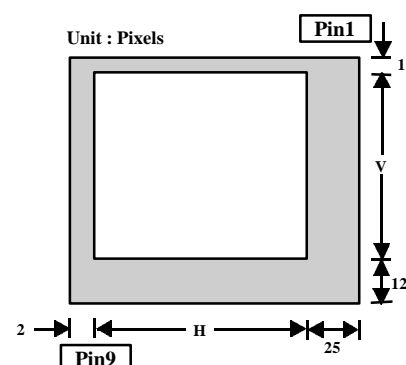
- Architecture : IT - CCD
- Optical size : 1/3 inch format
- Chip size : 6.0(H) x 5.2(V)  $\pm$
- Number of effective pixels :  
510 (H) x 492 (V) about 250K pixels
- Number of total pixels :  
537 (H) x 505 (V) about 270K pixels
- Pixel size : 9.65 (H) x 7.5 (V)  $\mu$  <sup>2</sup>
- Optical black area  
Horizontal direction : Front 2 pixels Rear 25 pixels  
Vertical direction : Front 12 pixels Rear 1 pixels
- Number of dummy bits  
Horizontal : 16  
Vertical : 1 ( Even field only )

## Pin Configuration

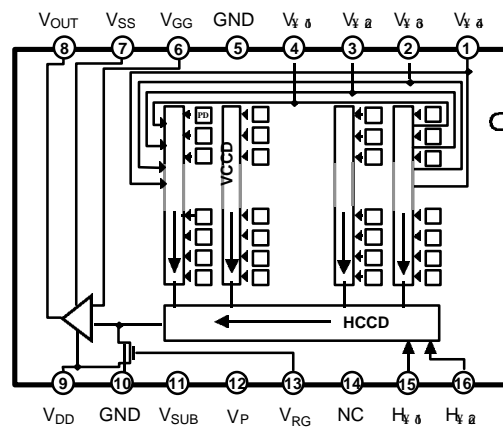


16 Pin Plastic - DIP  
( Top View )

## Optical black position( Top View )



**Block Diagram**



**Pin Description**

No.	Symbol	Description	No.	Symbol	Description
1	$V_{V4}$	Vertical register transfer clock 4	9	$V_{DD}$	Output amplifier drain bias
2	$V_{V3}$	Vertical register transfer clock 3	10	GND	Ground
3	$V_{V2}$	Vertical register transfer clock 2	11	$V_{SUB}$	Substrate(Overflow drain)bias
4	$V_{V1}$	Vertical register transfer clock 1	12	$V_P$	Protection bias
5	GND	Ground	13	$V_{RG}$	Reset gate clock
6	$V_{GG}$	Output amplifier gate bias	14	NC	No connection
7	$V_{SS}$	Output amplifier source bias	15	$H_{V1}$	Horizontal register transfer clock 1
8	$V_{OUT}$	CCD Output signal	16	$H_{V2}$	Horizontal register transfer clock 2

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Substrate voltage	$V_{SUB} - GND$	-0.3 to +55	V
Supply voltage	$V_{DD}, V_{OUT}, V_{SS} - GND$	-0.3 to +18	V
	$V_{DD}, V_{OUT}, V_{SS} - V_{SUB}$	-55 to +10	V
Vertical clock input voltage	$V_{V1}, 2, 3, 4 - GND$	-10 to +20	V
	$V_{V1}, 2, 3, 4 - V_P$	-0.3 to +27	V
	$V_{V1}, 2, 3, 4 - V_{SUB}$	-55 to +10	V
Horizontal clock input voltage	$H_{V1}, H_{V2} - GND$	-10 to +15	V
Between vertical clock input pins	$V_{Vx} - V_{Vy}$	-10 to +15	V
Between horizontal clock and vertical clock input pins	$H_{Vx}, H_{Vy} - V_{Vx}$	-17 to +17	V
Output pin voltage	$V_{RG}, V_{GG} - GND$	-10 to +15	V
	$V_{RG}, V_{GG} - V_{SUB}$	-55 to +10	V
Protective circuit voltage	$V_P - V_{SUB}$	-65 to 0.3	V
Storage temperature	$T_{STG}$	-30 to 80	$^{\circ}C$
Operation temperature	$T_{OPR}$	-10 to 60	$^{\circ}C$

### Bias Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Output amplifier drain voltage	$V_{dd}$	14.5	15.0	15.5	V	
Output amplifier gate voltage	$V_{gg}$	1.5	2.0	2.5	V	
Output amplifier source voltage	$V_{ss}$	Ground through 680Ω Resistor, ±5%				
Substrate voltage adjustment range	$V_{sub}$	5		15	V	
Fluctuation range after substrate voltage adjustment	$\Delta V_{sub}$	-1		1	V	
Reset gate clock voltage adjustment range	$V_{rgl}$	0		4	V	
Fluctuation range after reset gate voltage adjustment	$\Delta V_{rgl}$	-3		3	%	
Protection bias	$V_p$	Set to low level of vertical transfer clock				

### DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output amplifier drain current	$I_{DD}$	-	3	-	mA

### Driving Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical clock high voltage	$V_{H1}, V_{H3}$	14.5	15.0	15.5	V
Vertical clock middle voltage	$V_{M1, 2, 3, 4}$	-0.2	0.0	0.2	V
Vertical clock low voltage	$V_{L1, 2, 3, 4}$	-9.0	-8.5	-8.0	V
Horizontal clock high voltage	$V_{H1, 2}$	4.5	5.0	5.5	V
Horizontal clock low voltage	$V_{L1, 2}$	-0.5	0.0	0.5	V
RG clock voltage difference	$V_{RGHL}$	4.7	5.0	5.3	V
Substrate clock voltage	$V_{SUB}$	23	24	25	V

**Electro-optical Performance**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Method	Remark
Sensitivity	SENS	55	70		\$ \u00c5Lux	1	
Saturation signal	V <sub>SAT</sub>	800			\$ \u00c5	2	Temp=60; \u00c5
Smear	S <sub>MR</sub>			0.015	%	3	
Blooming	BL			1	%	4	
Video signal shading	OSNU			15	%	5	
Dark signal level	V <sub>DARK</sub>			2	\$ \u00c5	6	Temp=60; \u00c5
Dark signal shading	DSNU			2	\$ \u00c5	7	Temp=60; \u00c5

## Measurement Method

### 1. Sensitivity

- Set to SILC ( Standard Illumination Conditions\* )
- Measure the average value of signal output (  $V_{out}$  )
- Calculate the efficiency of  $V_{out}$  to light intensity

### 2. $V_{sat}$

- Adjust light intensity to 200 times of SILC
- Measure the average value of signal output

### 3. Smear

- Adjust light intensity to 200 times of SILC & readout clock
- Measure the signal output at horizontal optical black (  $V_{hopb}$  )
- Measure the signal output at vertical blanking dummy (  $V_{vbd}$  )
- $Smear = \{ ( V_{vbd} - V_{hopb} ) / V_{sat} \} \times 100 ( \% )$

### 4. Blooming

- Adjust light intensity to 200 times of SILC & readout clock
- Measure the signal output at horizontal optical black (  $V_{hopb}$  )
- Measure the signal output at blooming dummy area (  $V_{bd}$  )
- $Blooming = \{ ( V_{bd} - V_{hopb} ) / V_{sat} \} \times 100 ( \% )$

### 5. OSNU

- Set to SILC
- Measure the average value of signal output (  $V_{out}$  )
- Measure the maximum value and the minimum value of signal output
- $OSNU = ( V_{max} - V_{min} ) / V_{out} \times 100 ( \% )$

### 6. $V_{dark}$

- Measure the average value of signal output at dark condition

### 7. DSNU

- Measure the voltage difference between minimum and maximum of dark signal

#### \* Standard Illumination Conditions

- Measure the average value of output of linear region
  - At this time, measure the light intensity of illumination at CCD face plate
  - Define SILC with above
  - Light source: Tungsten lamp(3100K)
  - Use a standard test lens at F8
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## **Notes on Handling**

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

### 2) Soldering

- a) Make sure the package temperature does not exceed 80 °C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

### 3) Dust and Dirt protection

- a) Perform all assembly operations in a clean room (class 1000 or less).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

### 4) Others

- a) Do not expose to strong light (sun rays) for long periods.
- b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

Application Circuit

