A1 PROs

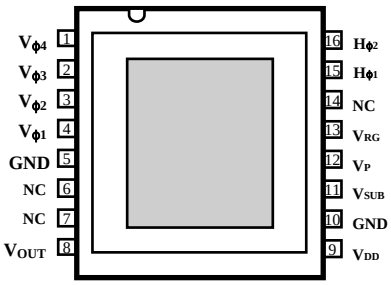
Ai325CA

1/3 inch CCD Image Sensor for NTSC Camera

GENERAL DESCRIPTION

The ***Ai325CA*** is a 250K pixels CCD area sensor for NTSC 1/3 inch video cameras. Buried photodiodes and micro lenses are adopted for low noise, low smear and high sensitivity. A chrominance signal is achieved by the adoption of Yellow, Magenta, Cyan and Green complementary color mosaic filters. This product also has the features of strong anti-blooming and electronic shutter with variable charge-storage time.

16 Pin Plastic - DIP
(Top View)



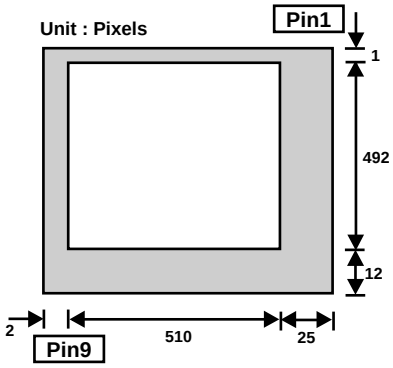
FEATURES

- Micro lens arrays for high sensitivity
- Ye, Mg, Cy and G complementary color mosaic filters
- Excellent blooming suppression
- TTL level(5V) operation on HCCD & RG electrodes
- 16 pin plastic DIP type package
- Variable electronic shutter of 1/60 to 1/100,000 sec
- High sensitivity and low smear
- Low image lag

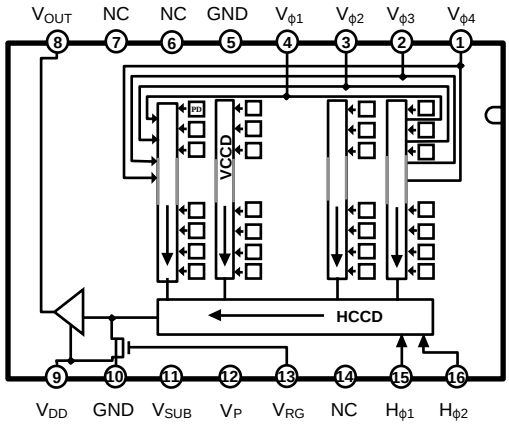
STRUCTURE

- Architecture : IT - CCD
- Optical size : 1/3 inch format
- Chip size : 6.0(H) x 5.2(V) ㎜²
- Number of effective pixels :
  510 (H) x 492 (V) about 250K pixels
- Number of total pixels :
  537 (H) x 505 (V) about 270K pixels
- Pixel size : 9.65 (H) x 7.5 (V) ㎛²
- Optical black area
  Horizontal direction : Front 2 pixels Rear 25 pixels
  Vertical direction : Front 12 pixels Rear 1 pixels
- Number of dummy bits
  Horizontal : 16
  Vertical : 1 (Even field only)

Optical black position (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Symbol	Description	Pin	Symbol	Description
1	$V_{\Phi4}$	Vertical register transfer clock 4	9	V_{DD}	Output amplifier drain bias
2	$V_{\Phi3}$	Vertical register transfer clock 3	10	GND	Ground
3	$V_{\Phi2}$	Vertical register transfer clock 2	11	V_{SUB}	Substrate (Overflow drain) bias
4	$V_{\Phi1}$	Vertical register transfer clock 1	12	V_P	Protection bias
5	GND	Ground	13	V_{RG}	Reset gate clock
6	NC	No connection	14	NC	No connection
7	NC	No connection	15	$H_{\Phi1}$	Horizontal register transfer clock 1
8	V_{OUT}	CCD output signal	16	$H_{\Phi2}$	Horizontal register transfer clock 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Substrate voltage	V_{SUB} – GND	–0.3 to +55	V
Supply voltage	V_{DD}, V_{OUT} – GND V_{DD}, V_{OUT} – V_{SUB}	–0.3 to +18 –55 to +10	V V
Vertical clock input voltage	$V_{\Phi1, 2, 3, 4}$ – GND $V_{\Phi1, 2, 3, 4}$ – V_P $V_{\Phi1, 2, 3, 4}$ – V_{SUB}	–10 to +20 –0.3 to +27 –55 to +10	V V V
Horizontal clock input voltage	$H_{\Phi1,}$ $H_{\Phi2}$ – GND	–10 to +15	V
Between vertical clock input pins	$V_{\Phi X}$ – $V_{\Phi Y}$	–10 to +15	V
Between horizontal clock and vertical clock input pins	$H_{\Phi1,}$ $H_{\Phi2}$ – $V_{\Phi4}$	–17 to +17	V
Output pin voltage	ΦRG – GND ΦRG – V_{SUB}	–10 to +15 –55 to +10	V V
Protective circuit voltage	V_P – V_{SUB}	–65 to 0.3	V
Storage temperature	T_{STG}	–30 to 80	℃
Operation temperature	T_{OPR}	–10 to 60	℃

* Protective circuit voltage(V_P) is induced to the image sensor before V_{DD} supplied power voltage.

BIAS CONDITION

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Output amplifier drain voltage	V_{DD}	14.5	15.0	15.5	V	
Substrate voltage adjustment range	V_{SUB}	5		15	V	
Fluctuation range after substrate voltage adjustment	$\triangle V_{SUB}$	–1		1	V	
Reset gate clock voltage adjustment range	V_{RG}	0		4	V	*
Fluctuation range after reset gate voltage adjustment	$\triangle V_{RG}$	–3		3	%	
Protection bias	V_P	Set to low level of vertical transfer clock				

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below.

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0.0	0.2	V	
	V_{RG}	8.5	9.0	9.5	V	

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Output amplifier drain current	I_{DD}	–	3	–	mA

DRIVING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit
Vertical clock high voltage	V_{H1}, V_{H3}	14.5	15.0	15.5	V
Vertical clock middle voltage	$V_{M1, 2, 3, 4}$	–0.2	0.0	0.2	V
Vertical clock low voltage	$V_{L1, 2, 3, 4}$	–9.0	–8.5	–8.0	V
Horizontal clock high voltage	$H_{H1, 2}$	4.5	5.0	5.5	V
Horizontal clock low voltage	$H_{L1, 2}$	–0.5	0.0	0.5	V
RG clock voltage difference	RG_{HL}	4.7	5.0	5.3	V
Substrate clock voltage	V_{SUB}	23	24	25	V

ELECTRO-OPTICAL PERFORMANCE (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Measurement Method	Remark
Sensitivity	SENS	65	80		mV/Lux	1	
Saturation signal	V_{SAT}	900			mV	2	Temp=60 °C
Smear	S_{MR}			0.015	%	3	
Blooming	BL			1	%	4	
Video signal shading	OSNU			25	%	7	
Uniformity between video signal channels	△Sr			10	%	9	
	△Sb			10	%	9	
Dark signal level	V_{DARK}			2	mV	6	Temp=60 °C
Dark signal shading	DSNU			2	mV	8	Temp=60 °C
Flicker Y	F_Y			2	%	5	
Flicker B-Y, R-Y	F_{Cr}, F_{Cb}			5	%	10	
Line crawl R, G, B, W	L_{Cr}, L_{Cb}, L_{Cg}, L_{Cw}			20	%	11	
Image lagging	Lag			0.5	%	12	

MESUREMENT METHOD

1. Sensitivity

① Set to SILC (Standard Illumination Conditions*)
② Measure the average value of signal output (V_{OUT})
③ Calculate the efficiency of V_{OUT} to light intensity

2. V_{SAT}

① Adjust light intensity to 200 times of SILC
② Measure the average value of signal output

3. Smear

① Adjust light intensity to 200 times of SILC & readout clock
② Measure the signal output at horizontal optical black (V_{HOPB})
③ Measure the signal output at vertical blanking dummy (V_{VBD})
④ Smear = { (V_{VBD} - V_{HOPB}) / V_{SAT} } × 100 (%)

4. Blooming

① Adjust light intensity to 200 times of SILC & readout clock
② Measure the signal output at horizontal optical black (V_{HOPB})
③ Measure the signal output at blooming dummy area (V_{BD})
④ Blooming = { (V_{BD} - V_{HOPB}) / V_{SAT} } × 100 (%)

5. OSNU

① Set to SILC
② Measure the average value of signal output (V_{OUT})
③ Measure the maximum value and the minimum value of signal output
④ OSNU = (V_{MAX} - V_{MIN}) / V_{OUT} ×100 (%)

6. ΔSr, ΔSb

① Set to SILC
② Measure the average value of signal output (V_{OUT})
③ Measure the maximum value and minimum value of chroma output
ΔSr = ｜(Cr_{MAX} - Cr_{MIN}) / V_{OUT} ｜×100 (%)
ΔSb= ｜(Cb_{MAX} - Cb_{MIN}) / V_{OUT} ｜×100 (%)

7. V_{DARK}

① Measure the average value of signal output at dark condition

8. DSNU

① Measure the voltage difference between minimum and maximum of dark signal

9. F_Y

① Set to SILC
② Measure the average value of signal output (V_{OUT})
③ Measure the difference of signal output between even field and odd field
④ FLK = (V_{OUT}/ V_{OUT}) ×100 (%)

10. F_{Cr}, F_{Cb}

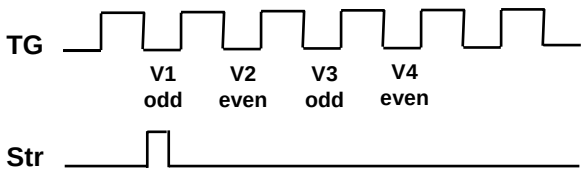
① Set to SILC using the R,B optical filter respectively
② Measure the average value of chroma signal output
③ Measure the difference of chroma signal output between even field and odd field
④ F_{Ci} = (ΔV_{CiOUT} / V_{CiOUT}) ×100 (%) (i = r,b)

11. L_{Cr}, L_{Cb}, L_{Cg}, L_{Cw}

① Set to SILC using the W,R,B,G optical filter respectively
② Measure the average value of signal output
③ Measure the difference of signal output between signal lines of the same field
(Δ Vlw, Δ Vlr, Δ Vlg, Δ Vlb)
④ Lci = (ΔVli_{OUT} / Vi_{OUT}) ×100 (%) (i = w,r,g,b)

12. Lag

① Light a strobe lamp as follow

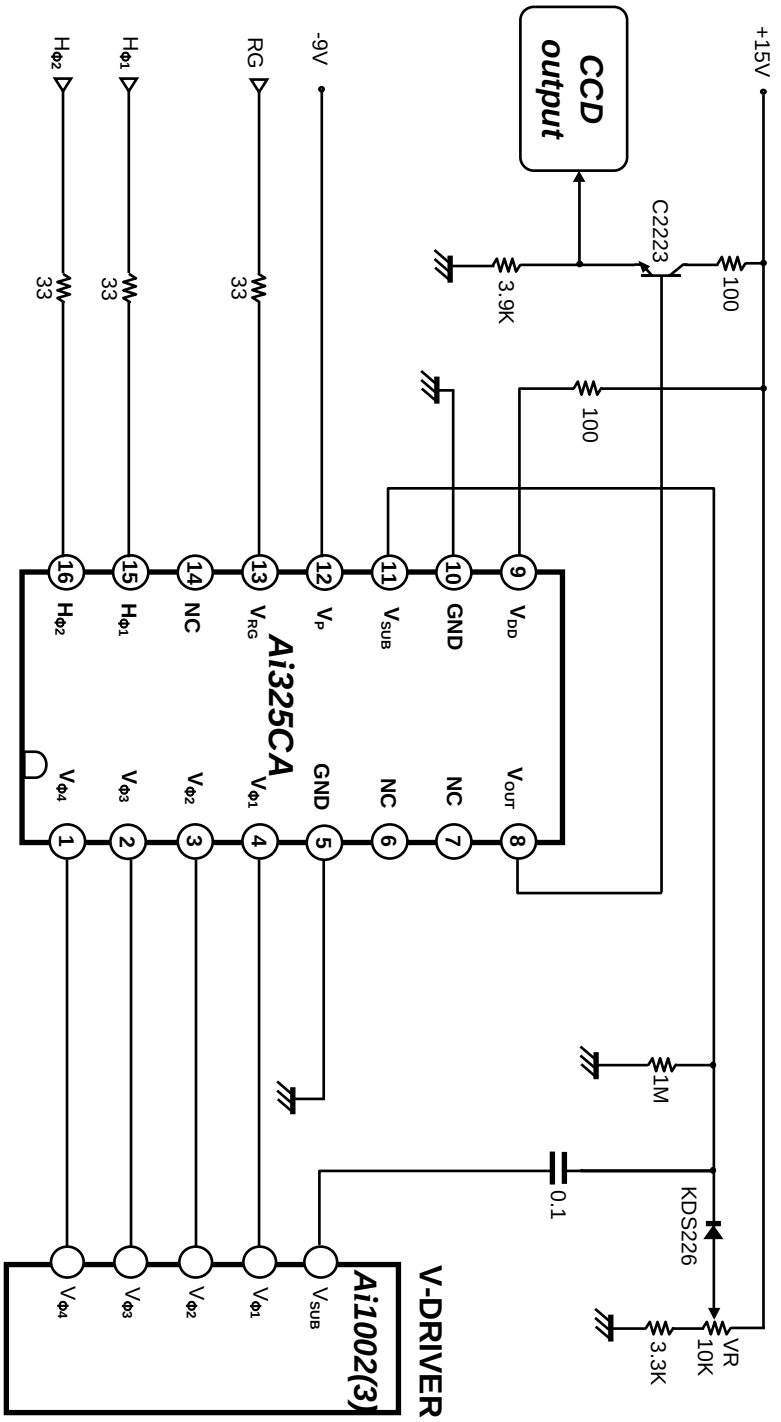


② Lag = { V2(out)+V3(out)+V4(out) } / V1(out)

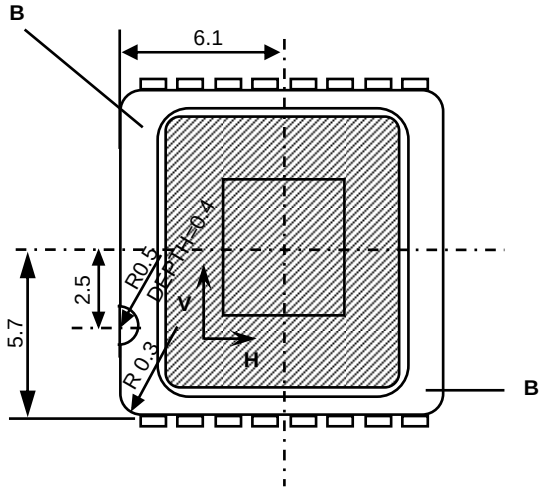
*** Standard Illumination Conditions**

① Measure the average value of output of linear region
② At this time, measure the light intensity of illumination at CCD face plate
③ Define SILC with above
④ Light source: Tungsten lamp(3100K)
⑤ Use a standard test lens at F8

APPLICATION CIRCUIT



PACKAGE DIMENSION (16 PIN PLASTIC-DIP)



UNIT = mm

1.The center of the effective image area relative to " B " and " B' "is (H, V) = (6.1, 5.7)±0.15mm.

2. The rotation angle of the effective image area relative to H and V is ±1.5°

: GLASS LID