adaptec

AIC™-33C94

Enhanced SCSI Bus Controller

Product Highlights

- Synchronous SCSI data transfer rate up to 10 MBps

- Programmable 128-word Writable Control Store for handling SCSI protocol and data transfer

- Support for SCSI Configured automatically (SCAM) protocol with low-level SCSI bus control

- Split-bus architecture with dedicated 8-bit microprocessor interface and integrated DMA controller, programmable to be bus master or slave

- 32-word by 9-bit dual port registers to store commands, messages, and status

Overview

The Adaptec® AIC-33C94 Enhanced SCSI Bus Controller (ESBC) is ideal for the needs of today's peripheral systems. SCSI command automation coupled with custom programmability provides a flexible solution for OEM designers. These features, integrated into a system with Adaptec host systems, deliver end-to-end compatibility and leading-edge performance.

Key Benefits

Fast, efficient data transfer

The AIC-33C94 ESBC controls data transfers between the 8-bit SCSI bus and the local data buffer. A split-bus architecture provides separate CPU and DMA buses that enable concurrent operations for optimum performance. The CPU bus is a dedicated 8-bit microprocessor interface. The 16-bit DMA bus is programmable to handle either 8-bit or 16-bit transfers, delivering a maximum data transfer rate of 10 MBps in 8-bit mode or 20 MBps in 16-bit mode. The total time required to perform arbitration, selection, command transfer, and message transfer is less than 20 microseconds.

A 32-byte on-chip RAM buffer enables the storage of command, message, and status bytes, reducing code development and ensuring more efficient operation by reducing the burden on the CPU. A pipelined 24-bit transfer counter, specifiable in bytes or blocks, enables larger data transfers to be performed with a single command.

Programming flexibility

The AIC-33C94 controllers can handle SCSI protocol and data transfer through a 128-word Writable Control Store (WCS), which allows developers to program any sequence of SCSI bus phases. The AIC-33C94 controller can act as a target as well as an initiator.

Simplified development

An advantage of the AIC-33C94 controller is ease of development. An evaluation kit is available that helps speed time to market. It includes an evaluation board with sample WCS, SCSI, and SCAM Level 1 and Level 2 codes that can be quickly customized. Easy-to-follow flow charts and application notes provide step-by-step programming guidance. Either target or initiator mode can be emulated for evaluation and debugging.

Power management

For implementations where power consumption is an issue, the AIC-33C94 controller features an automatic sleep mode. If the controller is idle for a specified period of time, it powers down. It goes back into operation within 200 nanoseconds. This feature is beneficial for portable-based applications.

AIC-33C94 Features Summary

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1 stop bit, no parity)

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AIC-33C94 ESBC Technical Information

Features:
- Automatic response to a bus-initiated selection/reselection
- 16-word FIFO to support synchronous offset up to 32 bytes
- Programmable synchronous transfer period
- Pipelined 24-bit transfer counter
- Transfers that can be specified in bytes or logical blocks
- Microprocessor that also accesses the internal registers through the DMA bus
- All the signals needed for users to interface 8-bit differential bus
- Power-down mode if not active
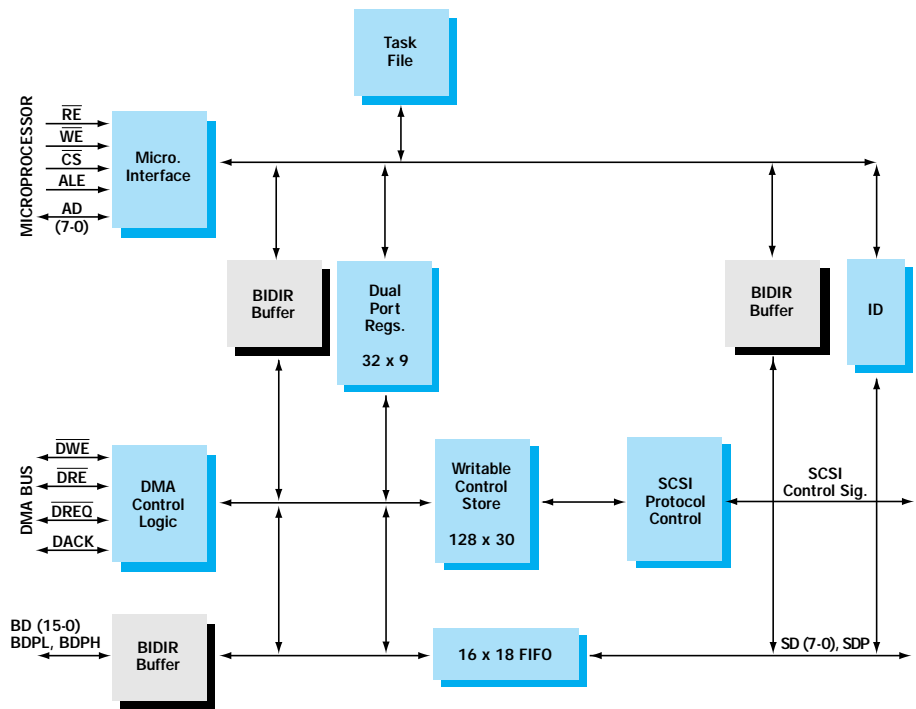
Applications:
Tape drives
CD-ROMs
Printers
Scanners
Copiers
DVDs
Analyzers
Voice mail
Instrumentation

Packaging: 100-pin MQFP

Design Support Tools: Demo94 Board
WCS assembler and sample codes
SCAM sample codes
Sample schematics
Application Notes

AIC-33C94 Enhanced SCSI Bus Controller Architecture