5-bit DAC, Synchronous PWM Power Regulator with Triple Linear Controllers

FEATURES

- Compatible with HIP6021.
- Provides 4 Regulated Voltages for Microprocessor Core, AGP Bus, Memory and GTL Bus Power.
- TTL Compatible 5-bit Digital-to-Analog Core Output Voltage Selection. Range from 1.3V to 3.5V.
  - 0.1V Steps from 2.1V to 3.5V.
  - 0.05V Steps from 1.3V to 2.05V.
- ±1.0% Output Voltage for VCORE, ±3.0% Accuracy for Linear Controller Outputs.
- Simple Voltage-Mode PWM Control and Built in Internal Compensation Networks.
- N-Channel MOSFET Driver for PWM Buck Converter.
- Linear Controller Drives Compatible with both N-Chanel MOSFET and NPN Bipolar Series Pass Transistor.
- Operates from +3.3V, +5V and +12V Inputs.
- Fast Transient Response.
- Full 0% to 100% Duty Ratios.
- Adjustable Current Limit without External Sense Resistor.
- Microprocessor Core Voltage Protection against Upper MOSFET shorted to +5V.
- Power Good Output Voltage Monitor.
- Over-Voltage and Over-Current Fault Monitors.
- 200KHz Free-Running Oscillator Programmable up to 700KHz.

APPLICATIONS

- Full Motherboard Power Regulation for Computers.

DESCRIPTION

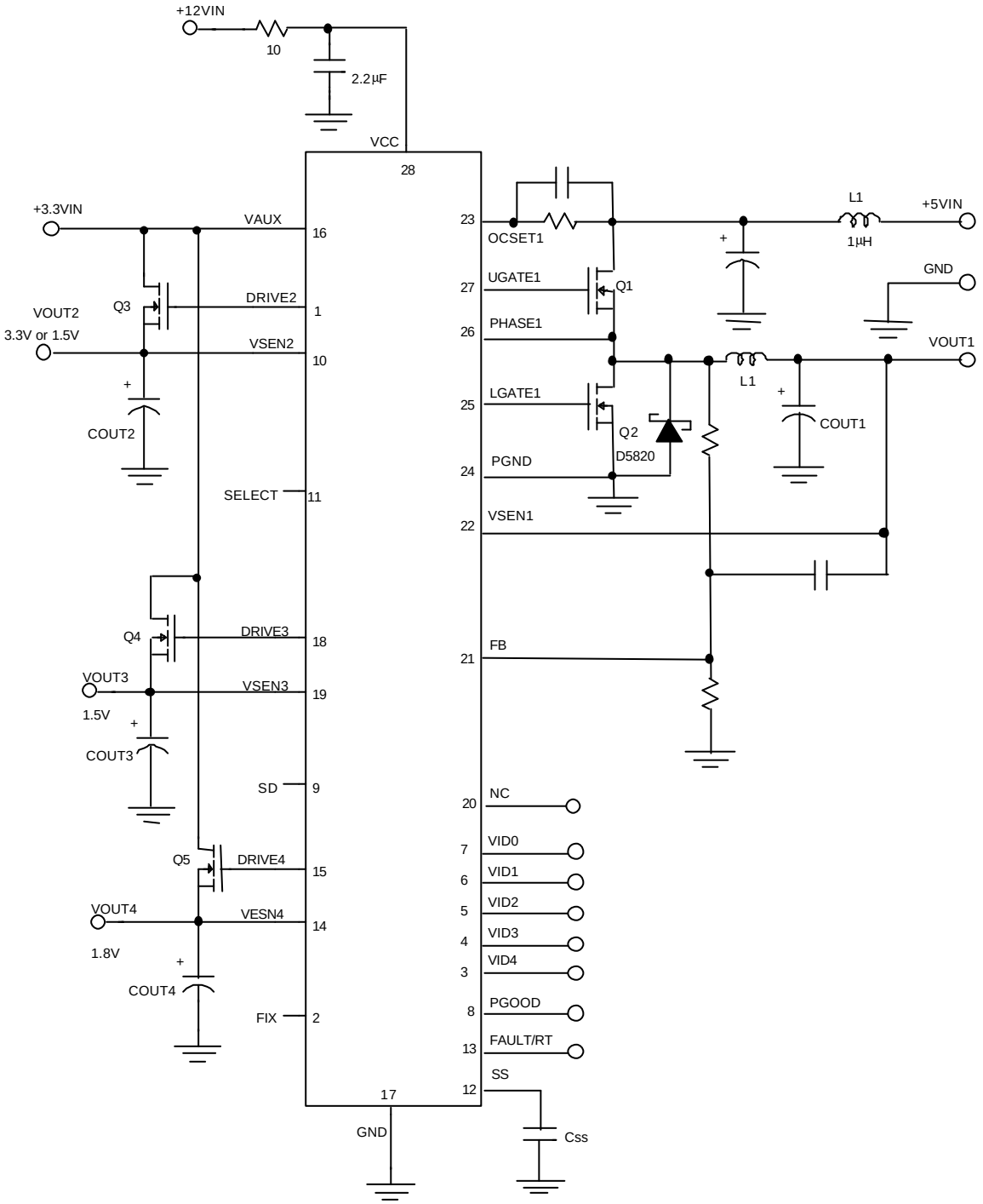
The AIC1574 combines a synchronous voltage mode controller with three linear controller as well as the monitoring and protection functions in this chip. The PWM controller regulates the microprocessor core voltage with a synchronous rectified buck converter. The three linear controllers regulate power for the 1.5V or 3.3V AGP bus power, the 1.5V GTL bus and the 1.8V power for the chip set core voltage and/or cache memory circuits.

An integrated 5 bit D/A converter that adjusts the core PWM output voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V increments. The linear controller for AGP bus power is selectable by TTL-compatible SELECT pin status for 1.5V or 3.3V with ±3% accuracy. The other two linear controller provide 1.5V±3% and 1.8V±3% or adjustable output voltage by means of external divided resistor based on FIX pin status.

This chip monitors all the output voltages. Power Good signal is issued when the core voltage is within ±10% of the DAC setting and the other levels are above their under-voltage levels. Over-voltage protection for the core output uses the lower N-channel MOSFET to prevent output voltage above 116% of the DAC setting.

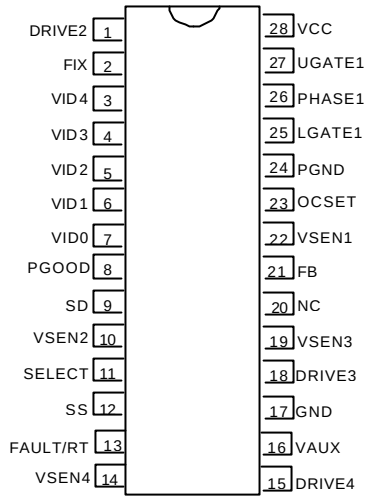
The PWM over-current function monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(ON)}$, eliminating the need for a current sensing resistor.

TYPICAL APPLICATION



ORDERING INFORMATION

AIC1574-CX
PACKAGING TYPE
S: SMALL OUTLINE

ORDER NUMBER	PIN CONFIGURATION
AIC1574CS (SO28)	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +15V

PGOOD, FAULT and GATE Voltage ..... GND -0.3V to V_{CC} +0.3V

Input, Output , or I/O Voltage ..... GND -0.3V to 7V

Recommended Operating Conditions

Supply Voltage; VCC..... +12V±10%
Ambient temperature Range ..... 0°C~70°C
Junction Temperature Range ..... 0°C~125°C

Thermal Information

Thermal Resistance, θ_{JA}

SOIC package ..... 70°C/W
SOIC package (with 3in^2 of copper) ..... 50°C/W

Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C ~ 150°C

Maximum Lead Temperature (Soldering 10 sec) ..... 300°C

TEST CIRCUIT

Refer to APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS (Vcc=12V, TJ=25°C, Unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC SUPPLY CURRENT						
Supply Current	UGATE, LGATE, GATE3 and VOUT2 open	I_{CC}		3		mA
POWER ON RESET						
Rising VCC Threshold	VOCSET=4.5V	V_{CCTHR}			10.4	V
Falling VCC Threshold	VOCSET=4.5V	V_{CCTHF}	8.2			V
Rising VAUX Threshold		$VAUX_{THR}$		2.5		V
VAUX Threshold Hysteresis		$VAUX_{HYS}$		500		mV
Rising VOCSET1 Threshold		V_{OCSETH}		1.26		V
OSCILLATOR						
Free Running Frequency	RT=Open	F	170	200	230	KHz
Total Variation	6kΩ<RT to GND<200kΩ		-15		+15	%
Ramp. Amplitude	RT=open	ΔV_{OSC}		1.5		VP-P
REFERENCE AND DAC						
DAC (VID0~VID4) Input Low Voltage		V_{IDL}			0.8	V
DAC (VID0~VID4) Input High Voltage		V_{IDH}	2.0			V
DACOUT Voltage Accuracy	V_{DAC}=1.8V~3.5V		-1.0		+1.0	%
Bandgap Reference Voltage		V_{REF}		1.265		V
Bandgap Reference Tolerance			-2.5		+2.5	%
LINEAR REGULATOR (OUT2, OUT3, OUT4)						
Regulation				3		%
VSEN2 Regulation Voltage	Select<0.8V	V_{REG2}		1.5		V
VSEN2 Regulation Voltage	Select>2.0V	V_{REG2}		3.3		V
VSEN3 Regulation Voltage		V_{REG3}		1.5		V
VSEN3 Regulation Voltage		V_{REG4}		1.8		V
Under-Voltage Level (V_{SEN}/V_{REG})	V_{SEN} Rising	V_{SENUV}		75		%
Under-Voltage Hysteresis (V_{SEN}/V_{REG})	V_{SEN} Falling			5		%
Output Drive Current (All Linears)	V_{AUX}-V_{DRIVE} > 0.6V		20	30		mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
SYNCHRONOUS PWM CONTROLLER AMPLIFIER						
DC Gain	(G.B.D.)			80		dB
Gain-Bandwidth Product	(G.B.D.)	G_{BWP}		13		MHz
Slew Rate	(G.B.D.) note 1.	S_R		6		V/μs
PWM CONTROLLER GATE DRIVER						
Upper Drive Source	V_{CC}=12V, V_{UGATE} = 6V	I_{UGH}		0.9		A
Upper Drive Sink	V_{UGATE}=1V	R_{UGL}		2.8	3.5	Ω
Lower Drive Source	V_{CC}=12V, V_{LGATE} =6V	I_{LGH}		1		A
Lower Drive Sink	V_{LGATE}=1V	R_{LGL}		2.2	3.0	Ω
PROTECTION						
VSEN1 Over-Voltage (V_{SEN1}/D_{ACOUT})	V_{SEN1} Rising	OVP		116	120	%
FAULT Sourcing Current	V_{CC}-$V_{FAULT/RT}$ =2.0V	I_{OVP}		20		mA
OCSET Current Source	V_{OCSET}=4.5VDC	I_{OCSET}	170	200	230	μA
Soft-Start Current		I_{SS}		25		μA
POWER GOOD						
V_{SEN1} Upper Threshold (V_{SEN1}/DA_{COUT})	V_{SEN1} Rising		108		111	%
V_{SEN1} Under-Voltage (VSEN1/DACOUT)	V_{SEN} Falling		92		95	%
V_{SEN1} Hysteresis (VSEN1/DACOUT)	Upper and Lower Threshold			2		%
P_{GOOD} Voltage Low	I_{PGOOD}=-4mA	V_{PGOOD}		0.4	0.8	V

Note 1. Without internal compensation network, the gain bandwidth product is 13MHz. Being associated with internal compensation networks, the Bode Plot is shown in Fig. 3, “Internal Compensation Gain of PWM Error Amplifier”.

TYPICAL PERFORMANCE CHARACTERISTICS

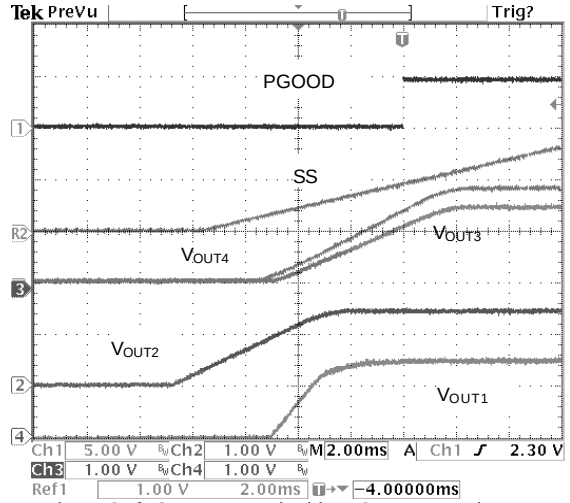


Fig. 1 Soft Start Interval with 4 Outputs and P_{GOOD}

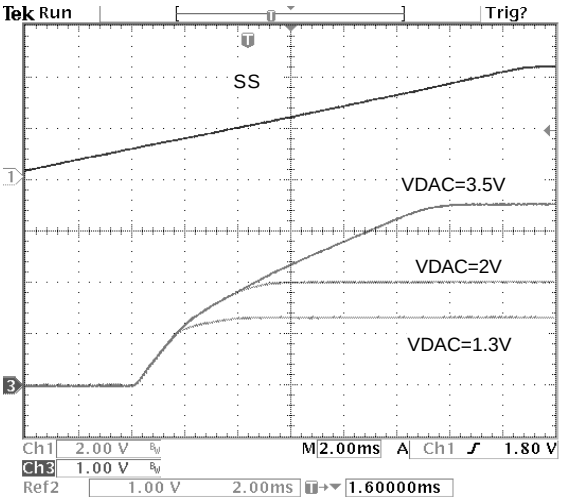


Fig. 2 Soft Start Initiates PWM Output

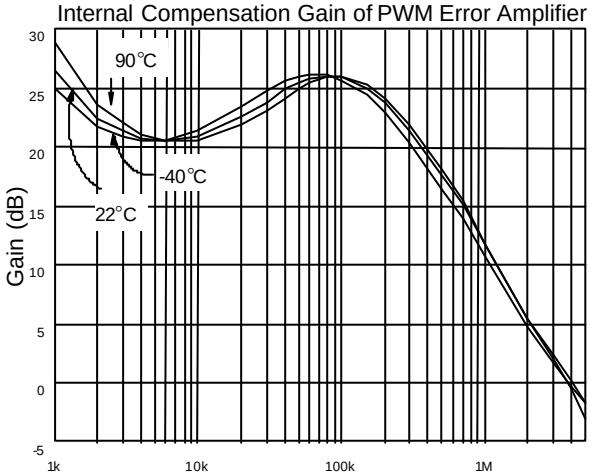


Fig. 3 Frequency (Hz)

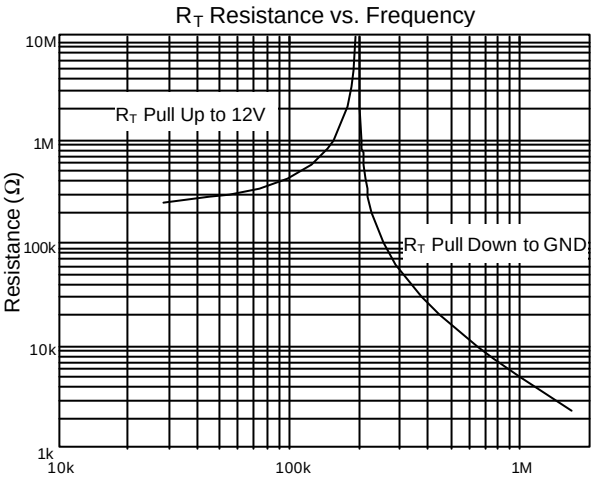


Fig. 4 Switching Frequency (Hz)

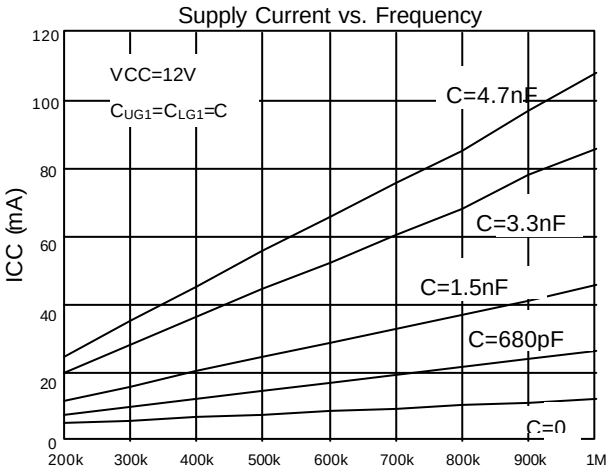


Fig. 5 Switching Frequency (Hz)

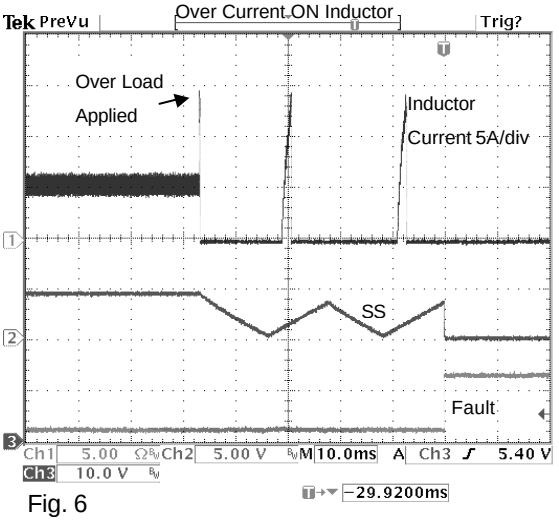


Fig. 6

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

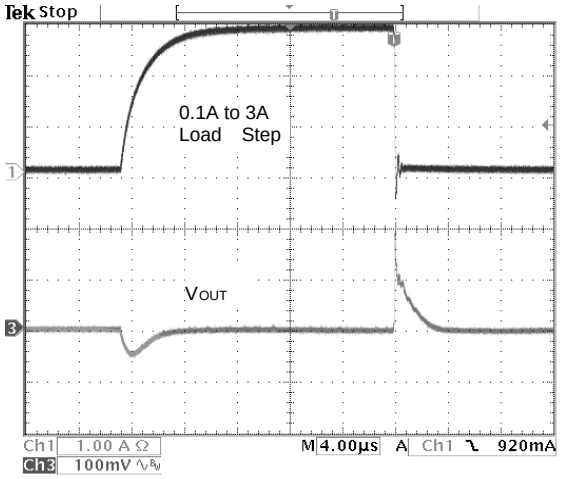


Fig. 7 Load Transient of Linear Controller

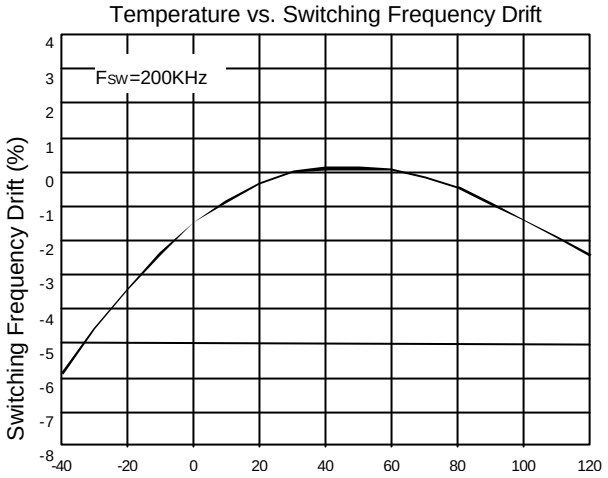


Fig. 8 Temperature (°C)

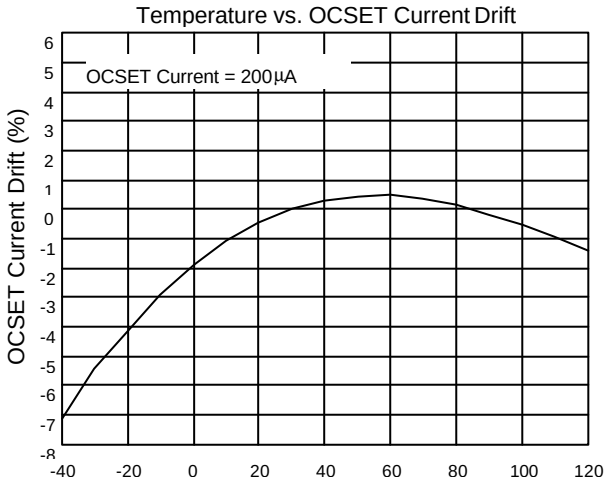


Fig. 9 Temperature (°C)

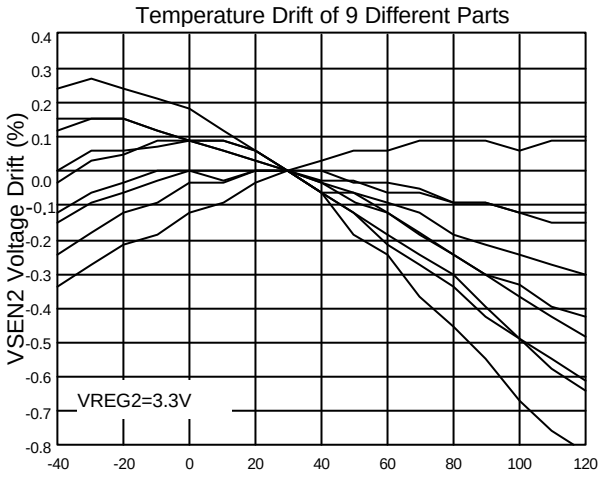


Fig. 10 Temperature (°C)

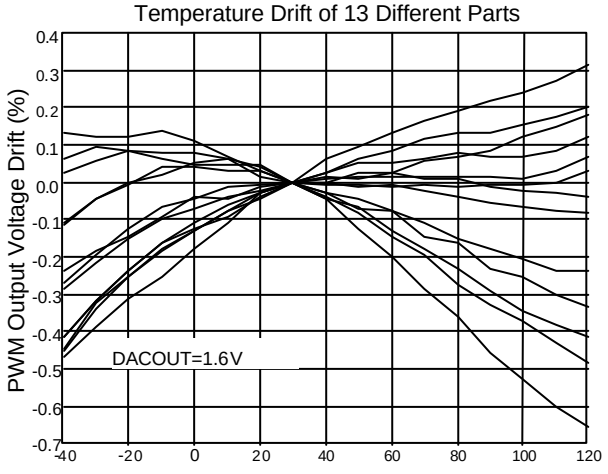


Fig. 11 Temperature (°C)

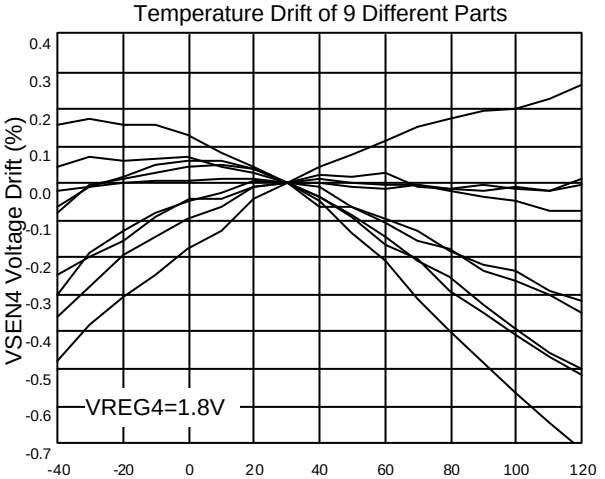


Fig. 12 Temperature (°C)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

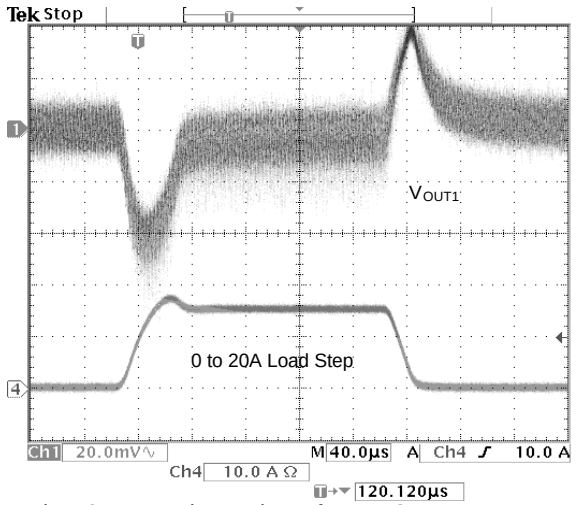


Fig. 13 Load Transient of PWM Output

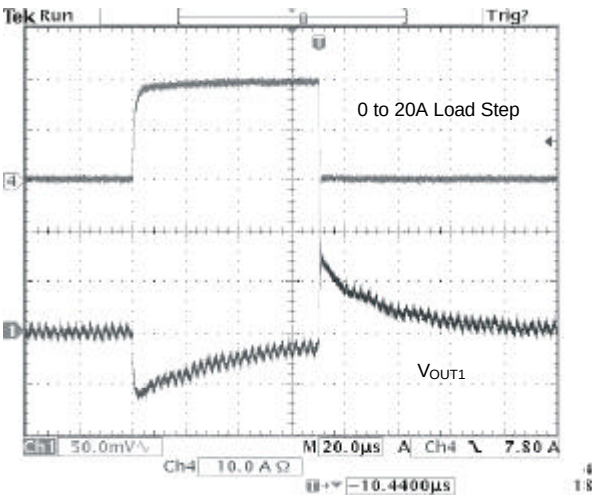


Fig. 14 Stringent Load Transient of PWM Output

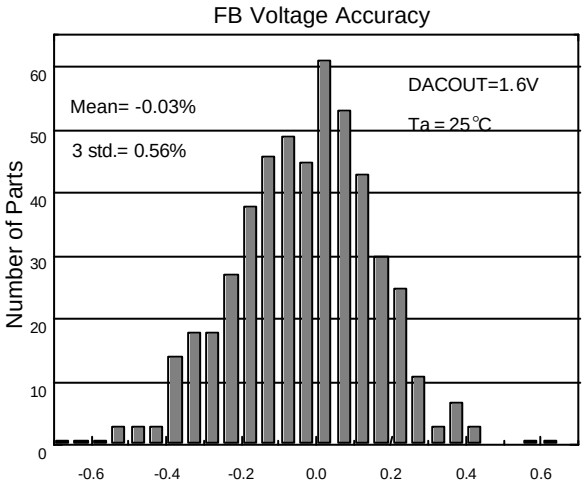


Fig. 15

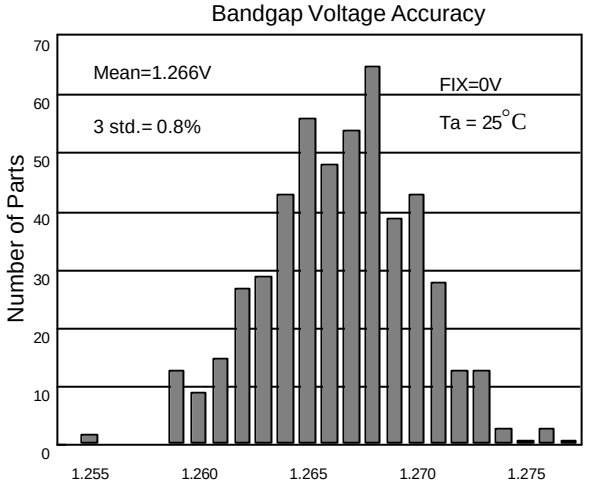
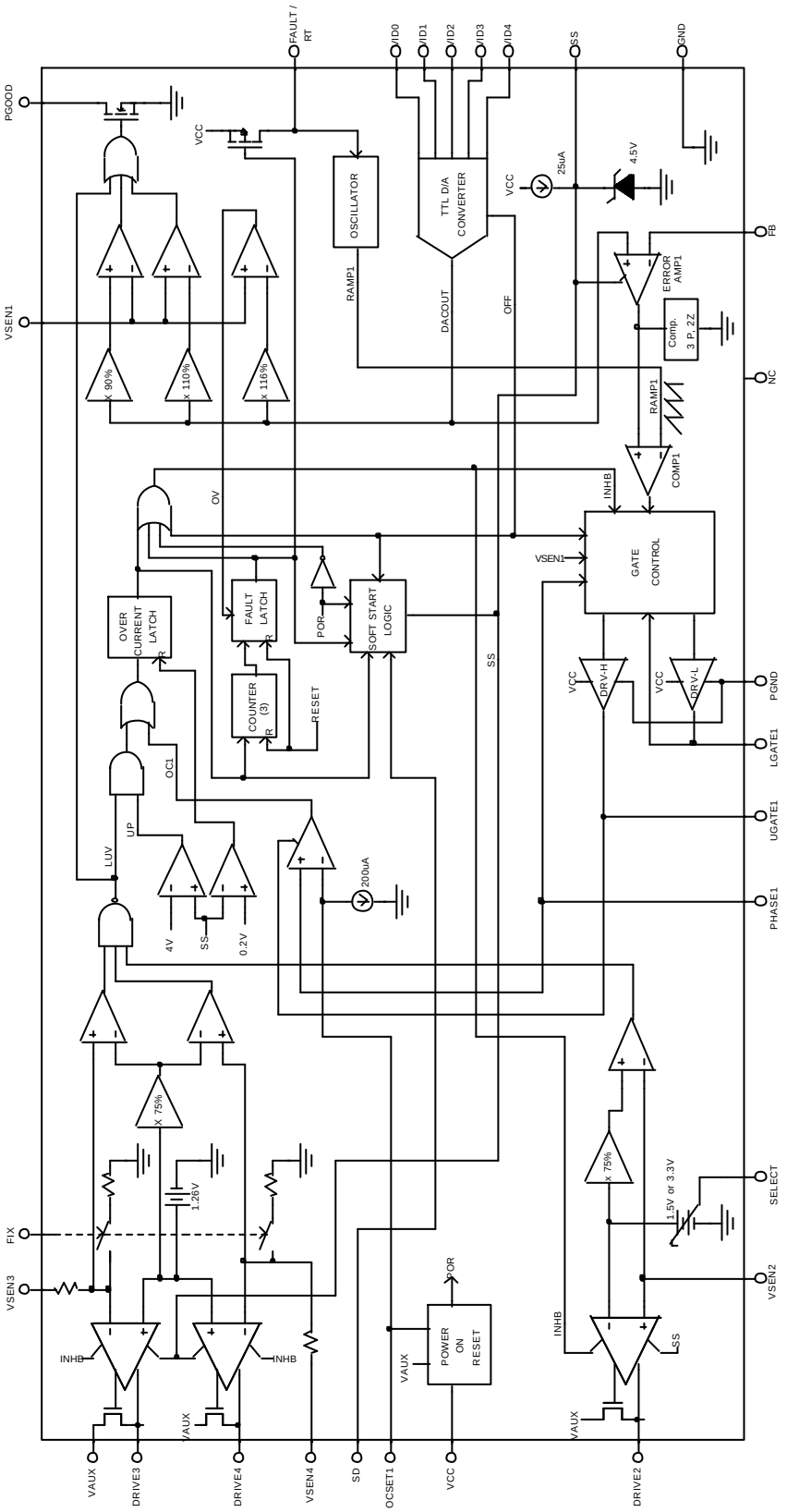


Fig. 16

BLOCK DIAGRAM



PIN DESCRIPTION

Pin 1: DRIVE2: Connect this pin to the Gate of the external N-MOS to supply AGP power.

Pin 2 : FIX: Left this pin open, its voltage is pulled high, enabling fixed output voltage operation for 1.5V and 1.8V linear regulators. If connect this pin to Ground, the new output voltage set by external resistors R_{GND} (Connected between VSEN and GND) and R_{OUT} (Connected between VSEN and VOUT) .

$$V_{OUT} = \frac{1.265V \times (R_{GND} + R_{OUT})}{R_{GND}}$$

Pin 7: VID4:
Pin 6: VID3:
Pin 5: VID2:
Pin 4: VID1:
Pin 3: VID0: 5bit DAC voltage select pin. TTL-compatible inputs used to set the internal voltage reference VDAC. When left open, these pins are internally pulled up to 5V and provide logic ones. The level of VDAC sets the converter output voltage as well as the PGOOD and OVP thresholds.

Table 1 specifies the VDAC voltage for the 32 combinations of DAC inputs.

Pin 8: PGOOD: Power good indicator pin. PGOOD is an open drain output. This pin is pulled low when the converter output is ±10% out of the VDAC reference voltage and the other outputs are below their under-voltage thresholds. The PGOOD output is open for VID codes that inhibit operation. See Table 1.

Pin 9 : SD: A TTL-compatibe logic level high signal applied this pin immediately discharges the soft-start capacitors, disabling all the outputs. Dedicated internal circuitry insures the core output voltage does not go nective during this process. When re-enabled, this IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down resistor, enabling operation.

Pin 10:VSEN2: Connect this pin to the output of the AGP linear regulator. The voltage at this pin is regulated to the 1.5V/3.3V predetermined by the logic Low/High level ststus of the SELECT pin. This pin is also monitored for under-voltage events.

Pin 11:SELECT: This pin determines the output voltage of the AGP bus linear regulator. A low TTL input sets the output voltage to 1.5V, while a high input sets the output voltage to 3.3V.

Pin 12:SS: Soft-start pin. Connect a capacitor from this pin to ground. This capacitor, along with an internal 25μA (typically) current source, sets the soft-start interval of the converter. Pulling this pin low will shut down the IC.

Pin 13: FAULT/RT: Frequency adjustment pin. Connecting a resistor (RT) from this pin to GND, increasing the frequency. Connecting a resistor (RT) from this pin to VCC, decreasing the frequency by the following figure (Fig. 4).

This pin is 1.26V during normal operation, but it is pulled to VCC in the event of an over-voltage or over-current condition.

$f = f_0\left(1+\frac{25.2K}{R_T}\right)$, R_T pulled to GND

$f = f_0\left(1-\frac{VCC-1.26V}{5\times R_T}\right)$, R_T pulled to VCC,

where f_0 is free run frequency.

Pin14: VSEN4: Connect this pin to the 1.8V linear regulator' s output. This pin is monitored for under-voltage events.

Pin15: DRIVE4: Connect this pin to the Gate of the external N-MOS to drive for the 1~8V power.

Pin 16: VAUX: This pin provides boost current for the linear regulator' s output. The voltage at this pin is also monitored for power-on-reset purpose.

Pin 17: GND: Signal GND for IC. All voltage levels are measured with respect to this pin.

Pin 18: DRIVE3: Connect this pin to the Gate of the external N-MOS for providing 1.5V power to GTL bus.

Pin 19: VSEN3: Connect this pin to the 1.5V linear regulator' s output. This pin is monitored for under-voltage events.

Pin 20: NC: Not Connected.

Pin 21: FB: The error amplifier inverting input pin.

Pin 22: VSEN1: Converter output voltage sense pin. Connect this pin to the converter output. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over-voltage protection function.

Pin 23: OCSET: Current limit sense pin. Connect a resistor R_{OCSET} from this pin to the drain of the external high-side N-MOSFET. R_{OCSET}, an internal 200μA current source (I_{OCSET}), and the upper N-MOSFET on-resistance ($R_{DS(ON)}$) set the over-current trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

Pin 24:PGND: Driver power GND pin. PGND should be connected to a low impedance ground plane in close to lower N-MOSFET source.

Pin 25: LGATE: Lower N-MOSFET gate drive pin.

Pin 26: PHASE: Over-current detection pin. Connect the PHASE pin to source of the external upper N-MOSFET. This pin detects the voltage drop across the upper N-MOSFET $R_{DS(ON)}$ for over-current protection.

Pin 27: UGATE: Connect UGATE to pin of the external upper N-MOSFET gate.

Pin 28: VCC: The chip power supply pin. It also provides the gate bias charge for all the MOSFETs controlled by the IC. Recommended supply voltage is 12V. The voltage at this pin is monitored for Power-On-Reset purpose.

APPLICATION INFORMATIONS

The AIC1574 is designed for microprocessor computer applications with 3.3V and 5V power, and 12V bias input. This IC has one synchronous PWM controller and three linear controllers. The PWM controller is designed to regulate the microprocessor core voltage (V_{OUT1}) by driving 2 MOSFETs (Q1 and Q2) in a synchronous rectified buck converter configuration. The core voltage is regulated to a level programmed by the 5-bit D/A converter. One of the linear controllers is designed to regulate the advanced graphic port (AGP) bus voltage (V_{OUT2}) to a digitally programmable level 1.5V or 3.3V. Selection of either output voltage is achieved by applying the proper logic level at the SELECT pin. The remaining two linear controllers supply the 1.5V GTL bus power (V_{OUT3}) and 1.8V memory power (V_{OUT4}). All linear controllers are designed to employ an external pass transistor.

The Power-On Reset (POR) function continually monitors the input supply voltage +12V at VCC pin, the 5V input voltage at OCSET pin, and the 3.3V input at VAUX pin. The POR function initiates soft-start operation after all three input supply voltage exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. An internal 25μA current source charges an external capacitor (C_{SS}) on the SS pin from 0V to 4.5V. The PWM error amplifier reference input (Non-inverting terminal) and output is clamped to a level proportional to the SS pin voltage. As the SS pin voltage slew from 1V to 4V, the output clamp generates PHASE pulses of increasing width that charge the output capacitors. After the the output voltage increases to approximately 70% of the set value, the reference input clamp slows the output voltage rate-to rise and provides a smooth transition to the final set voltage. Additionally, all linear regulator's reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a rapid and controlled output voltage rise.

Fig. 1 and Fig. 2 show the soft-start sequence for the typical application. The internal oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse width on PHASE pin increases. The interval of increasing pulse width continues until output reaches sufficient voltage to transfer control to the input reference clamp.

Each linear output initially follows a ramp. When each output reaches sufficient voltage the input reference clamp slows the rate of output voltage rise. The PGOOD signal toggles 'high' when all output voltage levels have exceeded their under-voltage levels.

Fault Protection

All four outputs are monitored and protected against

extreme overload. A sustained overload on any output or over-voltage on PWM output disable all converters and drive the FAULT/RT pin to VCC.

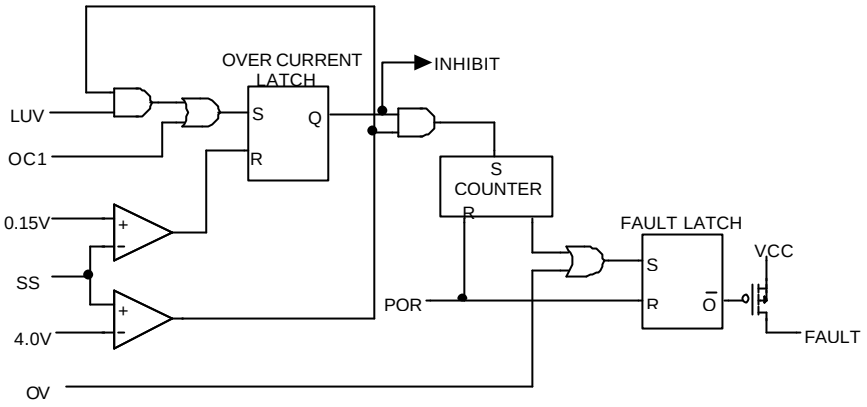


Fig. 17 Simplified Schematic of Fault Logic

A simplified schematic is shown in figure 17. An over-voltage detected on VSEN1 immediately sets the fault latch. A sequence of three over-current fault signals also sets the fault latch. An under-voltage event on either linear output (VSEN2, VSEN3, VSEN4) is ignored until the soft-start interval. Cycling the bias input voltage (+12V off then on) resets the counter and the fault latch.

Gate Drive Overlap Protection

The Overlap Protection circuit ensures that the Bottom MOSFET does not turn on until the Upper MOSFET source has reached a voltage low enough to ensure that shoot-through will not occur.

Over-Voltage Protection

During operation, a short on the upper PWM MOSFET (Q1) causes V_{OUT1} to increase. When the output exceed the over-voltage threshold of 116% of DACOUT, the FAULT pin is set to fault latch and turns Q2 on as required in order to regulate VOUT1 to 115% of DACOUT. The fault latch raises the FAULT/RT pin close to VCC potential.

A separate over-voltage circuit provides protection during the initial application of power. For voltage on VCC pin below the power-on reset (and above ~4V), should VSEN1 exceed 1.0V, the lower MOSFET (Q2) is driven on as needed to regulate VOUT1 to 1.0V.

Over-Current Protection

All outputs are protected against excessive over-current. The PWM controller uses upper MOSFET' s on-resistance, $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. All linear controllers monitor VSEN for under-voltage events to protect against excessive current.

When the voltage across Q1 ($I_D \cdot R_{DS(ON)}$) exceeds the level ($200\mu A \cdot R_{OCSET}$), this signal inhibit all outputs. Discharge soft-start capacitor (Css) with 25μA current sink, and increments the counter. Css recharges and initiates a soft-start cycle again until the counter increments to 3. This sets the fault latch to disable all outputs. Fig. 6 illustrates the over-current protection until an over load on OUT1.

Should excessive current cause VSEN to fall below

the linear under-voltage threshold, the LUV signal sets the over-current latch if C_{SS} is fully charged. Cycling the bias input power (off then on) reset the counter and the fault latch.

The over-current function for PWM controller will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The OC trip point varies with MOSFET' s temperature. To avoid over-current tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $R_{DS(ON)}$ at the temperature.

2. The minimum I_{OCSET} from the specification table.

3. Determine I_{PEAK} > $I_{OUT(MAX)}$ + (inductor ripple current) /2.

PWM OUT1 Voltage Program

The output voltage of the PWM converter is programmed to discrete levels between 1.3V to 3.5V. The VID pins program an internal voltage reference (DACOUT) through a TTL compatible 5 bit digital to analog converter. The VID pins can be left open for a logic 1 input, because they are internally pulled up to 5V by a 70KΩ resistor. Changing the VID inputs during operation is not recommended. All VID pin combinations resulting in an INHIBIT disable the IC and the open collector at the PGOOD pin.

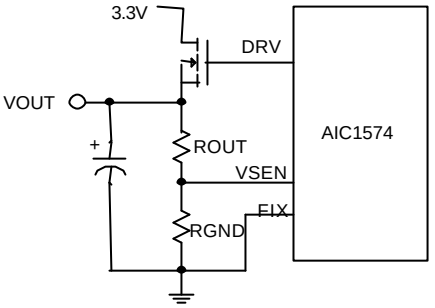
OUT2 Voltage Program

The AGP regulator output voltage is internally set to one of two discrete levels based on the SELECT pin status. Left SELECT pin open, internal pulled high, the output voltage is 3.3V. Grounding SELECT pin to GROUND will get the 1.5V output voltage.

The status of the SELECT pin can not be changed during operation of the IC without immediatelly causing a fault condition.

OUT3 and OUT4 Voltage Program

The GTL bus voltage (1.5V, OUT3) and the chip set and/or cache memorey voltage (1.8V,OUT4) are internally set for simpe, low cost implementation base on the FIX pin left open. Grounding FIX pin allows both output voltages to be set by means of external resistor dividers.



$$V_{OUT} = 1.265V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Adjusting the Output Voltage of OUTPUT 3 and 4

Shutdown

The AIC1574 features a dedicated shetdown pin (SD). A TTL-compatible logic high signal applied to this pin shuts down all four outputs and discharge the soft-start capacitor.

The VID codes resulting in an INHIBIT as shown in Table 1 also shut down the IC.

APPLICATION GUIDE LINES

Layout Considerations

Any inductance in the switched current path generates a large voltage spike during the switching interval. The voltage spikes can degrade efficiency,

radiate noise into the circuit, and lead to device over-voltage stress. Careful component selection and tight layout of critical components, and short, wide metal trace minimize the voltage spike.

A ground plane should be used. Locate the input capacitors (C_{IN}) close to the power switches. Minimize the loop formed by C_{IN}, the upper MOSFET (Q1) and the lower MOSFET (Q2) as possible. Connections should be as wide as short as possible to minimize loop inductance.

The connection between Q1, Q2 and output inductor should be as wide as short as practical. Since this connection has fast voltage transitions will easily induce EMI.

The output capacitor (C_{OUT}) should be located as close the load as possible. Because minimize the transient load magnitude for high slew rate requires low inductance and resistance in circuit board

The AIC1574 is best placed over a quiet ground plane area. The GND pin should be connected to the groundside of the output capacitors. Under no circumstances should GND be returned to a ground inside the C_{IN}, Q1, Q2 loop. The GND and PGND pins should be shorted right at the IC. This help to minimize internal ground disturbances in the IC and prevents differences in ground potential from disrupting internal circuit operation.

The wiring traces from the control IC to the MOSFET gate and source should be sized to carry peak current.

The Vcc pin should be decoupled directly to GND by a 2.2µF ceramic capacitor, trace lengths should be as short as possible.

Table 1 VOUT1 Voltage Program (0=connected to GND, 1=open or connected to 5V)

For all package versions											
PIN NAME					DACOUT	PIN NAME					DACOUT
VID4	VID3	VID2	VID1	VID0	VOLTAGE	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	1	1	1	1.30V	1	1	1	1	1	INHIBIT
0	1	1	1	0	1.35V	1	1	1	1	0	2.1 V
0	1	1	0	1	1.40V	1	1	1	0	1	2.2 V
0	1	1	0	0	1.45V	1	1	1	0	0	2.3 V
0	1	0	1	1	1.50V	1	1	0	1	1	2.4 V
0	1	0	1	0	1.55V	1	1	0	1	0	2.5 V
0	1	0	0	1	1.60V	1	1	0	0	1	2.6 V
0	1	0	0	0	1.65V	1	1	0	0	0	2.7 V
0	0	1	1	1	1.70V	1	0	1	1	1	2.8 V
0	0	1	1	0	1.75V	1	0	1	1	0	2.9 V
0	0	1	0	1	1.80 V	1	0	1	0	1	3.0 V
0	0	1	0	0	1.85 V	1	0	1	0	0	3.1 V
0	0	0	1	1	1.90 V	1	0	0	1	1	3.2 V
0	0	0	1	0	1.95 V	1	0	0	1	0	3.3 V
0	0	0	0	1	2.00 V	1	0	0	0	1	3.4 V
0	0	0	0	0	2.05 V	1	0	0	0	0	3.5 V

A multi-layer-printed circuit board is recommended. Figure 11 shows the connections of the critical components in the converter. The C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer.

PWM Output Capacitors

The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demand.

The ESR (equivalent series resistance) and ESL (equivalent series inductance) parameters rather than actual capacitance determine the buck capacitor values. For a given transient load magnitude, the output voltage transient change due to the output capacitor can be note by the following equation:

$$\Delta V_{OUT} = ESR \times \Delta I_{OUT} + ESL \times \frac{\Delta I_{OUT}}{\Delta T}$$, where ΔI_{OUT} is transient load current step.

After the initial transient, the ESL dependent term drops off. Because the strong relationship between output capacitor ESR and output load transient, the output capacitor is usually chosen for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

A common way to lower ESR and raise ripple

current capability is to parallel several capacitors. In most case, multiple electrolytic capacitors of small case size are better than a single large case capacitor.

Output Inductor Selection

Inductor value and type should be chosen based on output slew rate requirement, output ripple requirement and expected peak current. Inductor value is primarily controlled by the required current response time. The AIC1570 will provide either 0% or 100% duty cycle in response to a load transient. The response time to a transient is different for the application of load and remove of load.

$$t_{RISE} = \frac{L \times \Delta I_{OUT}}{V_{IN} - V_{OUT}}, \quad t_{FALL} = \frac{L \times \Delta I_{OUT}}{V_{OUT}}.$$

Where ΔI_{OUT} is transient load current step.

In a typical 5V input, 2V output application, a 3μH inductor has a 1A/μS rise time, resulting in a 5μS delay in responding to a 5A load current step. To optimize performance, different combinations of input and output voltage and expected loads may require different inductor value. A smaller value of inductor will improve the transient response at the expense of increase output ripple voltage and inductor core saturation rating.

Peak current in the inductor will be equal to the maximum output load current plus half of inductor ripple current. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f \times L \times V_{IN}};$$

f = AIC1574 oscillator frequency.

The inductor must be able to withstand peak current without saturation, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss

Input Capacitor Selection

Most of the input supply current is supplied by the input bypass capacitor, the resulting RMS current flow in the input capacitor will heat it up. Use a mix of input bulk capacitors to control the voltage overshoot across the upper MOSFET. The ceramic capacitance for the high frequency decoupling should be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedance. The buck capacitors to supply the RMS current is approximate equal to:

$$I_{RMS} = (1-D) \times \sqrt{D} \times \sqrt{I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{IN} \times D}{f \times L}\right)^2}$$

, where $D = \frac{V_{OUT}}{V_{IN}}$

The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage.

PWM MOSFET Selection

In high current PWM application, the MOSFET power dissipation, package type and heatsink are the dominant design factors. The conduction loss is the only component of power dissipation for the lower MOSFET, since it turns on into near zero voltage. The upper MOSFET has conduction loss and switching loss. The gate charge losses are proportional to the switching frequency and are dissipated by the AIC1574. However, the gate charge increases the switching interval, t_{SW}, which increase the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction tem-

perature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

$$P_{UPPER} = I_{OUT}^2 \times R_{DS(ON)} \times D + \frac{I_{OUT} \times V_{IN} \times t_{SW} \times f}{2}$$

$$P_{LOWER} = I_{OUT}^2 \times R_{DS(ON)} \times (1 - D)$$

The equations above do not model power loss due to the reverse recovery of the lower MOSFET' s body diode.

The $R_{DS(ON)}$ is different for the two previous equations even if the type devices is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Logic level MOSFETs should be selected based on on-resistance considerations, $R_{DS(ON)}$ should be chosen base on input and output voltage, allowable power dissipation and maximum required output current. Power dissipation should be calculated based primarily on required efficiency or allowable thermal dissipation.

Rectifier Schottky diode is a clamp that prevent the loss parasitic MOSFET body diode from conducting during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode' s rated reverse breakdown voltage must be greater than twice the maximum input voltage.

Linear Controller MOSFET Selection

The power dissipated in a linear regulator is :

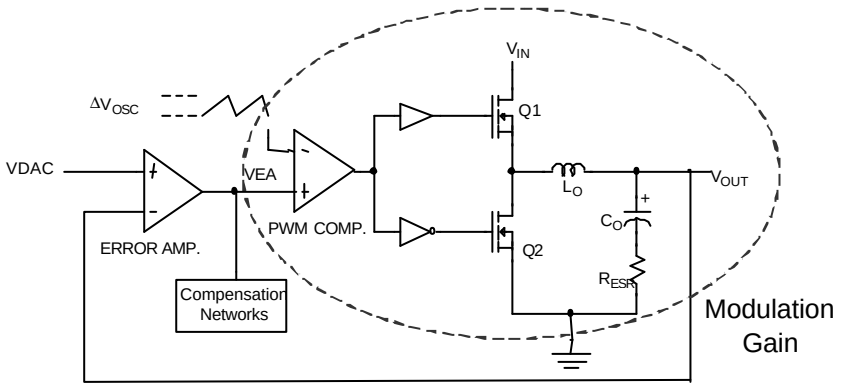
$$P_{LINEAR} = I_{OUT2} \times (V_{IN2} - V_{OUT2})$$

Select a package and heatsink that maintains junction temperature below the maximum rating while operation at the highest expected ambient temperature.

Linear Output Capacitor

The output capacitors for the linear regulator and linear controller provide dynamic load current. The linear controller uses dominant pole compensation integrated in the error amplifier and is insensitive to output capacitor selection. C_{OUT2}, C_{OUT3} and C_{OUT4} should be selected for transient load regulation.

PWM Feedback Analysis



The compensation network consists of the error amplifier and built in compensation networks. The goal of the compensation network is to provide for fast response and adequate phase margin. Phase Margin is the difference between the closed loop phase at 0dB and 180 degree.

Closed Loop Gain(dB) = Modulation Gain(dB) + Compensation Gain (dB)

Modulation Gain(dB)

$$\approx 20\log\left(\frac{V_{IN}}{\Delta V_{OSC}}\right)+10\log\left(1+\left(\frac{F}{F_{ESR}}\right)^2\right)$$

$$-10\log\left(\left[1-\left(\frac{F}{F_{LC}}\right)^2\right]^2+\left(\frac{F}{F_{LC}\times Q}\right)^2\right)$$

where

$$F_{LC}=\frac{1}{2p\sqrt{L_O C_O}};$$

$$F_{ESR}=\frac{1}{2p\times R_{ESR}\times C_O};$$

$$\frac{1}{Q}=\sqrt{\frac{C_O}{L_O}}\times R_{ESR}+\sqrt{\frac{L_O}{C_O}}\times\frac{1}{R_{LOAD}}$$

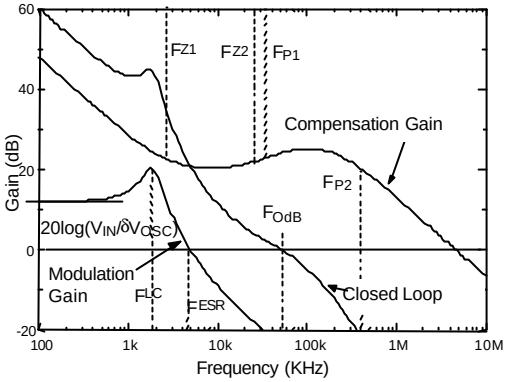
The break frequency of Internal Compensation Gain are given by

$F_{Z1}=2.6KHz$;

$F_{Z2}=24KHz$;

$F_{P1}=30KHz$;

$F_{P2}=400KHz$

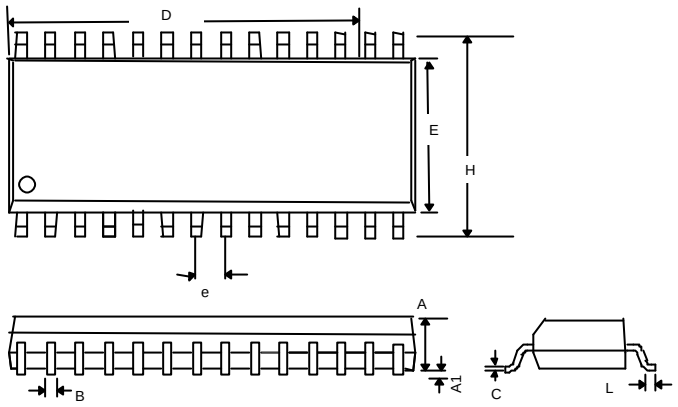


Bode Plot of Converter Gain

Sampling theory shows that F_{0dB} must be less that half the switching frequency for the loop stables. But it must be considerably less than that, or there will be large amplitude switching frequency ripple at the output. Thus, the usual practices is to fix F_{0dB} at 1/4 to 1/5 the switching frequency.

PHYSICAL DIMENSIONS

- **28 LEAD PLASTIC SO (unit: mm)**



SYMBOL	MIN	MAX
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	17.70	18.10
E	7.40	7.60
e	1.27 (TYP)	
H	10.00	10.65
L	0.40	1.27