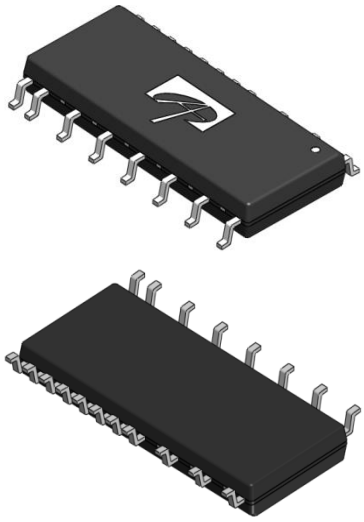
AIM705M25V1

Intelligent Power Module

External View



Size: 18 x 7.5 x 2.5 mm

GREEN Product

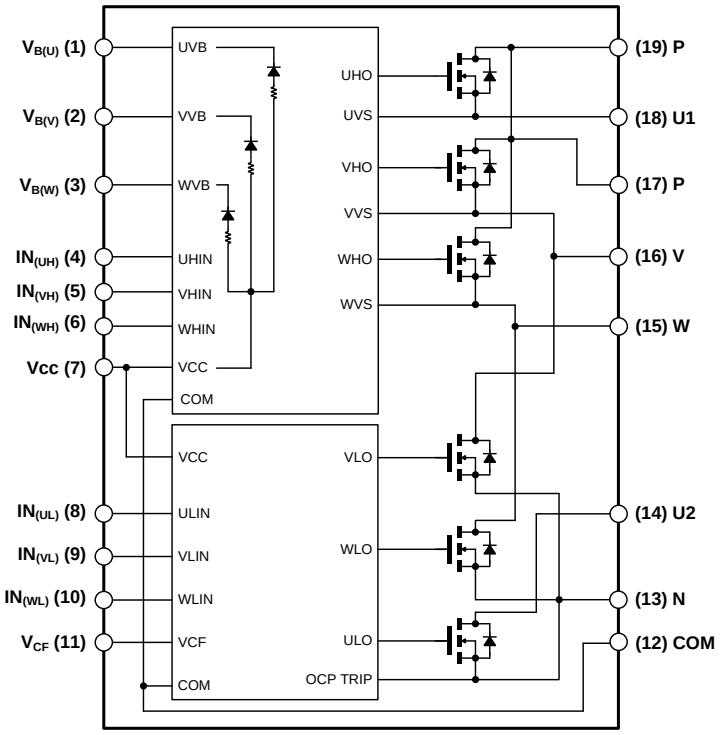
Features

- 250V, $R_{DS(on)}$ = 1.5Ω (Max)
- Advanced MOSFET technology for motor drives
- Low loss and EMI
- 3-phase Inverter module including HVIC drivers
- Wide input interface (3-18V), Schmitt trigger receiver circuit (Active High)
- Built-in bootstrap diodes with integrated current-limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Over-temperature (OT) protection
- Over-current protection (OCP)
- Controllable fault out signal (V_{CF}) corresponding to OC, UV, OT fault
- Isolation ratings of 1500Vrms/min

Applications

- AC 90~120Vrms class low power motor drives
- Fan motors

Internal Equivalent Circuit / Pin Configuration



Ordering Information

Part Number	Temperature Range	Package	Description
AIM705M25V1	-40°C to 150°C	IPM-7	N/A

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

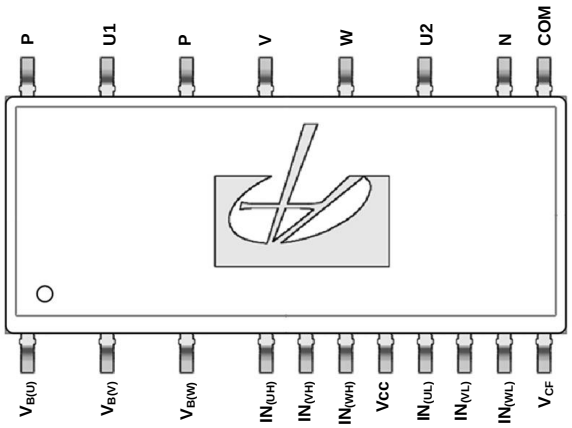


Figure 1. Pin Configuration

Pin Description

Pin Number	Pin Name	Pin Function
1	$V_{B(U)}$	High-Side Bias Voltage for U-phase MOSFET Driving
2	$V_{B(V)}$	High-Side Bias Voltage for V-phase MOSFET Driving
3	$V_{B(W)}$	High-Side Bias Voltage for W-phase MOSFET Driving
4	$IN_{(UH)}$	Signal Input for High-Side U-phase
5	$IN_{(VH)}$	Signal Input for High-Side V-phase
6	$IN_{(WH)}$	Signal Input for High-Side W-phase
7	V_{CC}	Control Supply Voltage
8	$IN_{(UL)}$	Signal Input for Low-Side U-phase
9	$IN_{(VL)}$	Signal Input for Low-Side V-phase
10	$IN_{(WL)}$	Signal Input for Low-Side W-phase
11	V_{CF}	Controllable Fault Output
12	COM	Common Supply Ground
13	N	Negative DC-Link Input
14	U2	Output for U-phase (connect to U1)
15	W	Output for W-phase
16	V	Output for V-phase
17	P	Positive DC-Link Input
18	U1	Output for U-phase (connect to U2)
19	P	Positive DC-Link Input

Absolute Maximum Ratings (T_J=25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Ratings	Units
Inverter				
BV_{DSS}	MOSFET Breakdown Voltage	T_J=25°C	250	V
I_D	MOSFET Drain Current (Continuous)	T_C=25°C	2	A
		T_C=80°C	1.5	A
I_{DP}	MOSFET Drain Current (Pulsed)	T_C=25°C, <100µs pulse width	3	A
P_D	Maximum Power Dissipation	T_C=25°C	8	W
T_J	Operating Junction Temperature		-40 to 150	°C
Control (Protection)				
V_{CC}	Control Supply Voltage	V_{CC}-COM	-0.3 ~ 20	V
V_{BS}	High-Side Control Bias Voltage	$V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	-0.3 ~ 20	V
V_{IN}	Input Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM	-0.3 ~ V_{CC}+0.5	V
V_{CF}	Fault Output Supply Voltage	Applied between V_{CF}-COM	-0.3 ~ 5.5	V
Thermal Resistance				
$R_{th(j-c)}$	Junction to Case Thermal Resistance	All operating condition	12.5	°C/W
$R_{th(j-a)}$	Junction to Ambient Thermal Resistance	All operating condition	39	°C/W
Total System				
T_C	Module Case Operation Temperature	Measurement point of T_C is provided in Figure 2	-30 to 125	°C
T_{STG}	Storage Temperature		-40 to 150	°C
V_{ISO}	Isolation Voltage	60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

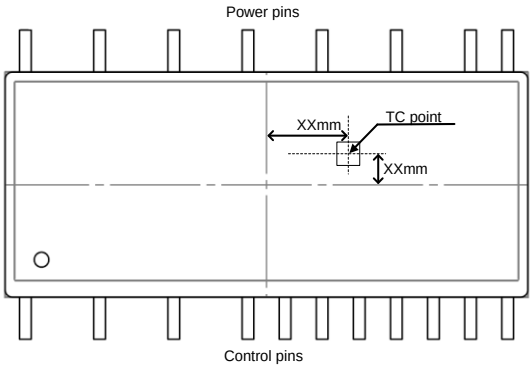


Figure 2. T_C Measurement Point

Recommended Operation Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{PN}	Bus Supply Voltage	Applied between P-N	0	140	200	V
V_{CC}	Control Supply Voltage	Applied between V_{CC}-COM	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	13.5	15.0	16.5	V
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation		-1	-	1	V/us
t_{dead}	Arm Shoot-Through Blocking Time	For each input signal	1.5	-	-	µs
f_{PWM}	PWM Input Frequency	-40°C < T_J < 150°C	-	16	-	kHz
$PW_{IN(ON)}$	Minimum Input Pulse Width (1)		0.7	-	-	µs
$PW_{IN(OFF)}$			0.7	-	-	µs

Note:

1. IPM may not respond if the input pulse width is less than $PW_{IN(ON)}$, $PW_{IN(OFF)}$.

Electrical Characteristics (T_J=25°C, unless otherwise specified)

Symbol	Parameter	Conditions		Min.	Typ.	Max	Units
Inverter							
BV_{DSS}	MOSFET Breakdown Voltage	I_D=1mA, V_{IN}=0V, T_J=25°C		250			V
I_{DSS}	Drain-Source Leakage Current	V_{IN}=0V, V_{DS}=250V		-	-	100	µA
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{CC}=V_{BS}=15V, V_{IN}=5V	I_D=1.0A	-	1.25	1.5	Ω
V_{SD}	MOSFET Body Diode Forward Voltage	V_{CC}=V_{BS}=15V, V_{IN}=0	I_{SD}=1.0A	-	0.9	1.3	V
t_{OFF}	Switching Times	V_{PN}=150V, V_{CC}=V_{BS}=15V I_D=1A, V_{IN}=0V↔5V Inductive load (high-side)		-	1100	-	ns
t_f				-	40	-	ns
t_{ON}				-	750	-	ns
t_r				-	60	-	ns
t_{rr}				-	120	-	ns
Control (Protection)							
I_{QCC}	Quiescent V_{CC} Supply Current	V_{CC}=15V, $IN_{(UL, VL, WL)}$=0V	V_{CC}-COM	-	-	1.5	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15V, $IN_{(UH, VH, WH)}$=0V	$V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	-	-	0.3	mA
UV_{CCT}	Supply Circuit Under-Voltage Protection	Trip Level		10.3	11.4	12.5	V
UV_{CCR}		Reset Level		10.8	11.9	13.0	V
UV_{BST}		Trip Level		9.0	10.0	11.0	V
UV_{BSR}		Reset Level		10.0	11.0	12.0	V
V_{OC}	Over-Current Protection	V_{CC}=15V		0.9	1.0	1.1	V
t_{OC_blk}	Over-Current Blanking Time			-	2	-	µs
OT_T	Over-Temperature Protection (2)	V_{CC}=15V, Detect LVIC Temperature	Trip Level	110	130	150	°C
OT_{HYS}			Hysteresis of Trip Reset	-	30	-	°C
V_{CFH}	Fault Output Voltage	V_N=0V		4.9	-	-	V
V_{CFL}		V_N=1V		-	-	0.5	V
V_{CF+}	CF positive going threshold			-	1.9	2.2	V
V_{CF-}	CF negative going threshold			0.8	1.1	-	V
t_{FO}	Fault Output Pulse Width (3)			20	-	-	µs
I_{IN}	Input Current	V_{IN}=5V		-	720	950	µA
$V_{th(on)}$	ON Threshold Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ –COM		-	-	2.5	V
$V_{th(off)}$	OFF Threshold Voltage			0.8	-	-	V
Bootstrap Diode							
V_{RRM}	Maximum Repetitive Reverse Voltage			600	-	-	V
$V_{F(BSD)}$	Bootstrap Diode Forward Voltage	I_F=10mA including voltage drop by limiting resistor		-	5.0	-	V
R_{BSD}	Bootstrap Diode Equivalent Resistance			-	500	-	Ω

Note:

2. When the LVIC temperature exceeds OT Trip temperature level (OT_T), OT protection is triggered and fault signal outputs.
3. At OC detection, F_O pulse width has a fixed width of minimum 20µs.

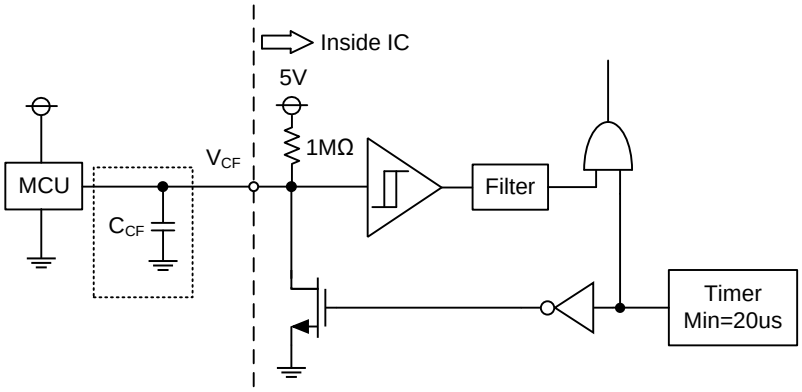


Figure 3. V_{CF} Output Circuit

(1) The V_{CF} pin provides an enable functionality that allows it to shut down the all low-side MOSFETs. When the V_{CF} pin is in the high state the IPM is able to operate normally. If the V_{CF} pin is in a low state, the low-side MOSFETs are turned off until the enable condition is restored.

(2) In addition, the V_{CF} pin can provide the fixed or adjustable pulse width of fault output signal for the OC protection.

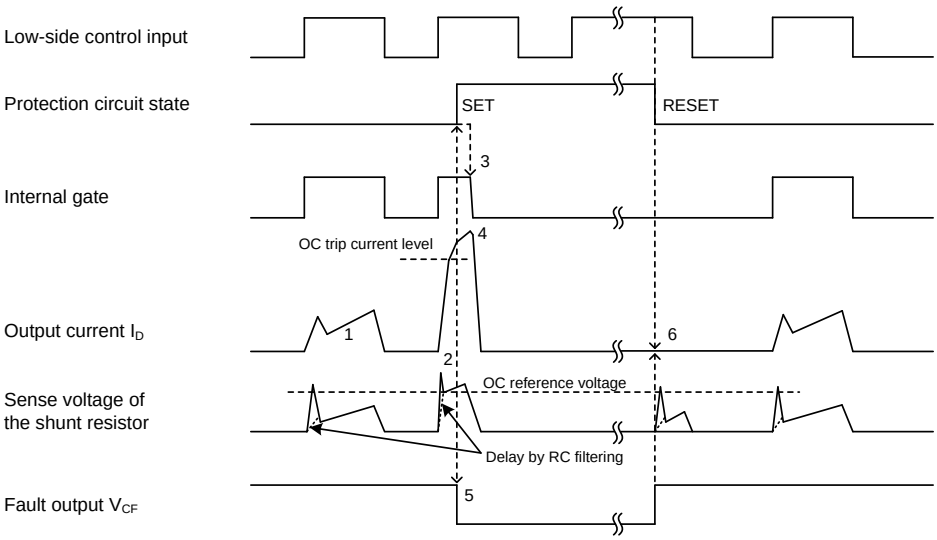
(3) If the V_{CF} pin is left, the pulse width is fixed at minimum 20us.

(4) If a capacitor is connected, the pulse width can be adjusted according to the capacitor value.

The length of pulse width is determined by the following formula ;

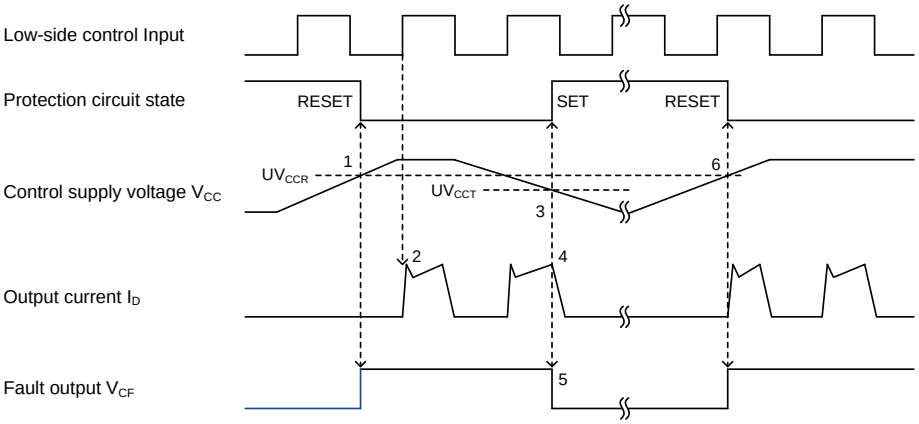
- t_{FO} = -(1MΩ*C_{CF})*ln(1-V_{CF}+/5V) + 100ns + 20us(min.)
- ex) C_{CF}=1nF, t_{FO}≈500us. Recommended parameters in the design are C_{CF} of ≤ 1nF.

Time Charts of the IPM Protective Function



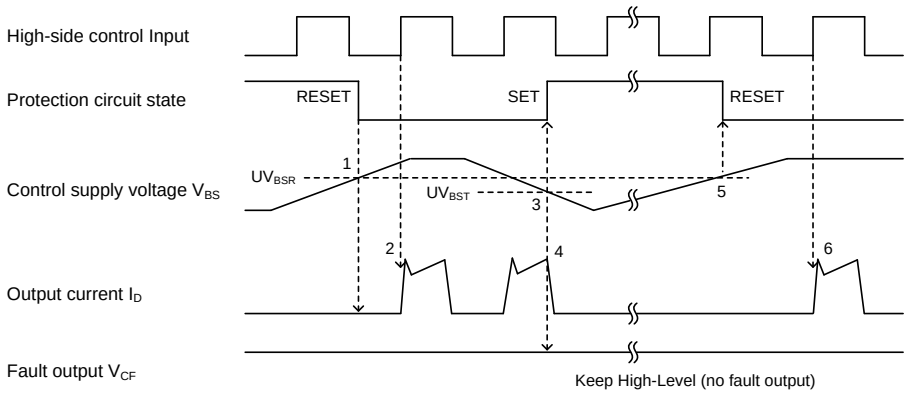
(1) Normal operation: MOSFET turns on and output current.
(2) Over-current detection (OCP triggered).
(3) All low-side MOSFETs' gate are turned off.
(4) Accordingly, all low-side MOSFETs are turned off.
(5) Fault signal outputs. F_O duration time (t_{FO}) is minimum 20μs.
(6) Fault output finishes. Normal operation starts according to the input control signal..

Figure 4. Over-Current Protection
(Low-side Operation Only with External Shunt Resistor and RC Filter)



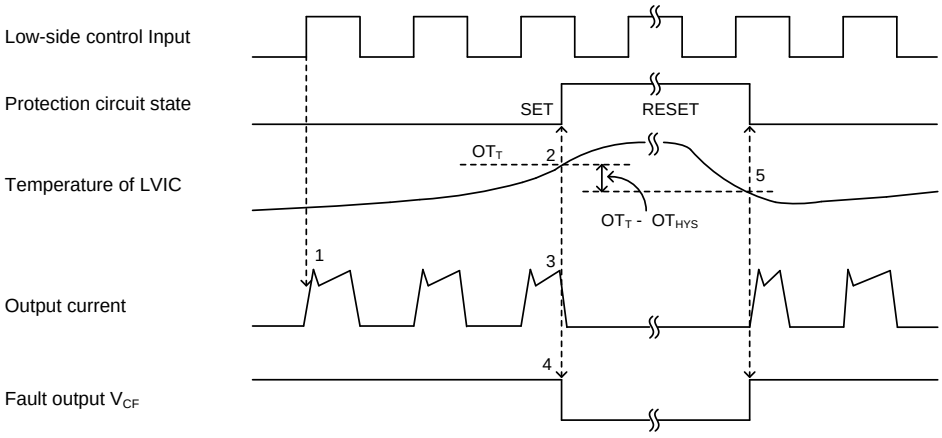
(1) Supply voltage V_{CC} becomes higher than under-voltage reset level (UV_{CCR}), and MOSFETs are turned on by the next ON signal.
(2) Normal operation: MOSFETs turn-on and output current.
(3) V_{CC} level drops to under-voltage trip level (UV_{CCT}).
(4) All low-side MOSFETs are turned off regardless of control input condition.
(5) F_O output is generated, and F_O stays low as long as V_{CC} is below UV_{CCR}.
(6) V_{CC} level reaches UV_{CCR}. Normal operation starts according to the input control signal.

Figure 5. Under-Voltage Protection (Low-side, UV_{CC})



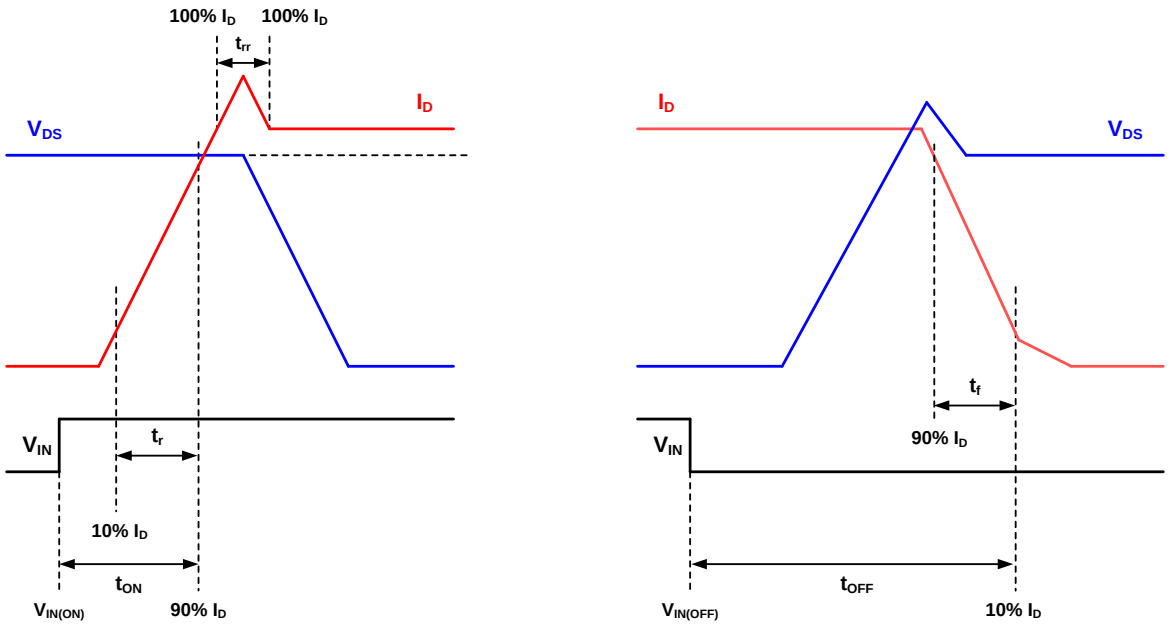
(1) Control supply voltage V_{BS} rises. After the voltage reaches under-voltage reset level (UV_{BSR}), MOSFETs are turned on by the next ON signal.
(2) Normal operation: MOSFETs turn on and output current.
(3) V_{BS} level drops to under-voltage trip level (UV_{BST}).
(4) All high-side MOSFETs are turned off regardless of control input condition.
(5) V_{BS} level reaches UV_{BSR}.
(6) Normal operation starts according to the input control signal.

Figure 6. Under-Voltage Protection (High-side, UV_{BS})



(1) Normal operation: MOSFETs turn on and output current.
(2) LVIC temperature exceeds over-temperature trip level (OT_T).
(3) All low-side MOSFETs are turned off regardless of control input condition.
(4) F_O output is generated, and F_O stays low as long as LVIC temperature is over OT_T.
(5) LVIC temperature drops to over-temperature reset level (OT_T-OT_{HYS}). Normal operation starts according to the input control signal.

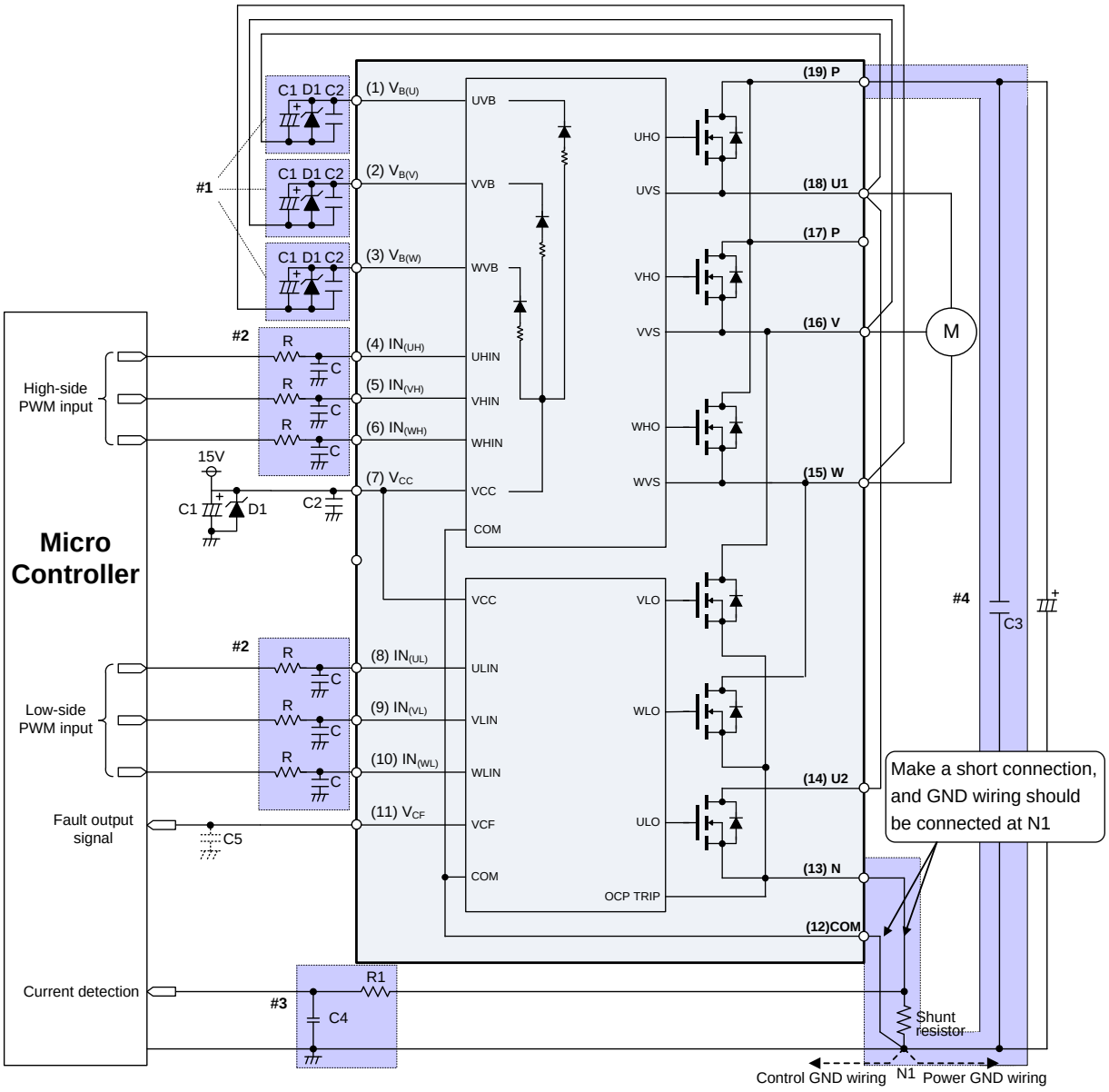
Figure 7. Over-Temperature Protection (Low-side, Detecting LVIC Temperature)



(a) Turn-on Waveform **(b) Turn-off Waveform**

Figure 8. Switching Times Definition

Example of Application Circuit



Recommended Component Values:	
(#1) C1:1~3.3μF, C2:100nF, D1:20V	(#2) R:100Ω, C:1nF
(#3) R1:1kΩ, C4:2nF	(#4) C3:0.1~0.22μF

(1) If the control GND is connected with the power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect the control GND and power GND at a point (N1), near the terminal of shunt resistor.

(2) A zener diode D1 (20V/1W) is recommended between each pair of control supply pins to prevent surge destruction.

(3) Prevention of surge destruction can further be improved by placing the bus capacitor as close to pin P and N1 as possible. Generally a 0.1~0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

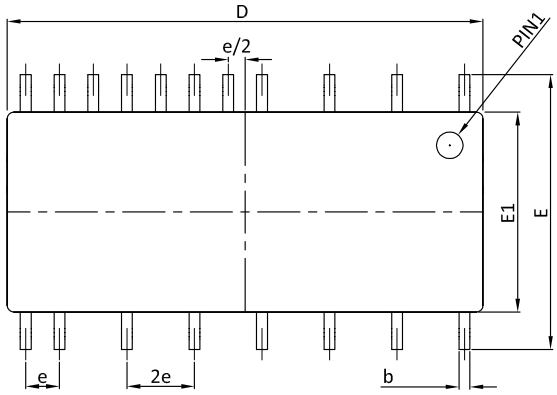
(4) When the current detection function is utilized by using the shunt resistor, the RC filter (R1 and C4) needs to be inserted to avoid the voltage spike noise in the current detection circuit. C4 should be placed as close to the controller as possible.

(5) It is recommended that all capacitors are mounted as close to the IPM as possible. (C1: electrolytic type with good temperature and frequency characteristics. C2: ceramic type with 0.1μF, good temperature, frequency and DC bias characteristics).

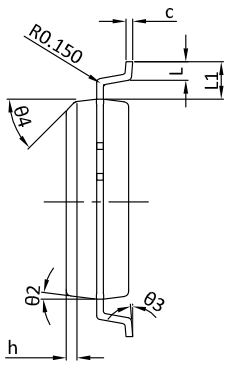
(6) To prevent malfunction, the layout to each input should be as short as possible. When using the RC coupling circuit (R: 100Ω, C: 1nF), place it as close to the IPM input pins as possible, and make sure the input signal levels meet the required turn-on and turn-off threshold voltages.

(7) The V_{CF} pin can provide the fault output signal with the fixed or adjustable pulse width for the OC protection. If the V_{CF} pin is left, the pulse width is fixed at minimum 20us. If a capacitor C5 is connected, the pulse width can be adjusted according to the capacitor value. For the design guide, please refer to the Figure 3.

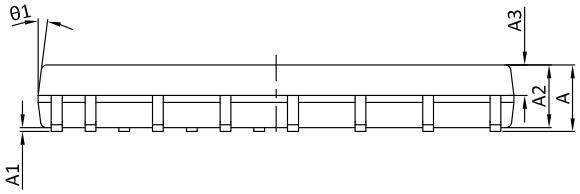
Package Dimensions, IPM-7



TOP VIEW



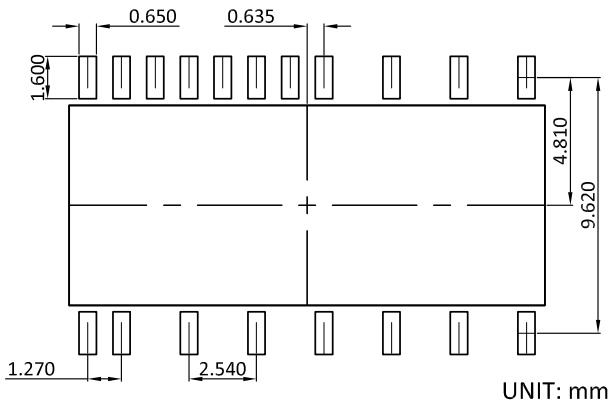
SIDE VIEW



SIDE VIEW

SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.304	2.504	2.704	0.091	0.099	0.106
A1	0.050	0.150	0.250	0.002	0.006	0.010
A2	2.254	2.354	2.454	0.089	0.093	0.097
A3	1.050	1.150	1.250	0.041	0.045	0.049
D	17.800	17.900	18.000	0.701	0.705	0.709
E	10.140	10.340	10.540	0.399	0.407	0.415
E1	7.420	7.520	7.620	0.292	0.296	0.300
L	0.505	0.705	0.905	0.020	0.028	0.036
L1	1.210	1.410	1.610	0.048	0.056	0.063
e	1.270TYP.			0.050TYP.		
b	0.410TYP.			0.016TYP.		
c	0.254TYP.			0.010TYP.		
θ1	7°TYP.			7°TYP.		
θ2	7°TYP.			7°TYP.		
θ3	0°	---	8°	0°	---	8°
θ4	45°TYP.			45°TYP.		
h	0.381TYP.			0.015TYP.		

LAND PATTERN RECOMMENDATIONS



UNIT: mm

NOTES

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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