AIP31021

96CH Segment Driver For Dot Matrix LCD

1、GENERAL DESCRIPTION

AIP31021 is a segment driver for dot matrix type LCD display. It features 96 channels with 48 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

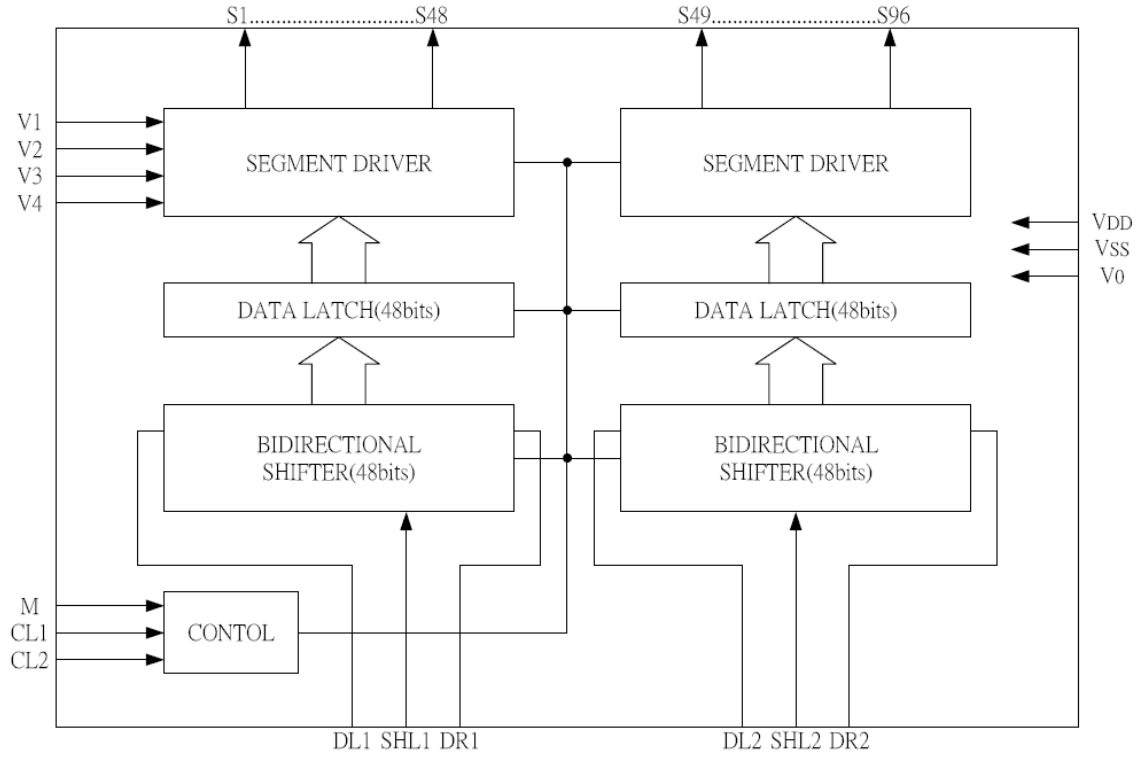
The AIP31021 can convert serial data received from an LCD controller, such as ST7920, into parallel data and send out LCD driving waveforms to the LCD panel. The AIP31021 is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment driver.

Features

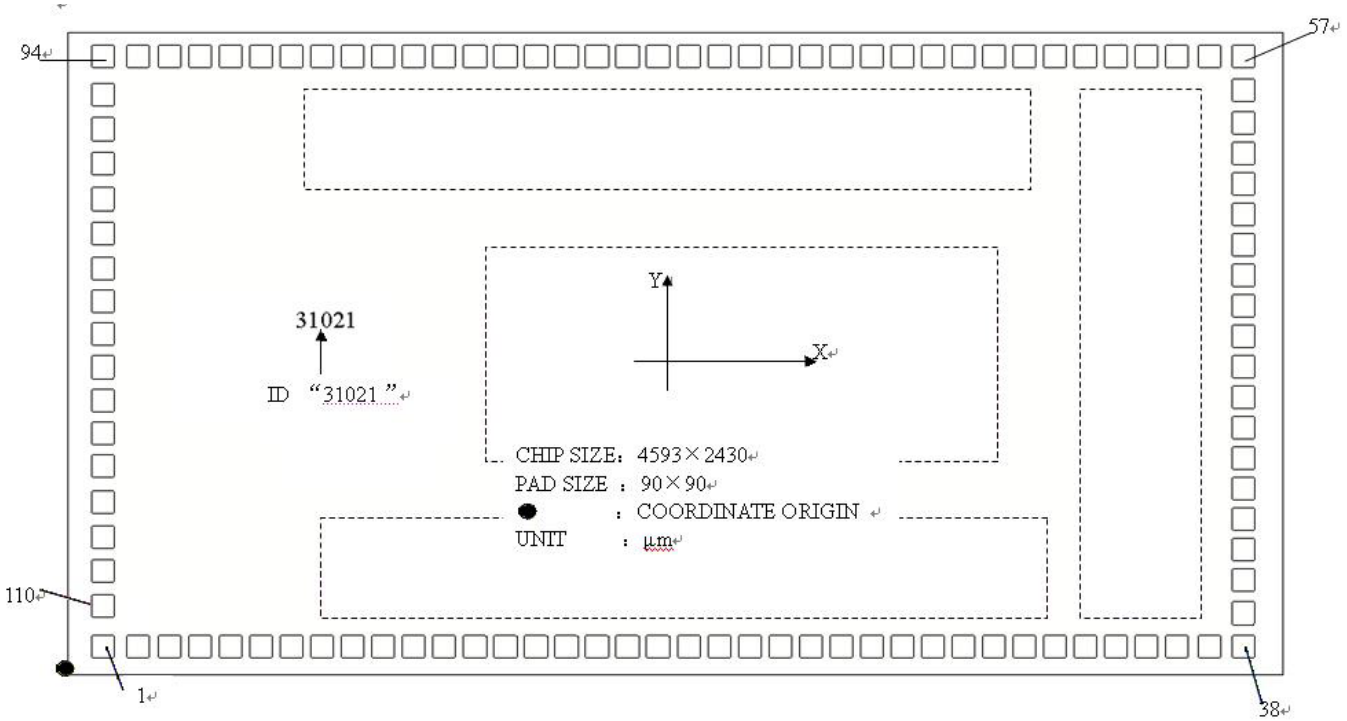
- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (V0~VSS) : 3V ~ 7V
- Dot matrix LCD driver with two 48 channel outputs
- Bias voltage (V0 ~ V4)
- Input/Output signals
  Input : Serial display data and control pulse from controller IC
  Output : 48 X 2 channels waveform for LCD driving
- Chip size: 4593×2430（μm×μm）.
- The IC substrate should be connected to Vss in the PCB layout artwork.
- bare chip available

2、BLOCK DIAGRAM AND PIN DESCRIPTION

2.1、BLOCK DIAGRAM



2.2、PAD DIAGRAM



2.3、PAD Location （UNIT:μm）

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	S50	55.00	55.00	56	S40	4538.00	2245.00
2	S51	186.50	55.00	57	S39	4538.00	2375.00
3	S52	316.50	55.00	58	S38	4406.50	2375.00
4	S53	436.50	55.00	59	S37	4276.50	2375.00
5	S54	556.50	55.00	60	S36	4156.50	2375.00
6	S55	676.50	55.00	61	S35	4036.50	2375.00
7	S56	796.50	55.00	62	S34	3916.50	2375.00
8	S57	916.50	55.00	63	S33	3796.50	2375.00
9	S58	1036.50	55.00	64	S32	3676.50	2375.00
10	S59	1156.50	55.00	65	S31	3556.50	2375.00
11	S60	1276.50	55.00	66	S30	3436.50	2375.00
12	S61	1396.50	55.00	67	S29	3316.50	2375.00
13	S62	1516.50	55.00	68	S28	3196.50	2375.00
14	S63	1636.50	55.00	69	S27	3076.50	2375.00
15	S64	1756.50	55.00	70	S26	2956.50	2375.00
16	S65	1876.50	55.00	71	S25	2836.50	2375.00
17	S66	1996.50	55.00	72	S24	2716.50	2375.00
18	S67	2116.50	55.00	73	S23	2596.50	2375.00
19	S68	2236.50	55.00	74	S22	2476.50	2375.00
20	S69	2356.50	55.00	75	S21	2356.50	2375.00
21	S70	2476.50	55.00	76	S20	2236.50	2375.00
22	S71	2596.50	55.00	77	S19	2116.50	2375.00
23	S72	2716.50	55.00	78	S18	1996.50	2375.00
24	S73	2836.50	55.00	79	S17	1876.50	2375.00
25	S74	2956.50	55.00	80	S16	1756.50	2375.00
26	S75	3076.50	55.00	81	S15	1636.50	2375.00
27	S76	3196.50	55.00	82	S14	1516.50	2375.00
28	S77	3316.50	55.00	83	S13	1396.50	2375.00
29	S78	3436.50	55.00	84	S12	1276.50	2375.00
30	S79	3556.50	55.00	85	S11	1156.50	2375.00
31	S80	3676.50	55.00	86	S10	1036.50	2375.00
32	S81	3796.50	55.00	87	S9	916.50	2375.00
33	S82	3916.50	55.00	88	S8	796.50	2375.00
34	S83	4036.50	55.00	89	S7	676.50	2375.00
35	S84	4156.50	55.00	90	S6	556.50	2375.00
36	S85	4276.50	55.00	91	S5]	436.50	2375.00

37	S86	4406.50	55.00	92	S4	316.50	2375.00
38	S87	4538.00	55.00	93	S3	186.50	2375.00
39	S88	4538.00	185.00	94	S2	55.00	2375.00
40	S89	4538.00	315.00	95	S1	55.00	2235.00
41	S90	4538.00	435.00	96	V0	55.00	2095.00
42	S91	4538.00	555.00	97	V2	55.00	1955.00
43	S92	4538.00	675.00	98	V3	55.00	1815.00
44	S93	4538.00	795.00	99	VSS	55.00	1679.00
45	S94	4538.00	915.00	100	VDD	55.00	1543.00
46	S95	4538.00	1035.00	101	CL1	55.00	1413.00
47	S96	4538.00	1155.00	102	SHL1	55.00	1283.00
48	S48	4538.00	1275.00	103	SHL2	55.00	1153.00
49	S47	4538.00	1395.00	104	CL2	55.00	1023.00
50	S46	4538.00	1515.00	105	DL1	55.00	893.00
51	S45	4538.00	1635.00	106	DR1	55.00	763.00
52	S44	4538.00	1755.00	107	DL2	55.00	623.00
53	S43	4538.00	1875.00	108	DR2	55.00	483.00
54	S42	4538.00	1995.00	109	M	55.00	343.00
55	S41	4538.00	2115.00	110	S49	55.00	199.00

2.4、PAD DESCRIPTION

Pin No.	Pin Name		I/O	Description
100	VDD	POWER	N/A	for logic
99	VSS	GROUND	N/A	for logic
96,97,98	V0 V2 V3	LCD Power	I	for LCD driving voltage
48~95	S1-S48	segment	O	LCD driver output for part 1
102	SHL1	direction	I	direction control for part 1 segments
105,106	DL1, DR1	data in /out	I/O	If SHL1 = 1 then DL1=out, DR1=in If SHL1 = 0 then DL1=in, DR1=out
110, 1~47	S49-S96	segment	O	LCD driver output for part 2
103	SHL2	direction	I	direction control for part 2 segments
107,108	DL2, DR2	data in/out	I/O	If SHL2 = 1 then DL2=out, DR2=in If SHL2 = 0 then DL2=in, DR2=out
109	M	alternation	I	Alternate the LCD driving waveform
101	CL1	latch clock	I	latch the data after shift is completed
104	CL2	shift clock	I	shift the data into the segments

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25 C, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	MIN.	MAX.	Unit
Supply Voltage	VDD	- 0.3	+7.0	V
Operating Temperature	TOPR	- 20	+85	℃
Storage Temperature	TSRG	- 55	+125	℃

3.2、ELECTRICAL CHARACTERISTICS

3.2.1、DC Characteristics

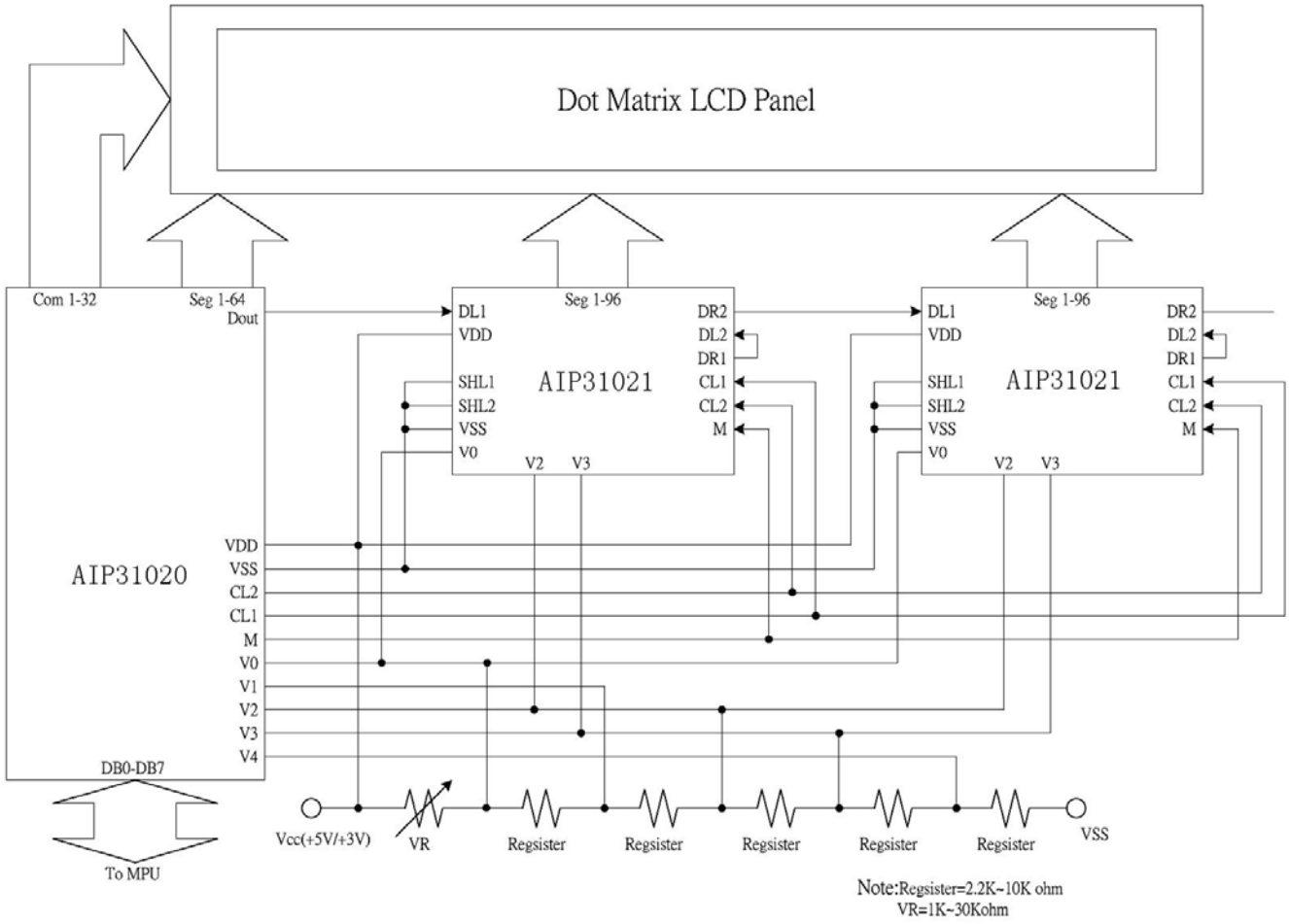
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Applicable pin
Operating Voltage	V_{DD}	-	2.7	-	5.5	V	-
Driver Supply Voltage	V_{LCD}	V_O-V_{SS}	3	-	7	V	-
Input High Voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V	CL1,CL2,M, SHL1,SHL2 DL1,DL2, DR1,DR2
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V	
Input Leakage Current	I_{LKG}	V_{IN}=0～V_{DD}	-5	-	5	μA	
Output High Voltage	V_{OH}	I_{OH}= -0.4mA	V_{DD}-0.4	-	-	V	DL1,DL2, DR1,DR2 V1~V4, S1~S80
Output Low Voltage	V_{OL}	I_{OL}= +0.4mA	-	-	0.4	V	
Operating Current	I_{DD}	F_{CL2}=400KHz	-	280	460	μA	VDD,V0
Leakage Current	I_V	V_{IN}=V_{DD}～V_{SS}	-10	-	10	μA	V1 ~ V4

3.2.2、AC Characteristics

Characteristic	Symbol	Test Condition	Min.	Max.	Unit	Applicable pin
Data Shift Frequency	F_{CL}	-	-	400	KHZ	CL2
Clock High Level Width	T_{WCKH}	-	800	-	ns	CL1,CL2
Clock Low Level Width	T_{WCKL}	-	800	-	ns	CL2
Clock Set-up Time	T_{SL}	CL2→CL1	500	-	ns	CL1,CL2
Clock Set-up Time	T_{LS}	CL1→CL2	500	-	ns	CL1,CL2
Clock Rise/Fall Time	T_R/T_F	-	-	200	ns	CL1,CL2
Data Set-up Time	T_{SU}	-	300	-	ns	DL1,DL2,DR1,DR2
Data Hold Time	T_{DH}	-	300	-	ns	DL1,DL2,DR1,DR2
Data Delay Time	T_D	CL = 15 PF	-	500	ns	DL1,DL2,DR1,DR2

4、TYPICAL APPLICATION CIRCUIT AND FUNCTION DESCRIPTION

4. 1、APPLICATION CIRCUIT: 2Line x 16 Chinese Word



4. 2、APPLICATION NOTE

4.2.1、Functional Description

- **Clock**

The CL1 is the clock to latch data on the falling edge. It latches the data input from the bi-directional shift register at the falling edge of CL1 and transfers its outputs to the LCD driver circuit. The CL2 is the clock to shift data on the falling edge. It shifts the serial data at the falling of CL2 and transfers the output of each bit of the register to the latch circuit.

- **Shift Registers And Data I/O**

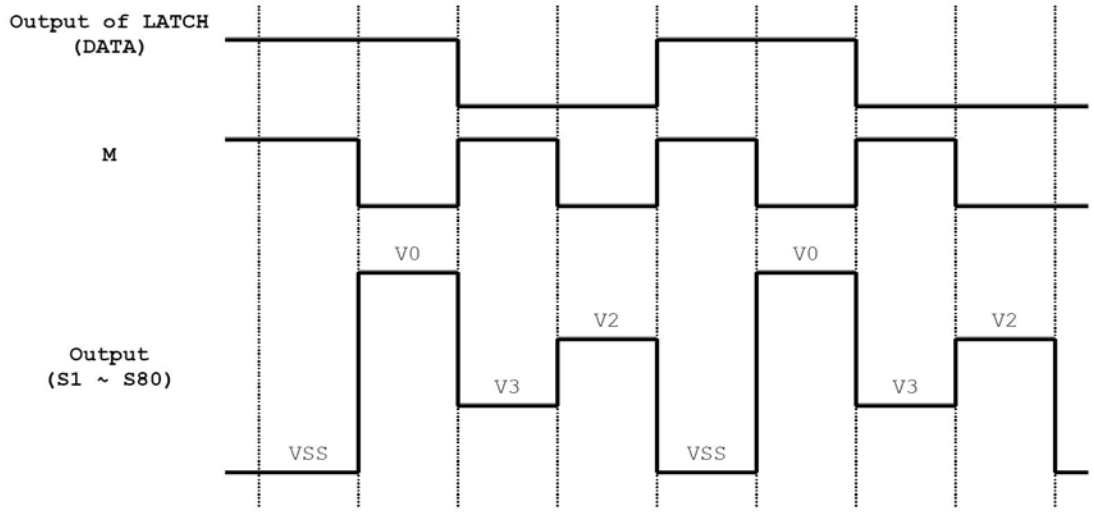
The AIP31021 supplies two sets of 48-bit shift register, which controls the shift direction by SHL1 & SHL2. The SHL1 controls the 1st 48-bit shift register, and SHL2 controls the 2nd 48-bit shift register. When SHL1 is connected to VDD, the 1st shift direction is from S48 to S1; when SHL1 is connected to VSS, the shift direction changes from S1 to S48. When SHL2 is connected to VDD, the 2nd shift direction is from S96 to S49; when SHL2 is connected to VSS, the shift direction changes from S49 to S96.

The DL1, DR1, DL2, DR2 are data input or output option function.

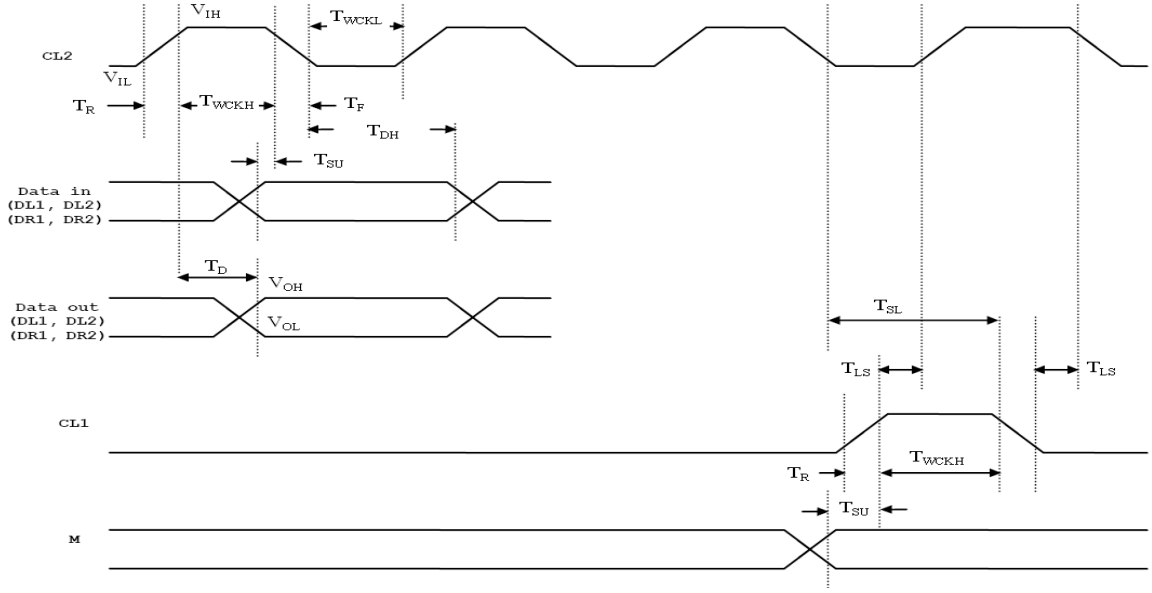
Shift Direction of Channel 1			
SHL1	Shift Direction	DL1	DR1
0	S1 →S48	IN	OUT
1	S48→ S1	OUT	IN

Shift Direction of Channel 2			
SHL2	Shift Direction	DL2	DR2
0	S49 →S96	IN	OUT
1	S96 →S49	OUT	IN

4.2.2、LCD Output Waveforms



4.2.3、Timing Characteristics



5、STATEMENTS AND NOTES：

5.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

5.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

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The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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