AIP31068L

16COM / 40SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

Product Specification

Specification Revision History ：

Version	Data	Description
2012-03-A1	2012-03	New-made

1、GENERAL DESCRIPTION

AIP31068L is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology.

Features

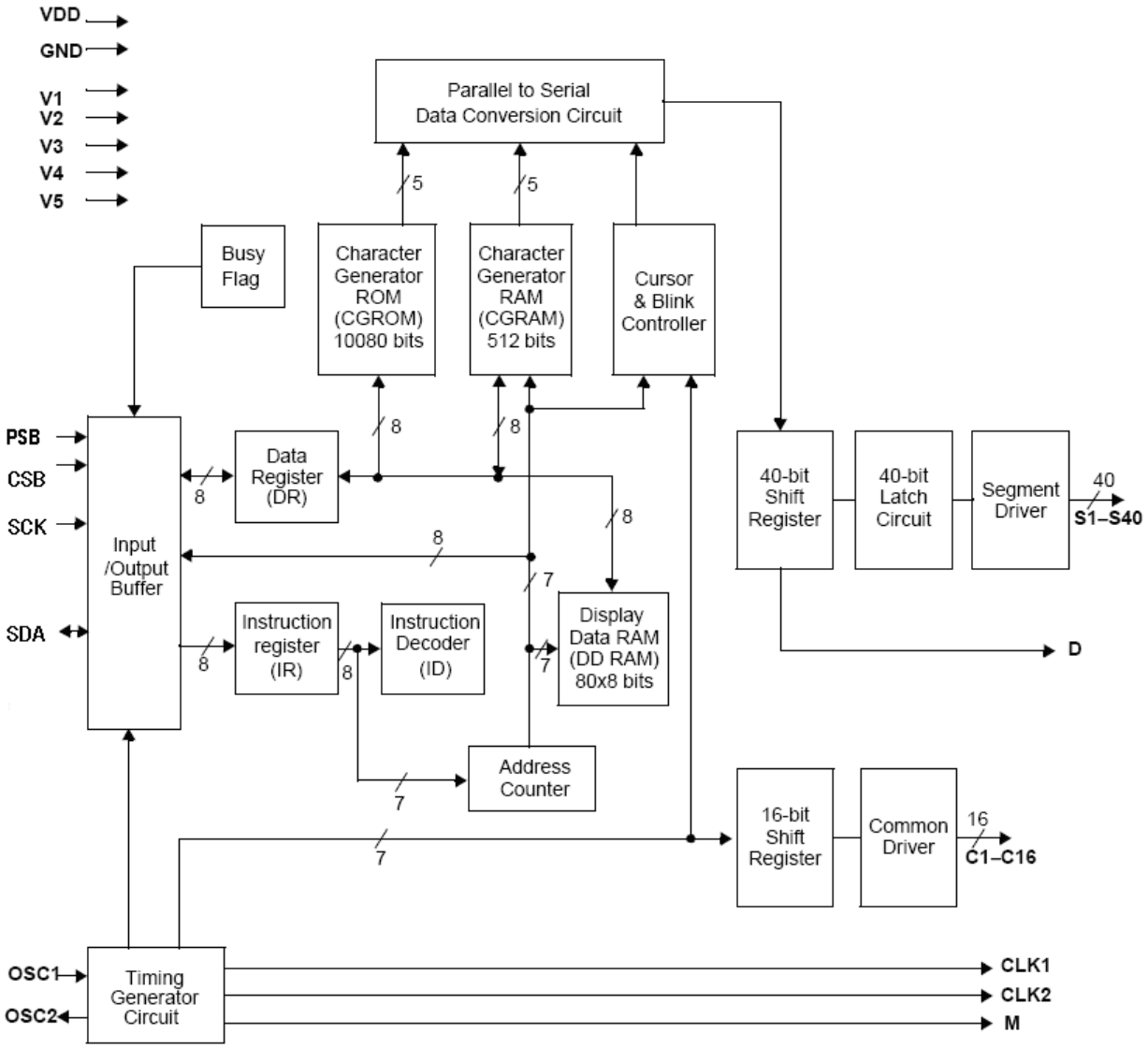
• Character type dot matrix LCD driver & controller.
• Internal driver: 16 common and 40 segment signal output.
• Two types interface: 3-lines serial interface and 2-lines serial interface (2-lines interface when power on)
• Display character pattern: 5×8 dots format (192 kinds) & 5×11 dots format (64 kinds).
• The Special character pattern is directly programmable by the Character Generator RAM.
• A customer character pattern is programmable by mask option.
• Programmable Driving Method by the same character font mask option: Display Waveform B-type
• It can drive a maximum at 80 characters by using the AIP31065 or AIP31063 externally.
• Various instruction functions.
• Built-in automatic power on reset.
•Internal Memory
-Character Generator ROM (CGROM): 10880 bits (192 characters×5×8 dots) & (64 characters×5×11 dots)
-Character Generator RAM (CGRAM): 64×8 bits (8 characters×5×8 dots)
-Display Data RAM (DDRAM): 80×8 bits (80 characters max.)
• Low power operation
-Power supply voltage range (VDD): 2.7 to 5.5 V
-LCD Drive voltage range (VDD-V5): 3.0 to 11.0 V
• CMOS process
• Programmable duty cycle: 1/8, 1/11, 1/16
• Character Patterns:

Type of Character Patterns
AIP31068L——Character patterns of English &Japanese

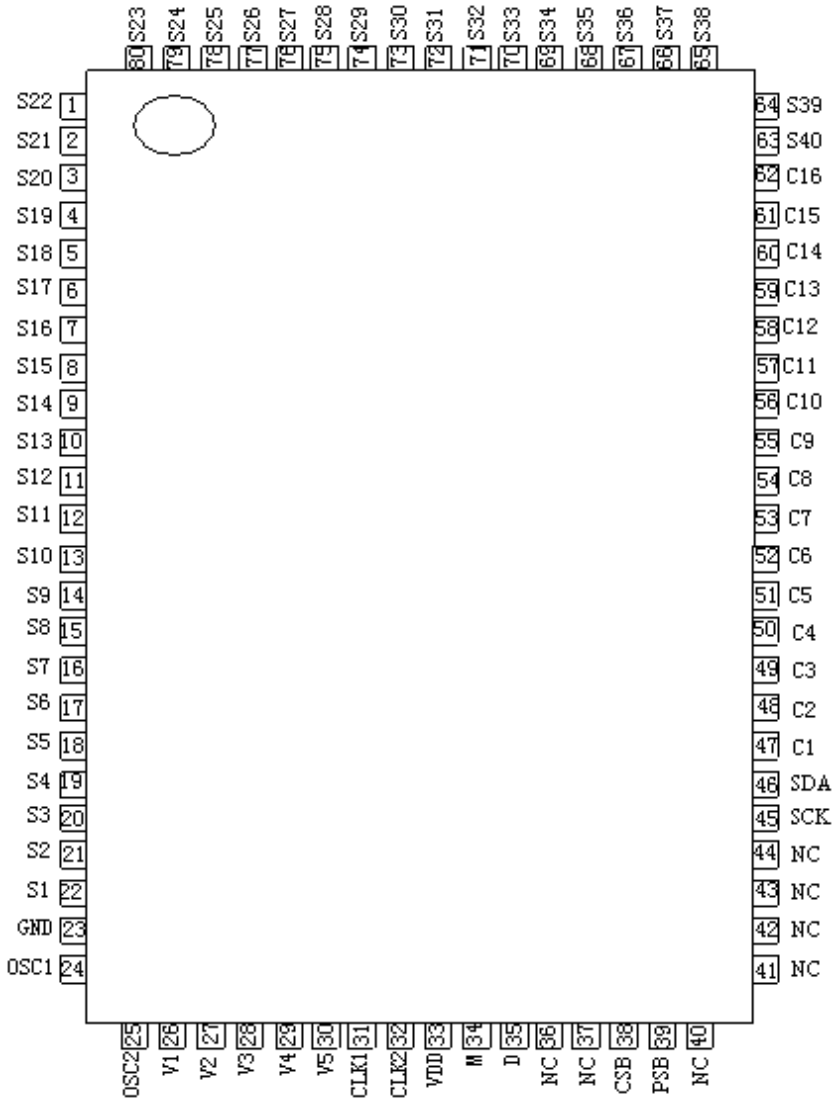
• Chip size: 2725×2455 (um×um).
•The IC substrate should be connected to VDD or float in the PCB layout artwork.
• 80 QFP or bare chip available (**PAD DIAGRAM is described in NO.6)**

2、BLOCK DIAGRAM AND PIN DESCRIPTION

2.1、BLOCK DIAGRAM



2.2、PIN CONFIGURATIONS



2.3、PIN DESCRIPTION

Pin No.	Pin Name		I/O	Description	Interface
33	VDD	Supply Voltage	P	Supply Voltage for logical circuit (+3V ±10%,+5V ±10%)	Power Supply
23	GND			Ground (0V)	
26～30	V1～V5			Bias voltage level for LCD driving	
1～22 63～80	S1～S40	Segment output	O	Segment signal output for LCD drive	LCD
47～62	C1～C16	Common output	O	Common signal output for LCD drive	LCD

24	OSC1	Oscillator	I	Oscillator. When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/oscillator (OSC1)
25	OSC2		O		
31	CLK1	Extension driver Latch clock	O	Extension driver latch clock	Extension driver
32	CLK2	Extension driver Shift clock		Extension driver shift clock	
34	M	Alternated signal for LCD driver output		Outputs the alternating signal to convert LCD driver waveform to AC.	
35	D	Display data interface		Outputs extension driver data (the 41st dot's data)	
38	CSB	Chip select	I	Chip select input pins. When use 3-line interface, CSB pin is used. When use 2-line interface, CSB pin is unused, it is floating.	MPU
39	PSB	Mode select		Mode select input pin with pull-high resistor. When PSB=”High”, 2-line interface is selected. When PSB=”Low”, 3-line interface is selected. It will be selected 2-line interface when power on.	
45	SCK	Serial clock input		Serial clock input	
46	SDA	Serial input data	I/O	Serial input data	
36、37 40～44	NC			Not Connect	

3、ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Ta =25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Power Supply Voltage(1)	V_{DD}	-0.3 ~ +7.0	V
Power Supply Voltage(2)	V_{LCD}	V_{DD}-12.0 ~ V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_{OPR}	-30 ~ +85	℃
Storage Temperature	T_{STG}	-55 ~ +125	℃

Note: Voltage greater than above may damage the circuit. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

3.2、ELECTRICAL CHARACTERISTICS

3.2.1、DC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-	4.5	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=5.0 V, fosc = 250 kHz)	-	0.55	0.8	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	2.5	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (2) (OSC1)	V_{IH2}	-	V_{DD}-1.0	-	V_{DD}	V
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH}= -0.205 mA	2.4	-	-	V
	V_{OL1}	I_{OL}= 1.2 mA	-	-	0.4	
Output Voltage (2) (except DB0 to	V_{OH2}	I_O= -40 mA	0.9V_{DD}	-	-	V
	V_{OL2}	I_O= 40 mA	-	-	0.1V_{DD}	
Voltage Drop	Vd_{COM}	I_O=± 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IKG}	V_{IN}= 0 V to V_{DD}	-1	-	1	uA
Input Low Current	I_{IL}	V_{IN}= 0 V, V_{DD}= 5 V (PULL UP)	-50	-125	-250	
Internal Clock (external Rf)	f_{OSC1}	Rf =91 kΩ± 2% (V_{DD}= 5 V)	190	270	350	kHz
External Clock	f_{OSC}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R, t_F		-	-	0.2	ms
COM ON resistance	R_{COM}	I_O = ±50uA, V_{LCD} = 4.0V COM1 - COM16			20	KΩ
SEG ON resistance	R_{SEG}	I_O = ±50uA, V_{LCD} = 4.0V SEG1 - SEG40			30	
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5(1/5, 1/4 Bias)	3.0	-	11.0	V

3.2.2、DC Characteristic (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-	2.7	-	4.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=3.0 V, fosc = 250 kHz)	-	0.2	0.4	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.55	
Input Voltage (2) (OSC1)	V_{IH2}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL2}	-	-	-	0.2V_{DD}	
Output Voltage (1)	V_{OH1}	I_{OH}= -0.1 mA	0.75V_{DD}	-	-	V

(DB0 to DB7)	V_{OL1}	I_{OL}= 0.1 mA	-	-	$0.2V_{DD}$	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O= -40 mA	$0.8V_{DD}$	-	-	V
	V_{OL2}	I_O= 40 mA	-	-	$0.2V_{DD}$	
Input Leakage Current	I_{IKG}	V_{IN}= 0 V to V_{DD}	-1	-	1	mA
Input Low Current	I_{IL}	V_{IN}= 0 V, V_{DD}= 3 V (PULL UP)	-10	-50	-120	
Internal Clock (external Rf)	f_{OSC1}	Rf = 75 kΩ± 2% (V_{DD}= 3 V)	190	270	350	kHz
External Clock	f_{OSC2}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R ,t_F		-	-	0.2	ms
COM ON resistance	R_{COM}	I_O = ±50uA, V_{LCD} = 4.0V COM1 - COM16			20	KΩ
SEG ON resistance	R_{SEG}	I_O = ±50uA, V_{LCD} = 4.0V SEG1 - SEG40			30	
LCD Driving Voltage	V_{LCD}	V_{DD}-V5 (1/5, 1/4 Bias)	3.0	-	9.0	V

LCD Driving Voltage:

Power	Duty	1/8, 1/11 Duty	1/16 Duty
	Bias	1/4 Bias	1/5 Bias
V_{DD}		V_{DD}	V_{DD}
V1		V_{DD}-V_{LCD}/4	V_{DD}-V_{LCD}/5
V2		V_{DD}-V_{LCD}/2	V_{DD}-2V_{LCD}/5
V3		V_{DD}-V_{LCD}/2	V_{DD}-3V_{LCD}/5
V4		V_{DD}-3V_{LCD}/4	V_{DD}-4V_{LCD}/5
V5		V_{DD}-V_{LCD}	V_{DD}-V_{LCD}

3.2.3、AC Characteristics 1 (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Cycle Time	t_{SCYC}	Write Mode (Refer to Fig-1)	100	-	-	ns
SCL Pulse Width (High)	t_{SHW}		20	-	-	
SCL Pulse Width (Low)	t_{SLW}		160	-	-	
SCL Rise / Fall Time	t_r,t_f		-	-	20	
Data Setup Time	t_{SDS}		10	-	-	
Data Hold Time	t_{SDH}		10	-	-	
SCL Cycle Time	t_{SCYC}		20	-	-	
SCL Pulse Width (High)	t_{SHW}		350	-	-	

SCL Frequency	f_{SCLK}	Read Mode (Refer to Fig-2)	-	-	400	ns
SCL Pulse Width (High)	t_{SHW}		0.6	-	-	
SCL Pulse Width (Low)	t_{SLW}		1.3	-	-	
Data Setup Time	$t_{SU:DAT}$		100	-	-	
Data Hold Time	$t_{HD:DAT}$		0	-	0.9	
SCL/SDA Rise / Fall Time	t_r,t_f		20	-	300	
START Setup Time	$t_{SU:STA}$		0.6	-	-	
START Hold Time	$t_{HD:STA}$		0.6	-	-	
STOPSetup Time	$t_{SU:STO}$		0.6	-	-	
STOP-START Time	t_{BUF}		1.3	-	-	

3.2.4、AC Characteristics 2 (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Cycle Time	t_{SCYC}	Write Mode (Refer to Fig-1)	200	-	-	ns
SCL Pulse Width (High)	t_{SHW}		20	-	-	
SCL Pulse Width (Low)	t_{SLW}		160	-	-	
SCL Rise / Fall Time	t_r,t_f		-	-	20	
Data Setup Time	t_{SDS}		10	-	-	
Data Hold Time	t_{SDH}		10	-	-	
SCL Cycle Time	t_{SCYC}		20	-	-	
SCL Pulse Width (High)	t_{SHW}		200	-	-	
SCL Frequency	f_{SCLK}	Read Mode (Refer to Fig-2)	-	-	400	KHZ
SCL Pulse Width (High)	t_{SHW}		0.6	-	-	us
SCL Pulse Width (Low)	t_{SLW}		1.3	-	-	
Data Setup Time	$t_{SU:DAT}$		180	-	-	ns
Data Hold Time	$t_{HD:DAT}$		0	-	0.9	us
SCL/SDA Rise / Fall Time	t_r,t_f		20	-	300	ns
START Setup Time	$t_{SU:STA}$		0.6	-	-	us
START Hold Time	$t_{HD:STA}$		0.6	-	-	us
STOPSetup Time	$t_{SU:STO}$		0.6	-	-	us
STOP-START Time	t_{BUF}		1.3	-	-	us
Clock Pulse Width (High, Low)	t_c	Interface Mode with Extension Driver (Refer to Fig-3)	800	-	-	ns
Clock Rise / Fall Time	t_R, t_F		-	-	25	
Clock Setup Time	t_{su1}		500	-	-	
Data Setup Time	t_{su2}		300	-	-	

Data Hold Time	t_{DH}		300	-	-	
M Delay Time	t_{DM}		-1000	-	1000	

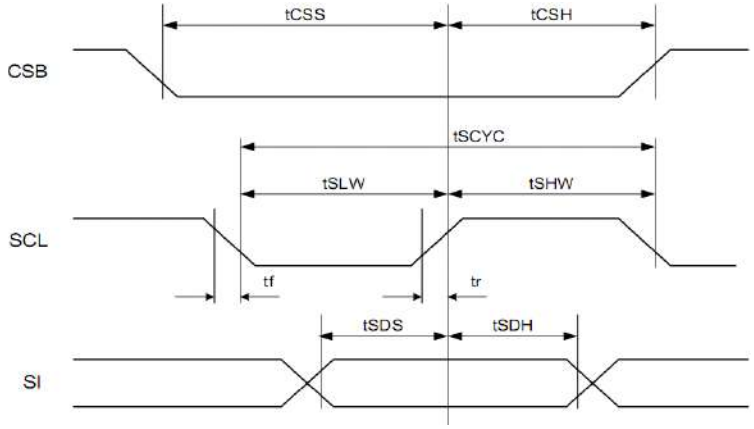


Figure 1 . Timing Diagram of 3-lines interface

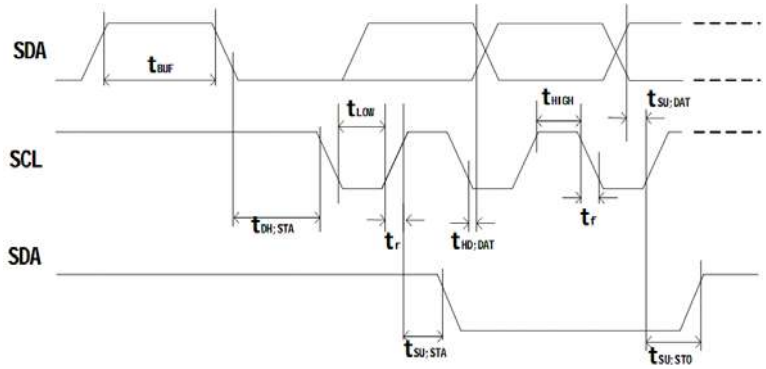


Figure 2 . Timing Diagram of 2-lines interface

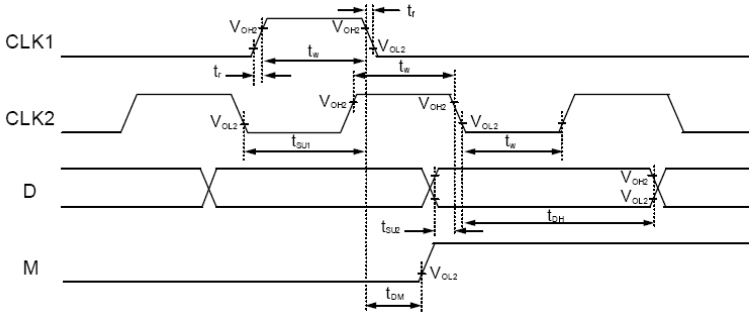


Figure 3 . Interface Mode with Extension Driver

4、FUNCTION DESCRIPTION

4.1、System Interface

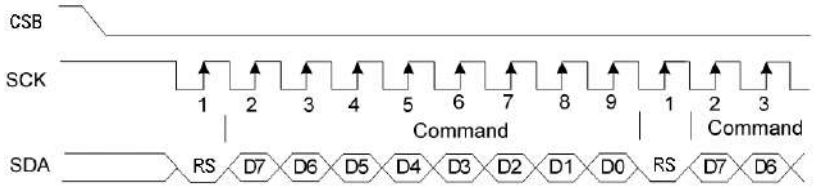
AIP31068L has two types of interface with a MPU, which are 3-lines serial interface and 2-lines serial interface. The interface is determined by PSB pin.

PSB pin	Interface type	Used pins
L	3-lines serial interface	CSB、SCK、SDA
H	2-lines serial interface	SCK、SDA

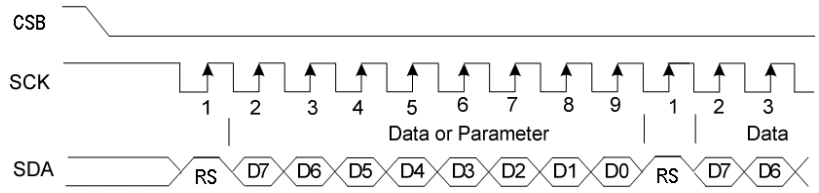
4.1.1、3-lines serial interface

The 3-lines serial interface (9-bit) uses three pins(CSB、SDA、SCK) to enter commands and data. Timing sequence is shown below.

Transfer command mode:



Transfer data mode:



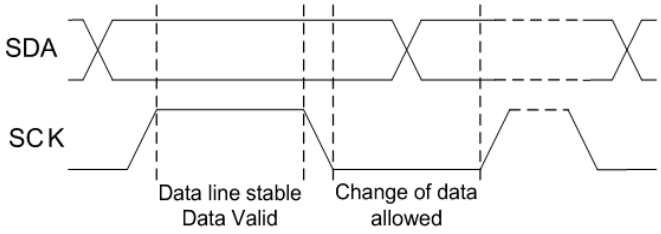
Note: 1、the RS bit defines whether the following data bytes are interpreted as COMMAND or as DATA: When RS is “low”, the following data is COMMAND. When RS is “high”, the following data is DATA.

2、The serial interface don’t read the Flag(BF), thus it must be waiting enough execution time between the two instructions.(Refer to Table 4).

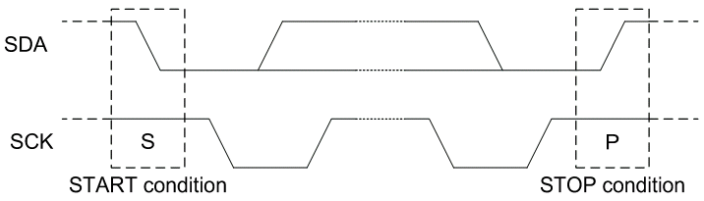
4.1.2、2-lines serial interface

The 2-lines are a Serial Data line (SDA) and a Serial Clock line (SCK). Both lines must be connected with a pull-up resistor which drives SDA and SCK to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in below Figure.

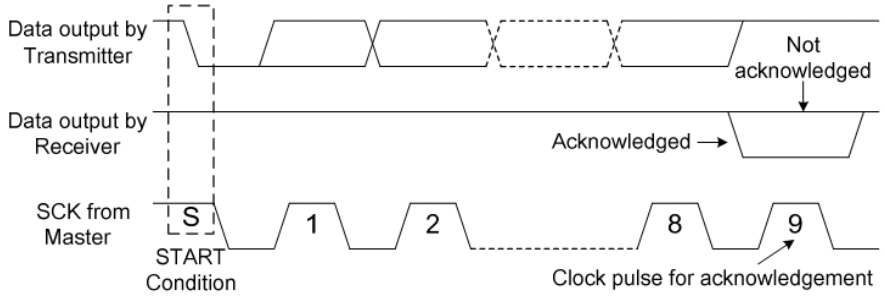


Both SDA and SCK lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCK is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCK is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in below Figure.

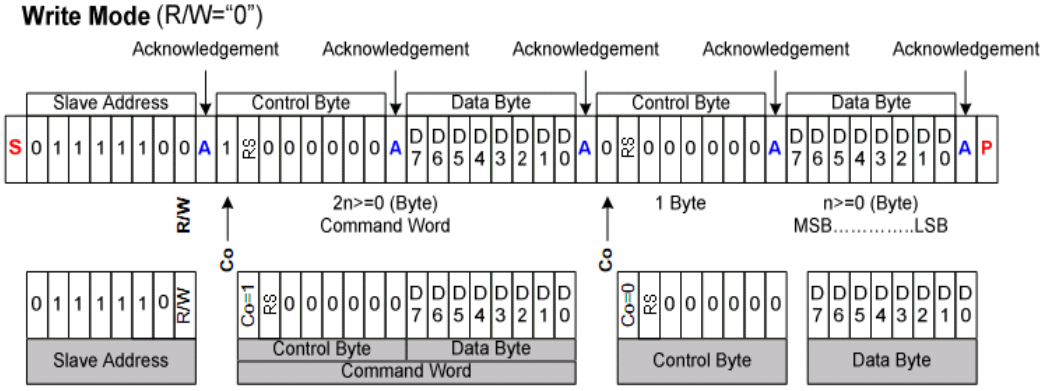


Acknowledge condition:

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a LOW signal put on SDA by the transmitter during the time when the MPU generates an extra acknowledge-related clock pulse. The AIP31086L receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A MPU receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A MPU receiver must signal an end-of-data to the AIP31086L transmitter by not generating a acknowledge-bit on the last byte that has been clocked out of the AIP31086L. In this event the transmitter must leave the data line HIGH to enable the MPU to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in below Figure.



2-lines serial interface protocol:



Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

Note ： 1、the RS bit defines whether the following data bytes are interpreted as COMMAND or as DATA: When RS is "low", the following data is COMMAND. When RS is "high", the following data is DATA.

2、The serial interface don't read the Flag(BF), thus it must be waiting enough execution time between the two instructions.(Refer to Table 4).

During write operation, two 8-bit registers are used. One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into

DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. Thus, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction codes transferred from MPU. MPU cannot use it to read instruction data. To select a register, you can use RS input pin.

Various kinds of Operations according to RS bits：

RS	Operation
L	Instruction Write operation (MPU writes Instruction code into IR)
H	Data Write operation (MPU writes data into DR)

- **Busy Flag (BF)**

BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = “Low” and R/W = “High” (Read Instruction Operation). Before executing the next instruction, be sure that BF is not “High”.

- **Address Counter (AC)**

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = “Low” and R/W = “High”, AC can be read through ports DB0 to DB6.

- **Display Data RAM (DDRAM)**

DDRAM stores display data of maximum 80 8 bits (80 characters). DDRAM address is set in the address counter(AC) as a hexadecimal number (Refer to Fig-4.)

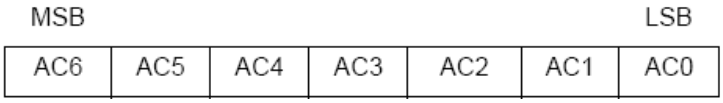


Figure 4 . DDRAM Address

1) 1-line display

In case of 1-line display, the address range of DDRAM is00H～4FH.

An extension driver will be used. Fig-5 shows the example with 40 segment extension driver added.

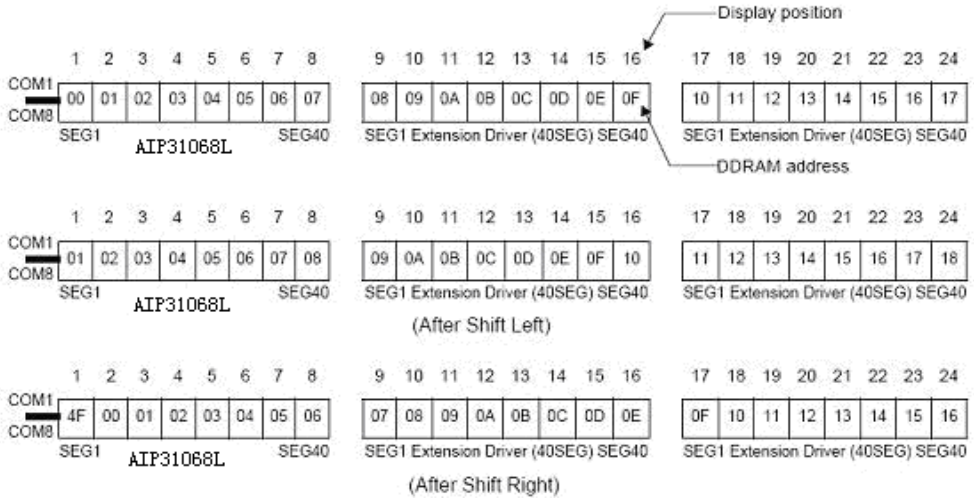


Figure 5 . 1-line × 24 char. display with 40 SEG. extension driver

2) 2-line display

In case of 2-line display, the address range of DDRAM is 00H～27H and 40H～67H .

An extension driver will be used. Fig-6 shows the example with 40 segment extension driver added.

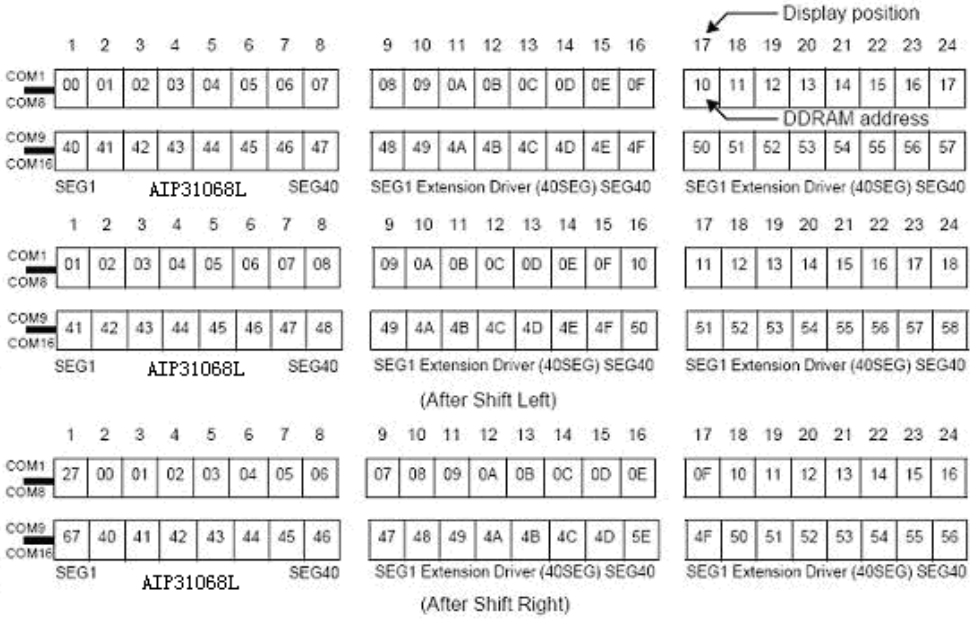


Figure 6 . 2-line × 24 char. display with 40 SEG. extension driver

- **CGROM(Character Generator ROM)**

  CGROM has a 5*8 dots 192 characters pattern and a 5*11 dots 64 characters pattern.

- **CGRAM(Character Generator RAM)**

  CGRAM has up to 5*8 dots 8 characters. By writing font data to CGRAM, user defined characters can be used (Refer to Table 1)

- **Timing Generation Circuit**

  Timing generation circuit generates clock signals for the internal operations.

- **LCD Driver Circuit**

  LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to a 40-bit segment latch serially, and then is stored to 40-bit shift latch. When each common is selected by 16-bit common register, segment data is also output through segment driver from a 40-bit segment latch. In case of 1-line display mode, COM1 to COM8 have 1/8 duty or COM1 to COM11 have 1/11 duty, and in 2-line mode, COM1 to COM16 have a 1/16 duty ratio.

- **Cursor/Blink Control Circuit**

  It controls the cursor/blink ON/OFF at cursor position.

Table 1. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	0	1	1	1	0	pattern1
											0	0	1				0	0	1	0	0	
											0	1	0				0	0	1	0	0	
											0	1	1				0	0	1	0	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	1	1	1	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	×	0	0	1	0	0	1	0	0	0	×	×	×	0	1	1	1	0	pattern2
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	0	
											0	1	1				1	0	0	0	0	
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											1	1	1				0	0	0	0	0	
					* * * *						* * * *						* * * *					
0	0	0	0	×	1	1	1	1	1	1	0	0	0	×	×	×	1	1	1	1	1	pattern8
											0	0	1				1	0	0	0	0	
											0	1	0				1	0	0	0	0	
											0	1	1				1	1	1	1	0	
											1	0	0				1	0	0	0	0	
											1	0	1				1	0	0	0	1	
											1	1	0				1	1	1	1	0	
											1	1	1				0	0	0	0	0	

4.2、INSTRUCTION DESCRIPTION

To overcome the speed difference between the internal clock of AIP31068L and the MPU clock, AIP31068L performs internal operations by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 3).

Instructions can be divided largely into four groups:

1) AIP31068L function set instructions (set display methods, set data length, etc.)

2) address set instructions to internal RAM

3) data transfer instructions with internal RAM

4) others

The address of the internal RAM is automatically increased or decreased by 1.

Note: During internal operation, Busy Flag (DB7) is read “High”.

Busy Flag check must be preceded by the next instruction.

When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to “Low”.

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D = “High”).

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

* “-”: dont care

Return Home is cursor return home instruction. Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: Shift of entire display

When DDRAM read (CGRAM read/write) operation or SH = “Low”, shifting of entire display is not performed. If SH = “High” and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = “High”: shift left, I/D = “Low”: shift right).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D = “High”, entire display is turned on.

When D = “Low”, display is turned off, but display data remains in DDRAM.

C: Cursor ON/OFF control bit

When C = “High”, cursor is turned on.

When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit

When B = “High”, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.

When B = “Low”, blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data.(Refer to Table 2) During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

Table 2. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit

When N = “Low”, 1-line display mode is set.

When N = “High”, 2-line display mode is set.

F: Display font type control bit

When F = “Low”, 5 8 dots format display mode is set.

When F = “High”, 5 11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = Low), DDRAM address is from “00H” to “4FH”. In 2-line display mode (N = High), DDRAM address in the 1st line is from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether AIP31068L is in internal operation or not.

If the resultant BF is “High”, internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not Yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

Table 3. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc= 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.53 ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5×11dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

* "-": dont care

Note: When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2Fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

4.3、INITIALIZING

When the power is turned on, AIP31068L is initialized automatically by power on reset circuit.

During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) to the end of initialization.

(1) Display Clear instruction: Write "20H" to all DDRAM

(2) Set Functions instruction: DL = "High": 8-bit bus mode

N = “Low”: 1-line display mode

F = “Low”: 5 X 8 font type

(3) Control Display ON/OFF instruction: D = “Low”: Display OFF

C = “Low”: Cursor OFF

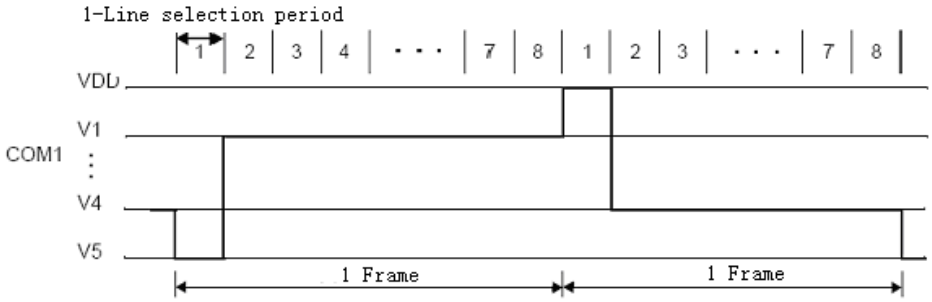
B = “Low”: Blink OFF

(4) Set Entry Mode instruction: I/D = “High”: Increment by 1

SH = “Low”: No entire display shift

4.4、FRAME FREQUENCY

1) 1/8 duty cycle

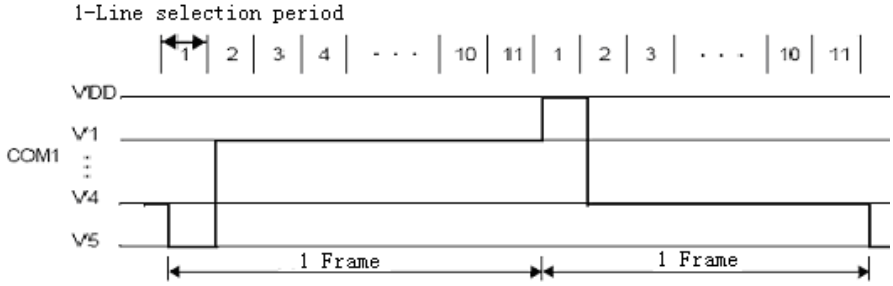


1-Line selection period = 400 clocks

1 Frame =400×8×3.7μs = 11850μs = 11.9 ms (1 clock=3.7μs, fosc=270 kHz)

Frame frequency = 1 / 11.9 ms = 84.4 Hz

2) 1/11 duty cycle

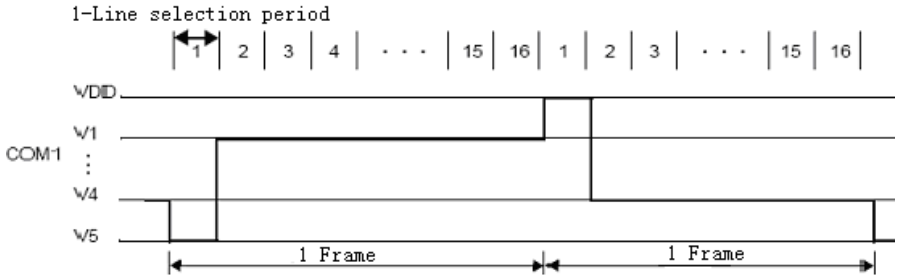


1-Line selection period = 400 clocks

1 Frame = 400×11×3.7μs = 16300μs = 16.3 ms (1 clock=3.7μs, fosc=270 kHz)

Frame frequency = 1 / 16.3 ms = 61.4 Hz

3) 1/16 duty cycle



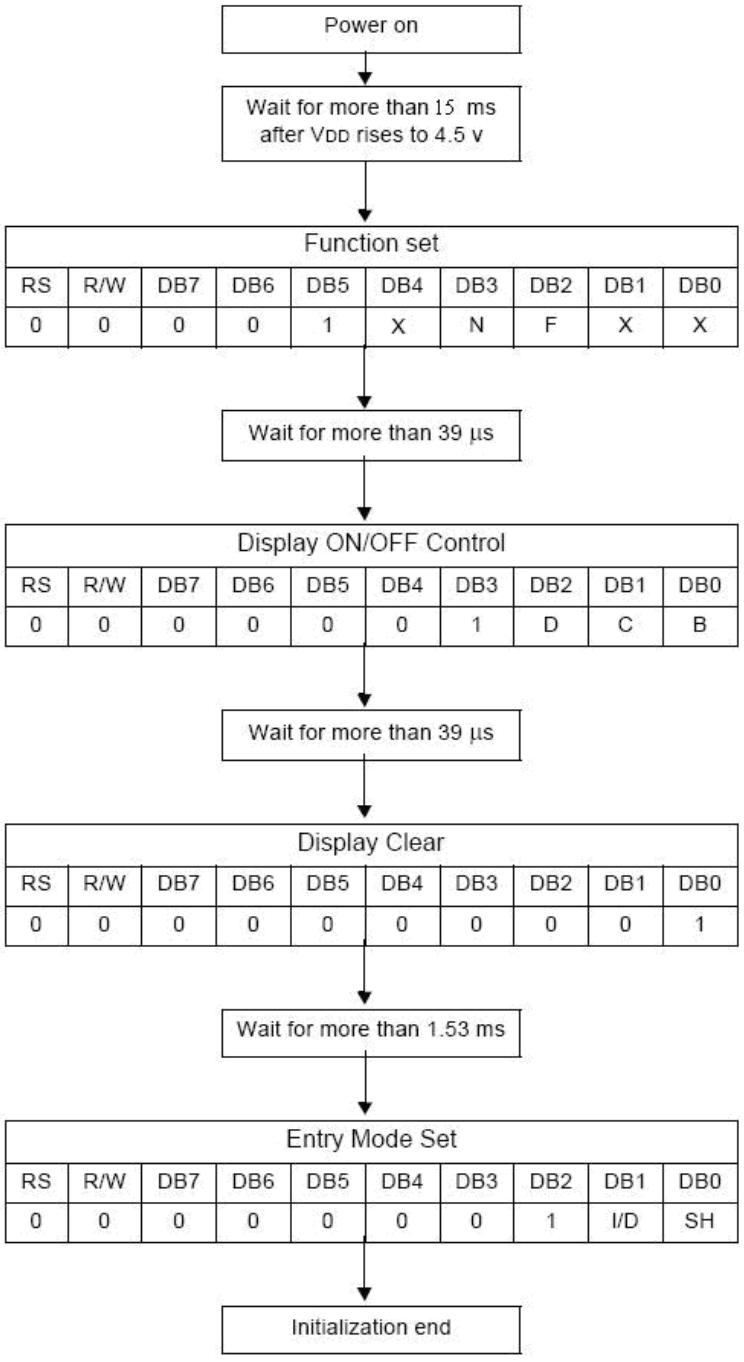
1-Line selection period = 200 clocks

1 Frame = 200×16×3.7μs = 11850μs = 11.9 ms (1 clock=3.7μs, fosc=270 kHz)

Frame frequency = 1 / 11.9 ms = 84.3 Hz

4.5、INITIALIZING BY INSTRUCTION

1) Serial interface mode (Condition: fosc = 270KHZ)

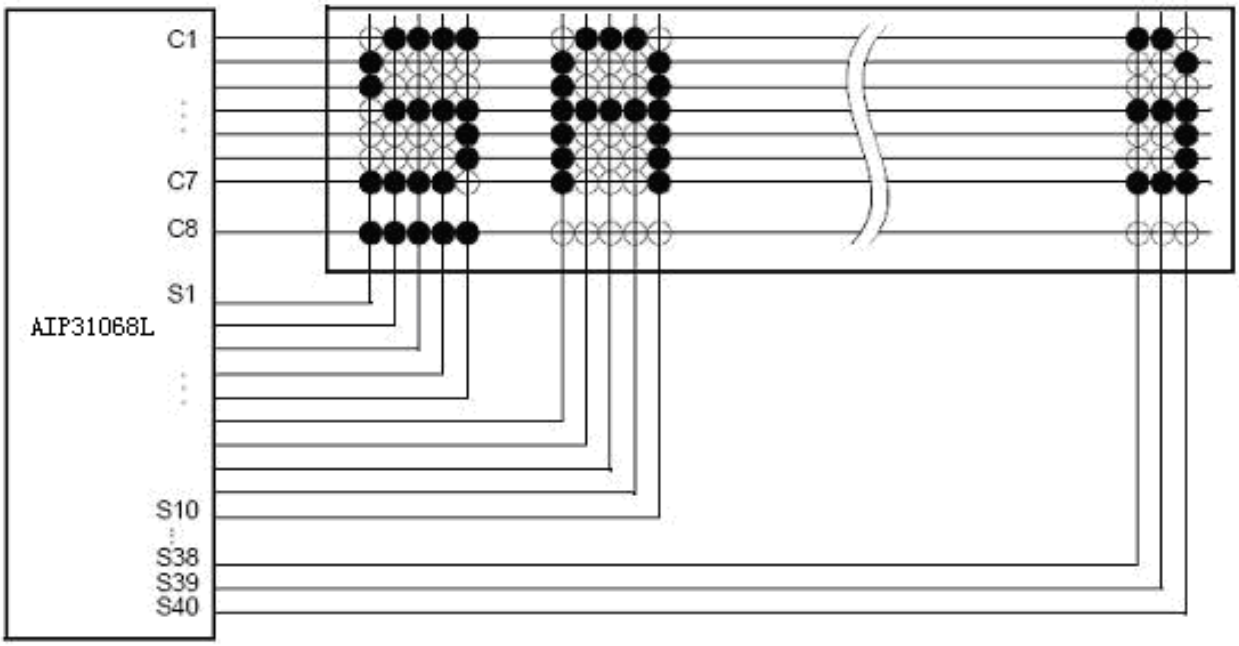


N	0	1-line mode
	1	2-line mode
F	0	display off
	1	display on
D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on

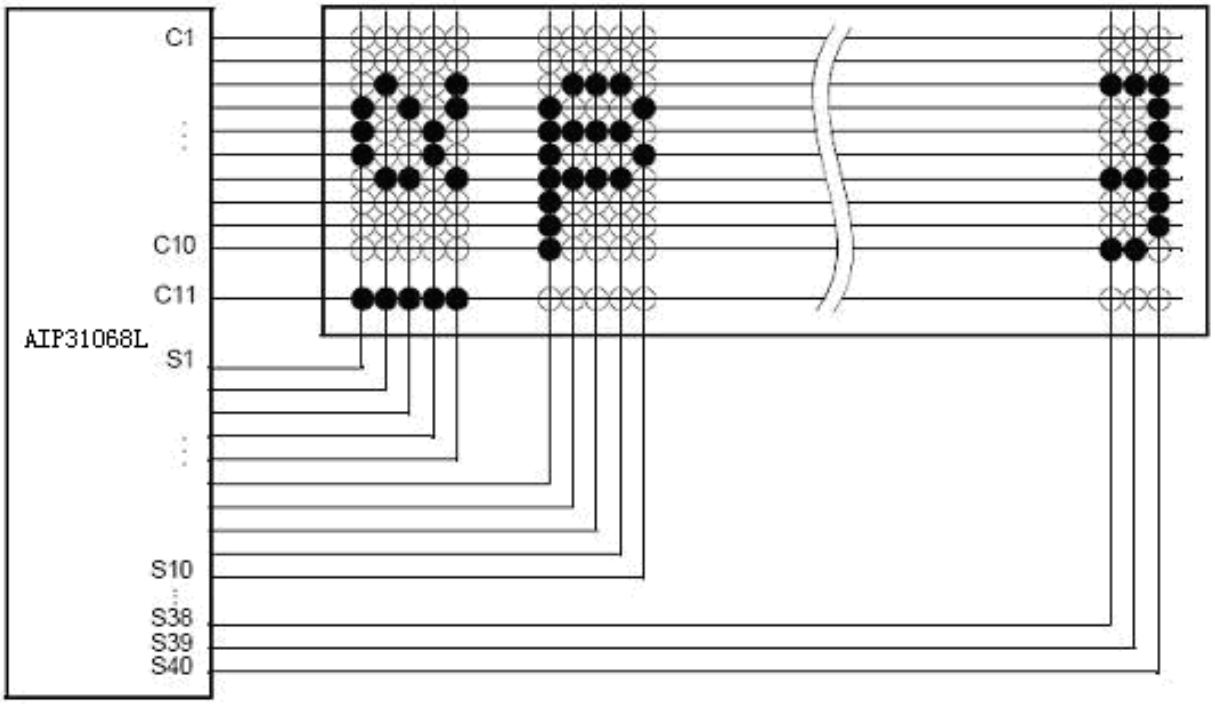
5、TYPICAL APPLICATION

5.1、typical application

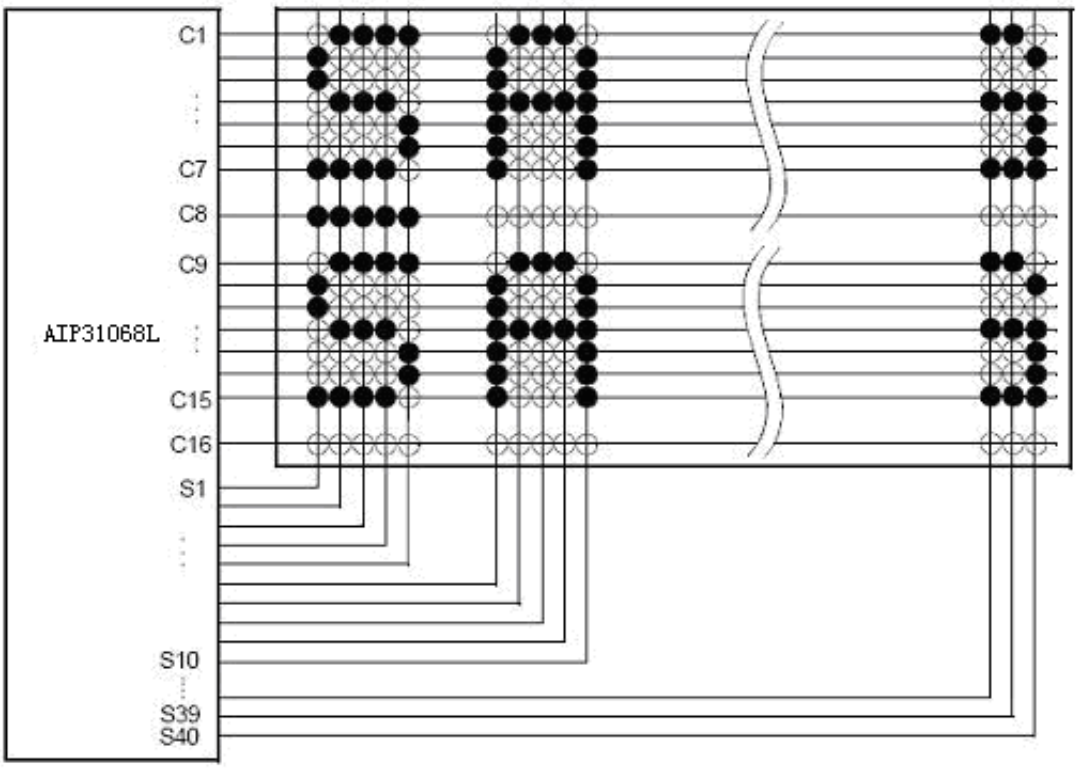
1) LCD Panel: 8 characters ×1-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)



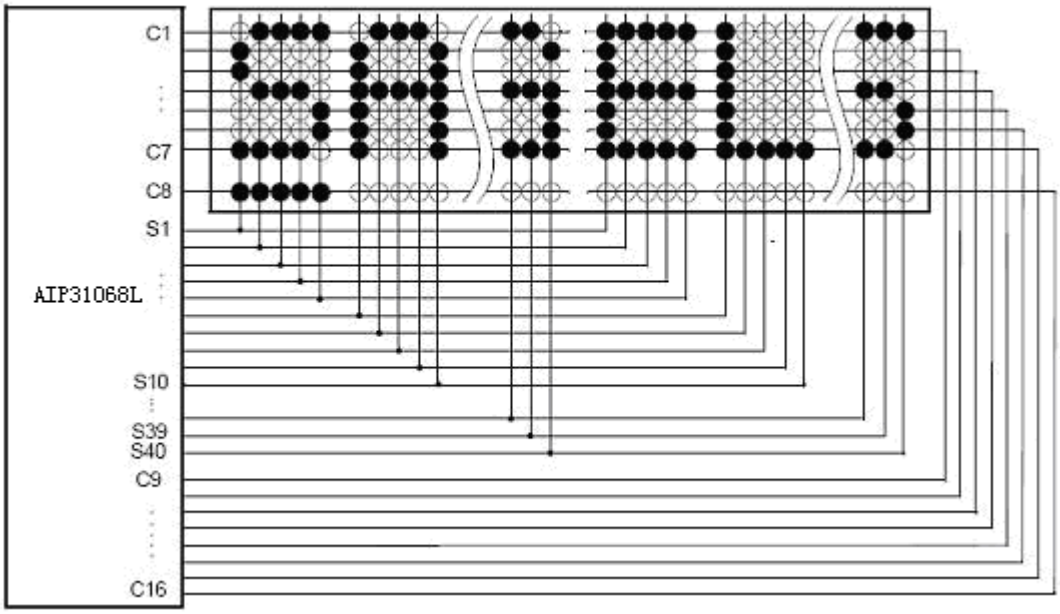
2) LCD Panel: 8 characters×1-line format (5×10 dots + 1cursor line, 1/4 bias, 1/11 duty)



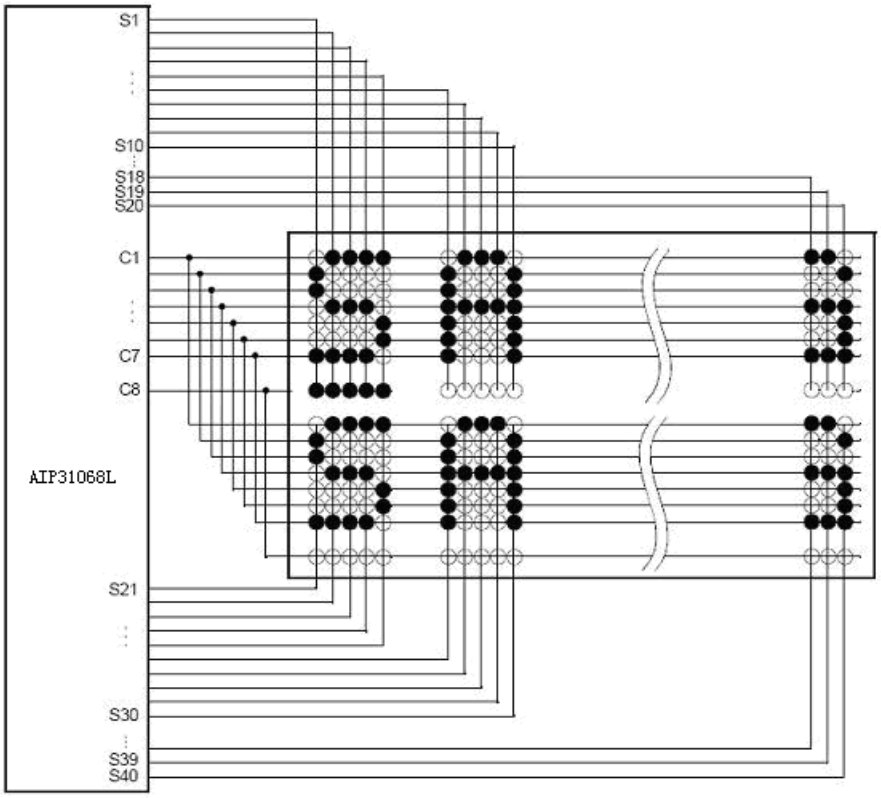
3) LCD Panel: 8 characters×2 -line format (5×7 dots + line, 1/5 bias, 1/16 duty)



4) LCD Panel: 16 characters×1-line format (5×7 dots + 1cursor line, 1/5 bias, 1/16 duty)

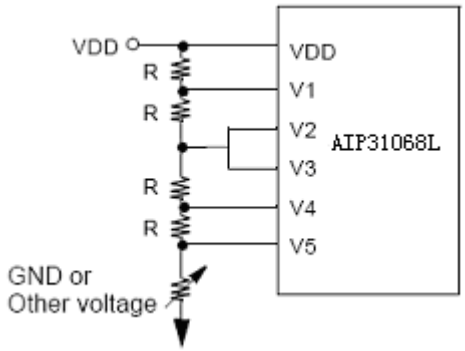


5) LCD Panel: 4 characters ×2-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)

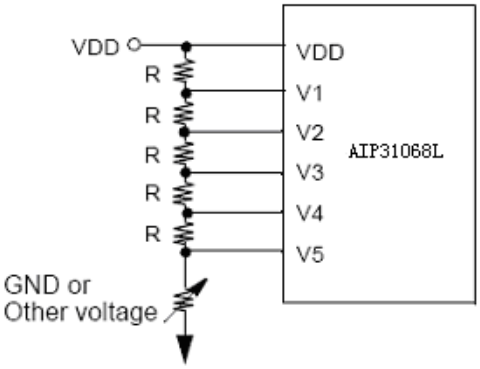


5.2、BIAS VOLTAGE DIVIDE CIRCUIT

- 1/4 bias, 1/8 or 1/11 duty

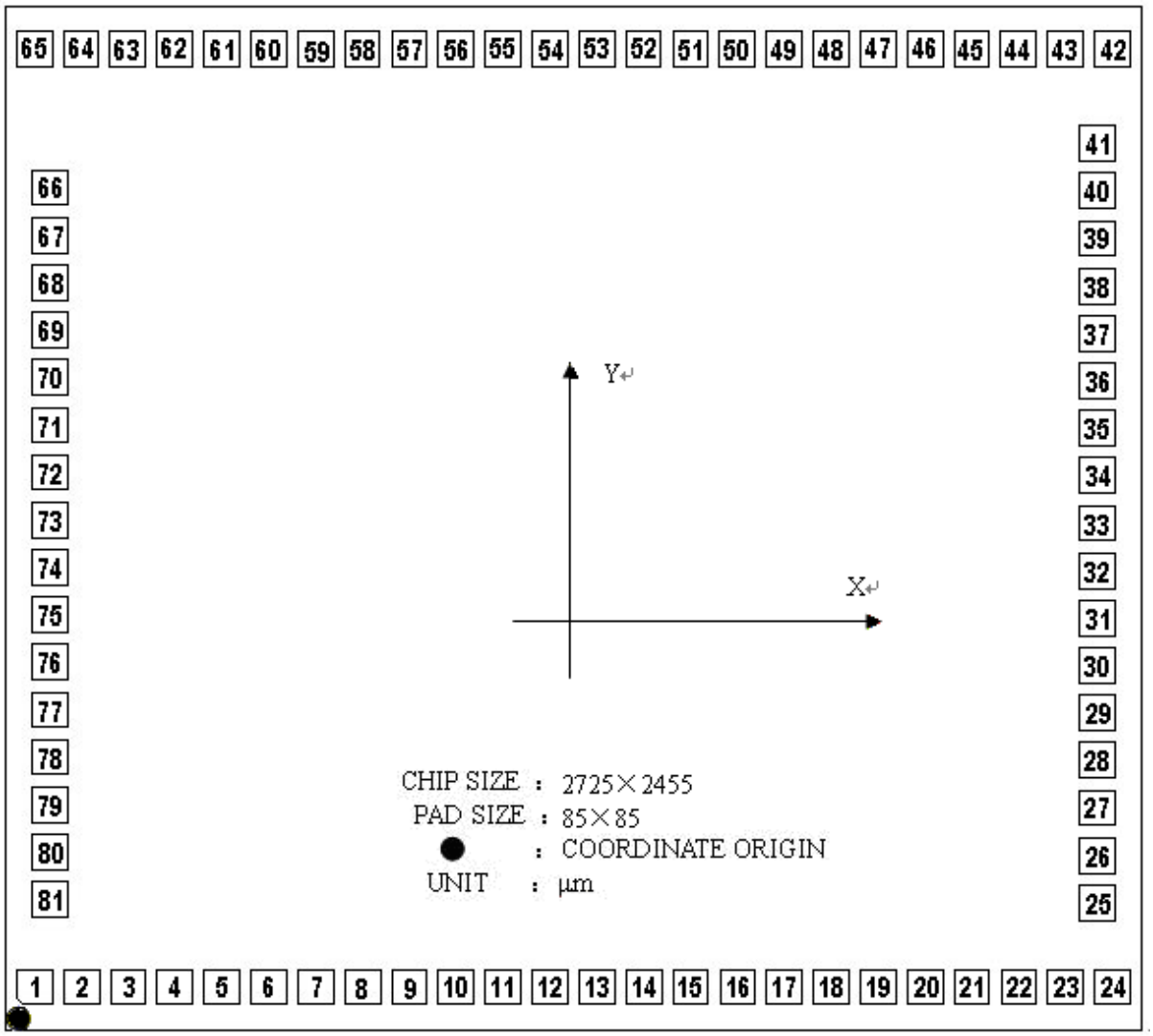


- 1/5 bias, 1/16 duty



6、PAD DIAGRAM AND PAD LOCATION

6.1、PAD DIAGRAM



6.2、PAD Location （UNIT: μm）

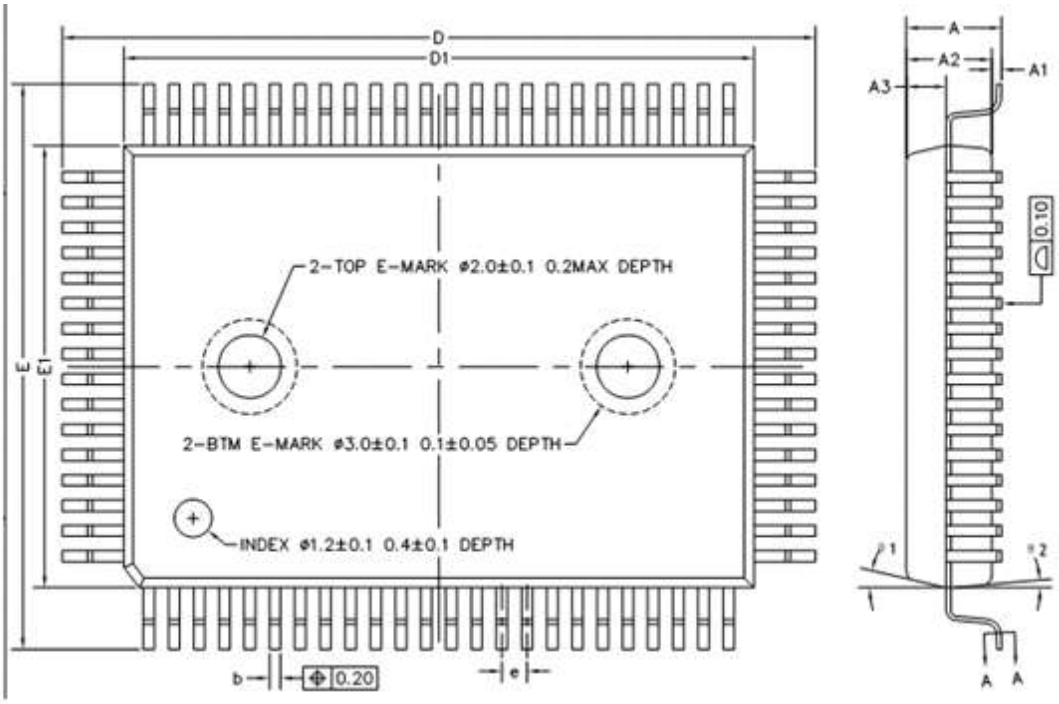
NO.	NAME	X	Y	NO.	NAME	X	Y
1	S22	68.75	100.6	42	NC	2655.75	2354.4
2	S21	181.25	100.6	43	NC	2543.25	2354.4
3	S20	293.75	100.6	44	NC	2430.75	2354.4
4	S19	406.25	100.6	45	NC	2318.25	2354.4
5	S18	518.75	100.6	46	SCK	2205.75	2354.4
6	S17	631.25	100.6	47	SDA	2093.25	2354.4
7	S16	743.75	100.6	48	C1	1980.75	2354.4
8	S15	856.25	100.6	49	C2	1868.25	2354.4
9	S14	968.75	100.6	50	C3	1755.75	2354.4
10	S13	1081.25	100.6	51	C4	1643.25	2354.4

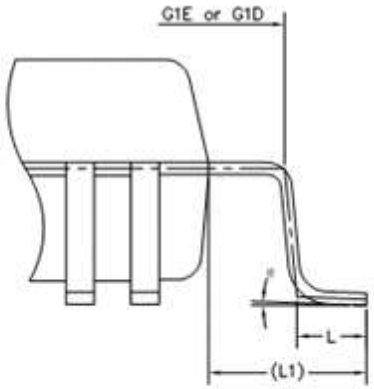
11	S12	1193.75	100.6	52	C5	1530.75	2354.4
12	S11	1306.25	100.6	53	C6	1418.25	2354.4
13	S10	1418.75	100.6	54	C7	1305.75	2354.4
14	S9	1531.25	100.6	55	C8	1193.25	2354.4
15	S8	1643.75	100.6	56	C9	1080.75	2354.4
16	S7	1756.25	100.6	57	C10	968.25	2354.4
17	S6	1868.75	100.6	58	C11	855.75	2354.4
18	S5	1981.25	100.6	59	C12	743.25	2354.4
19	S4	2093.75	100.6	60	C13	630.75	2354.4
20	S3	2206.25	100.6	61	C14	518.25	2354.4
21	S2	2318.75	100.6	62	C15	405.75	2354.4
22	S1	2431.25	100.6	63	C16	293.25	2354.4
23	GND	2543.75	100.6	64	S40	180.75	2354.4
24	OSC1	2656.25	100.6	65	S39	68.25	2354.4
25	OSC2	2620.5	302.8	66	S38	104.6	2020.6
26	V1	2620.5	416.8	67	S37	104.6	1906.6
27	V2	2620.5	530.8	68	S36	104.6	1792.6
28	V3	2620.5	644.8	69	S35	104.6	1678.6
29	V4	2620.5	758.8	70	S34	104.6	1564.6
30	V5	2620.5	872.8	71	S33	104.6	1450.6
31	CLK1	2620.5	986.8	72	S32	104.6	1336.6
32	CLK2	2620.5	1100.8	73	S31	104.6	1222.6
33	VDD	2620.5	1214.8	74	S30	104.6	1108.6
34	M	2620.5	1328.8	75	S29	104.6	994.6
35	D	2620.5	1442.8	76	S28	104.6	880.6
36	NC	2620.5	1556.8	77	S27	104.6	766.6
37	NC	2620.5	1670.8	78	S26	104.6	652.6
38	CSB	2620.5	1784.8	79	S25	104.6	538.6
39	PSB	2620.5	1898.8	80	S24	104.6	424.6
40	NC	2620.5	2012.8	81	S23	104.6	310.6
41	NC	2620.5	2126.8				

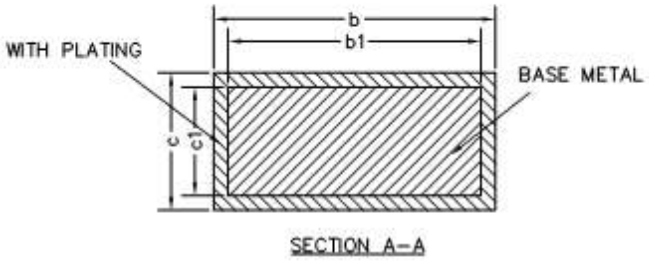
Note: NC is unused.

7、PACKAGE INFORMATION

7.1、QFP80







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.32	–	0.42
b1	0.32	0.35	0.38
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.70	0.80	0.90
G1D		22.00REF	
G1E		16.00REF	
L	0.60	0.80	1.00
L1		1.95REF	
θ	0°	2°	8°
θ1	11°	13°	15°
θ2	3°	5°	7°

AIP31068L CHARACTER PATTERNS

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

8、STATEMENTS AND NOTES：

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

8.2 NOTION:

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

9、CONTACT：

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