



AIP31108

64CH SEGMENT DRIVER FOR DOT MATRIX LCD

1、GENERAL DESCRIPTION

The AIP31108 is a LCD driver LSI with 64channel output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64bit data latch, 64 bit drivers and decoder logics.

It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The AIP31108 composed of the liquid crystal display system in combination with the AIP31107 (64 channel common driver).

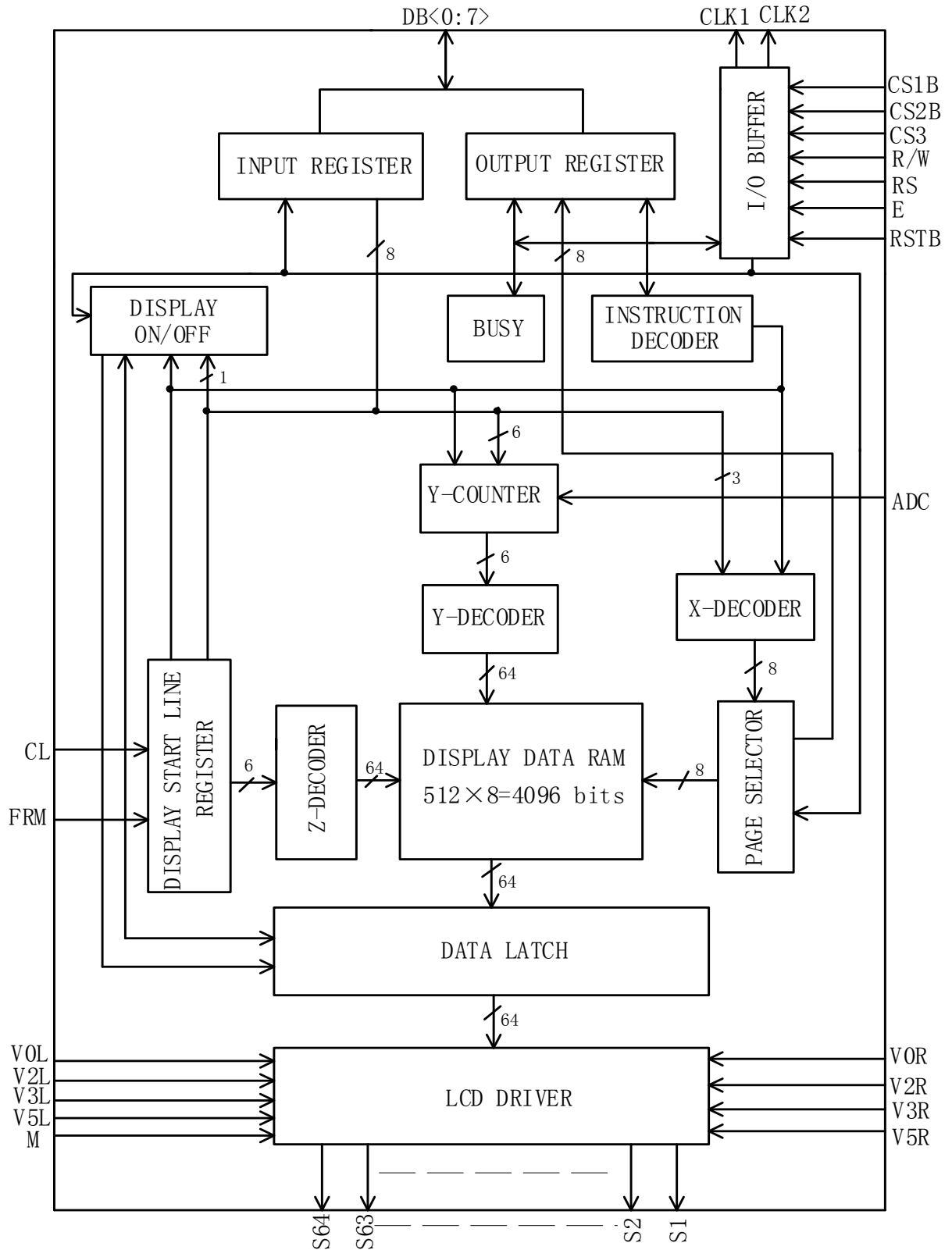
Features

- Dot matrix LCD segment driver with 64 channel output
- Input and Output signal
 - Input: 8 bit parallel display data
 - Control signal from MPU
 - Divided bias voltage (V0R, V0L, V2R, V2L, V3R, V3L, V5R, V5L)
 - Output: 64 channel for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
 - Capacity: 512 bytes (4096 bits)
 - RAM bit data: RAM bit data = 1: ON
 - RAM bit data = 0: OFF
- Applicable LCD duty: 1/32 ~1/64
- LCD driving voltage: 8V ~17V(VDD-VEE)
- Power supply voltage: + 5V \pm 10%
- High voltage CMOS process.
- chip size: 3815 \times 3760 ($\mu\text{m} \times \mu\text{m}$),
- The IC substrate should be connected to VDD or float in the PCB layout artwork.
- 100QFP and bare chip available



2、BLOCK DIAGRAM AND PIN DESCRIPTION

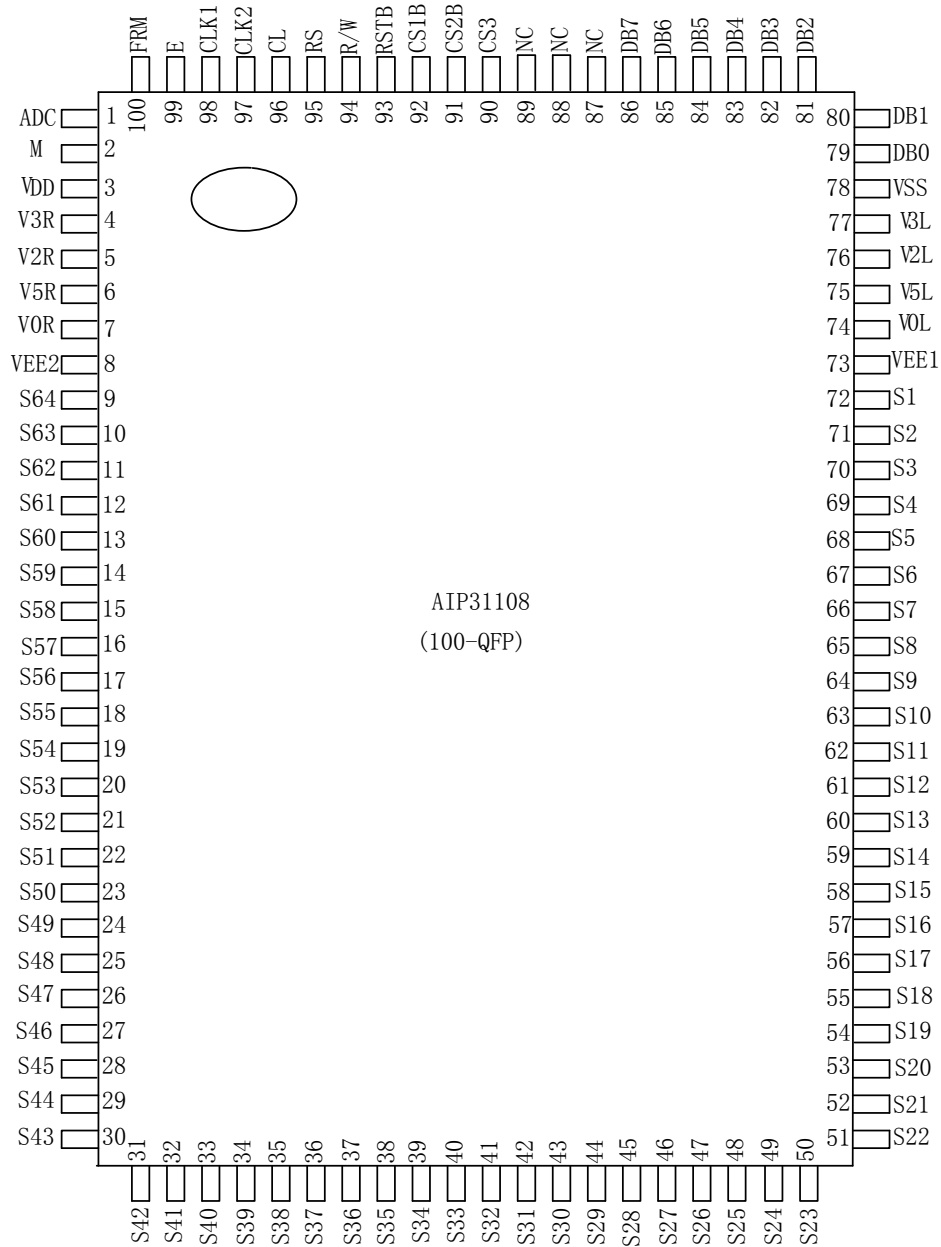
2.1、BLOCK DIAGRAM





2.2、PIN CONFIGURATIONS

QFP-100





2.3、PIN DESCRIPTION

PIN NO.(QFP)	Symbol	I/O	Description				
3 78 73,8	VDD VSS VEE1, 2	Power	For internal logic circuit (+5V ± 10%) GND(0V) For LCD driver circuit VSS=0V,VDD=+5V ± 10%,VDD-VEE=8V~17V VEE1 and VEE2 is connected by the same voltage.				
74,7 76,5 77,4 75,6	V0L,V0R V2L,V2R V3L,V3R V5L,V5R	Power	Bias supply voltage terminals to drive the LCD. <table border="1" style="margin-left: 20px;"> <tr> <td>Select Level</td> <td>Non-Select Level</td> </tr> <tr> <td>V0L(R),V5L(R)</td> <td>V2L(R),V3L(R)</td> </tr> </table> V0L and V0R(V2L&V2R,V3L&V3R,V5L&V5R) should be connected by the same voltage.	Select Level	Non-Select Level	V0L(R),V5L(R)	V2L(R),V3L(R)
Select Level	Non-Select Level						
V0L(R),V5L(R)	V2L(R),V3L(R)						
92 91 90	CS1B CS2B CS3	I	Chip selection In order to interface data for input or output, the terminals have to be CS1B=L,CS2B=L,CS3=H				
2	M	I	Alternating signal input for LCD driving.				
1	ADC	I	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H→Y0:S1-Y63: S64 ADC=L→Y0:S64-Y63: S1				
100	FRM	I	Synchronous control signal. Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.				
99	E	I	Enable signal. write mode (R/W=L) →data of DB<0:7> is latched at the falling edge of E. read mode (R/W=H) → DB<0:7> appears the reading data while E is at high level.				
98 97	CLK1 CLK2	I	2 phase clock signal for internal operation. Used to execute operations for input/output of display RAM data and others.				
96	CL	I	Display synchronous signal. Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.				
95	RS	I	Data or Instruction. RS=H→DB<0:7>: Display RAM Data RS=L→DB<0:7>: Instruction Data				



94	R/W	I	<p>Read or Write. R/W=H → Data appears at DB<0:7> and can be read by the CPU while E=H, CS1B=L, CS2B=L and CS3=H. R/W=L→Display data DB<0:7> can be written at falling of E when CS1B=L, CS2B=L and CS3=H.</p>													
79-86	DB0-DB7	I/O	Data bus. There state I/O common terminal.													
72-9	S1-S64	0	<p>LCD Segment driver output. Display RAM data 1:ON Display RAM data 0:OFF (Relation of display RAM data & M)</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">M</th> <th style="width: 20%;">Data</th> <th style="width: 20%;">Output Level</th> </tr> </thead> <tbody> <tr> <td rowspan="2" style="text-align: center;">L</td> <td style="text-align: center;">L</td> <td style="text-align: center;">V_2</td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">V_0</td> </tr> <tr> <td rowspan="2" style="text-align: center;">H</td> <td style="text-align: center;">L</td> <td style="text-align: center;">V_3</td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">V_5</td> </tr> </tbody> </table>	M	Data	Output Level	L	L	V_2	H	V_0	H	L	V_3	H	V_5
M	Data	Output Level														
L	L	V_2														
	H	V_0														
H	L	V_3														
	H	V_5														
93	RSTB	I	<p>Reset signal. When RSTB=L, 1) ON/OFF register becomes set by 0. (display off) 2) Display start line register becomes set by 0 (Z-address 0 set, display from line 0) After releasing reset, this condition can be changed only by instruction.</p>													
87 88 89	NC		connection.(open)													

3、 ELECTRICAL PARAMETER

3.1、 ABSOLUTE MAXIMUM RATINGS

(Tamb=25°C, All voltage referenced to VSS, unless otherwise specified)

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	VDD	-0.3~+7.0	V	(1)
Supply Voltage	VEE	VDD-19.0~VDD+0.3	V	(4)
Driver Supply Voltage	VB	-0.3~VDD+0.3	V	(1), (3)
	VLCD	VEE-0.3~VDD+0.3	V	(2)
Operating Temperature	TOPR	-30~+85	°C	
Storage Temperature	TSTG	-55~+125	°C	
Soldering Temperature	TL	245(10s)	°C	



- *1. Based on $V_{SS}=0V$.
- *2. Applies the same supply voltage to V_{EE1} and V_{EE2} . $V_{LCD}=V_{DD}-V_{EE}$.
- *3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0~DB7.
- *4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).
Voltage level: $V_{DD} \geq V_{0L} = V_{0R} \geq V_{2L} = V_{2R} \geq V_{3L} = V_{3R} \geq V_{5L} = V_{5R} \geq V_{EE}$.

3.2、 ELECTRICAL CHARACTERISTICS

3.2.1 DC Characteristics ($V_{DD}=+5V \pm 10\%$, $V_{SS}=0V$, $|V_{DD}-V_{EE}|=8 \sim 17V$, $T_a=-30 \sim +85^\circ C$,)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
Input High Voltage	V_{IH1}	—	0.7VDD	—	VDD	V	(1)
	V_{IH2}	—	2.0	—	VDD	V	(2)
Input Low Voltage	V_{IL1}	—	0	—	0.3VDD	V	(1)
	V_{IL2}	—	0	—	0.8	V	(2)
Output High Voltage	V_{OH}	$I_{OH}=-200\mu A$	2.4	—	—	V	(3)
Output Low Voltage	V_{OL}	$I_{OL}=1.6mA$	—	—	0.4	V	(3)
Input Leakage Current	I_{LKG}	$V_{IN}=V_{SS}-V_{DD}$	-1.0	—	1.0	μA	(4)
Three-state(OFF) Input Current	I_{TSL}	$V_{IN}=V_{SS}-V_{DD}$	-5.0	—	5.0	μA	(5)
Driver Input Leakage Current	I_{DIL}	$V_{IN}=V_{EE}-V_{DD}$	-2.0	—	2.0	μA	(6)
Operating Current	I_{DD1}	During Display	—	—	150	μA	(7)
	I_{DD2}	During Access Access Cycle=1MHz	—	—	600	μA	(7)
On Resistance	R_{ON}	$V_{DD}-V_{EE}=15V$ $I_{LOAD}=\pm 0.1mA$	—	—	7.5	$K\Omega$	(8)

- *1. CL, FRM, M, RSTB, CLK1, CLK2
- *2. CS1B, CS2B, CS3, E, R/W, RS, DB0~DB7
- *3. DB0~DB7
- *4. Except DB0~DB7
- *5. DB0~DB7 at High Impedance
- *6. V0L(R), V2L(R), V3L(R), V5L(R)
- *7. 1/64 duty, FCLK=250KHZ, Frame Frequency=70HZ, Output: No Load
- *8. $V_{DD}-V_{EE}=15.5V$ $V_{0L(R)}>V_{2L(R)}=V_{DD}-2/7$ ($V_{DD}-V_{EE}$) $>V_{3L(R)}=V_{EE}+2/7(V_{DD}-V_{EE})>V_{5L(R)}$



3.2.2 AC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, T_a=-30~+85°C)

Clock Timing

Characteristic	Symbol	Min	Typ	Max	
CLK1, CLK2 Cycle Time	t _{CY}	2.5	—	20	us
CLK1 LOW Level Width	t _{WL1}	625	—	—	ns
CLK2 LOW Level Width	t _{WL2}	625	—	—	
CLK1 HIGH Level Width	t _{WH1}	1875	—	—	
CLK2 HIGH Level Width	t _{WH2}	1875	—	—	
CLK1-CLK2 Phase Difference	t _{D12}	625	—	—	
CLK2-CLK1 Phase Difference	t _{D21}	625	—	—	
CLK1, CLK2 Rise Time	t _R	—	—	150	
CLK1, CLK2 Fall Time	t _F	—	—	150	

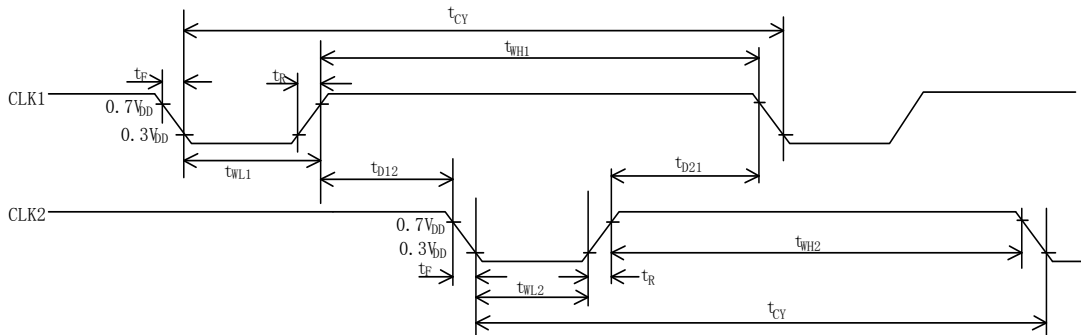


Fig1.External clock waveform

Display Control Timing

Characteristic	Symbol	Min	Typ	Max	Unit
FRM Delay Time	t _{DF}	-2	—	+2	us
M Delay Time	t _{DM}	-2	—	+2	us
CL LOW Level Width	t _{WL}	35	—	—	us
CL HIGH Level Width	t _{WH}	35	—	—	us

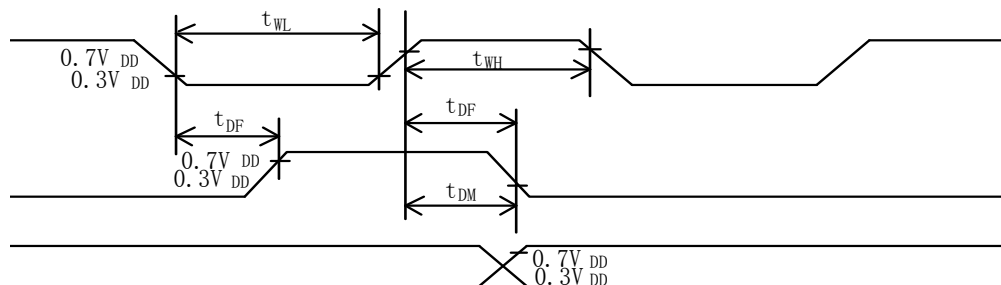


Fig2. Display control signal waveform



MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	t_C	1000	—	—	ns
E High Level Width	t_{WH}	450	—	—	ns
E Low Level Width	t_{WL}	450	—	—	ns
E Rise Time	t_R	—	—	25	ns
E Fall Time	t_F	—	—	25	ns
Address Set-Up Time	t_{ASU}	140	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Data Set-Up Time	t_{DSU}	200	—	—	ns
Data Delay Time	t_D	—	—	320	ns
Data Hold Time (Write)	t_{DHW}	10	—	—	ns
Data Hold Time (Read)	t_{DHR}	20	—	—	ns

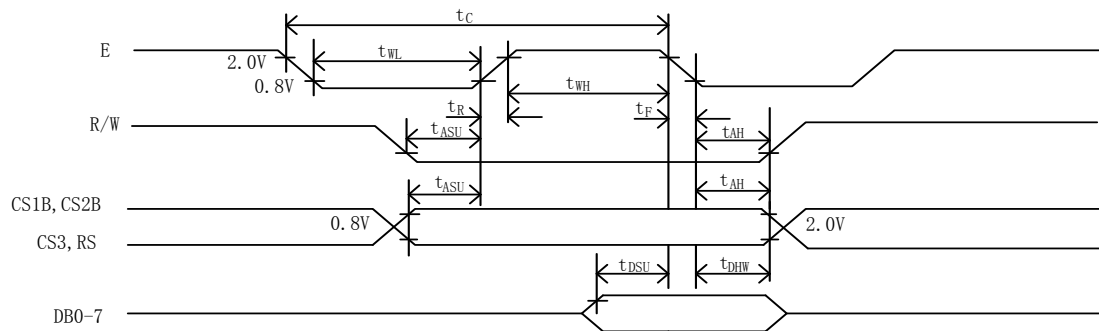


Fig 3. MPU write timing

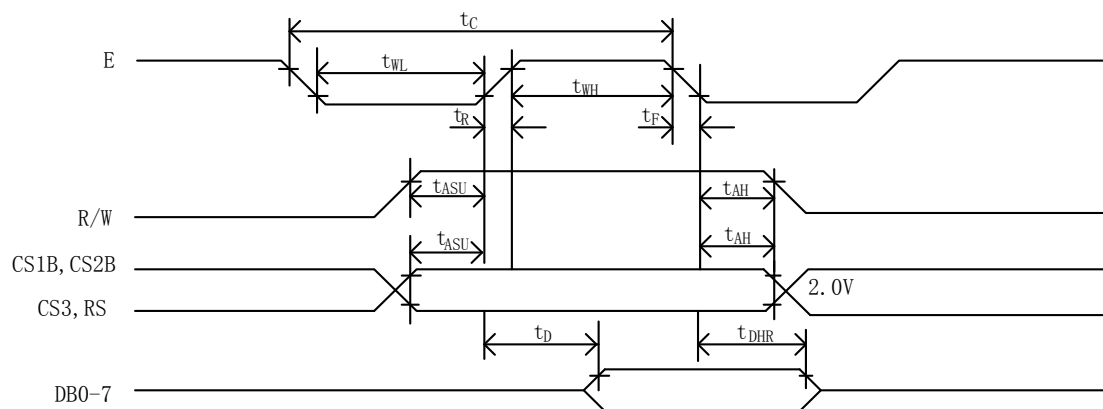
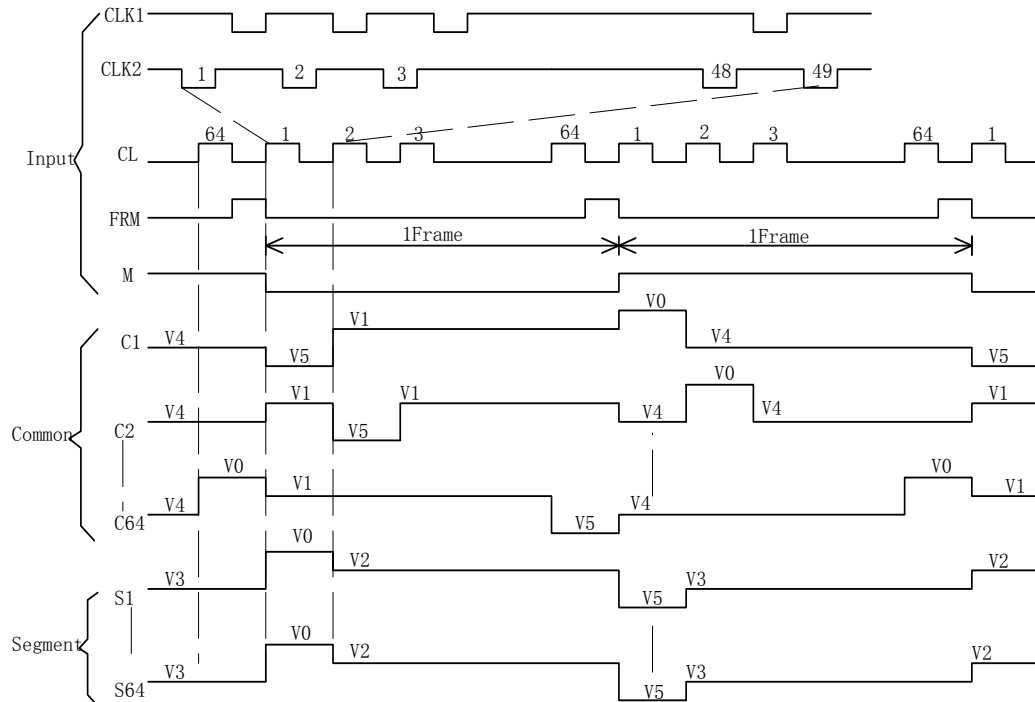


Fig 4. MPU Read timing



4. 2、 APPLICATION NOTE

OPERATING PRINCIPLES & METHODS

I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But



status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

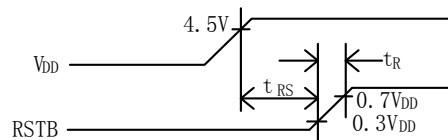
When RSTB becomes low, following procedure is occurred.

1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction.

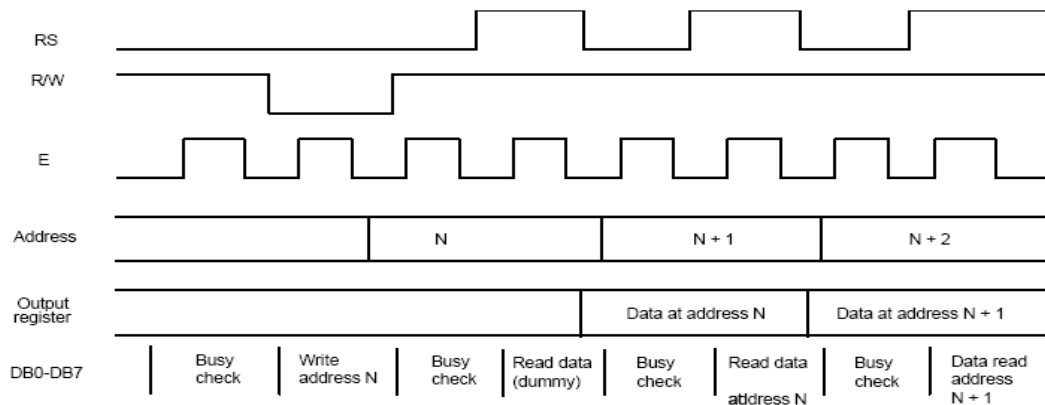
Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	—	—	μs
Rise Time	t_R	—	—	200	ns

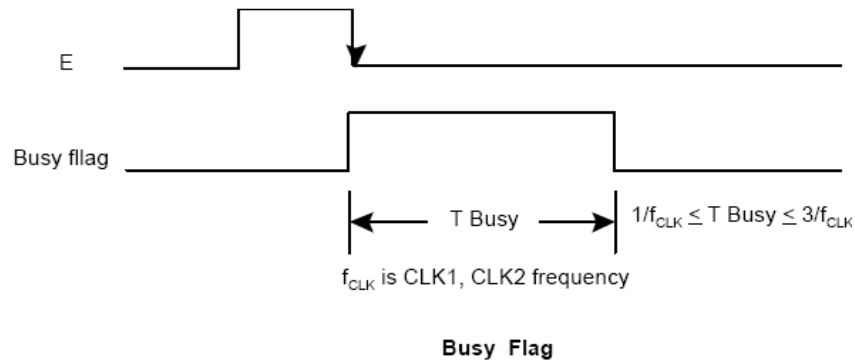


Busy flag

Busy flag indicates that AIP31108 is operating or no operating. When busy flag is high, AIP31108 is in internal operating. When busy flag is low, AIP31108 can accept the data or instruction. DB7 indicates busy flag of the AIP31108.



Busy Check



Display On/Off Flip - Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

X Page Register

X page register designates pages of the internal display data RAM.
Count function is not available. An address is set by instruction.

Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC=H → Yaddress 0:S1 -Y address 63:64

ADC=L → Yaddress 0:S64 -Y address 63:S1

ADC terminal connect the V_{DD} or V_{SS} .

Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.

Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.



It is used for scrolling of the liquid crystal display screen.

Display Control Instruction

The display control instructions control the internal state of the AIP31108. Instruction is received from MPU to AIP31108 for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function	
Display ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON	
Set Address (Y address)	L	L	L	H	Y address (0~63)						Sets the Y address in the Y address counter.	
Set Page (X address)	L	L	H	L	H	H	H	Page (0-7)			Sets the X address at the X address register.	
Display Start Line (Z address)	L	L	H	H	Display start line (0-63)						Indicates the display data RAM displayed at the top of the screen.	
Status Read	L	H	busy	L	On/off	reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset	
Write Display Data	H	L	Write Data									Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	H	H	Read Data									Reads data (DB0:7) from display data RAM to the data bus.

Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.

Though the data is not on the screen with D=0, it remains in the display data RAM.

Therefore, you can make it appear by changing D=0 into D=1.



Set Address (Y Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0 ~ AC5) of the display data RAM is set in the Y address counter.

An address is set by instruction and increased by 1 automatically by read or write operations of display data.

Set Page (X Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address(AC0 ~ AC2) of the display data RAM is set in the X address register.

Writing or reading to or from MPU is executed in this specified page until the next page is set.

Display Start Line (Z Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0 ~ AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others(1/32 ~ 1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

- **BUSY**

When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.

When BUSY is 0, the Chip is ready to accept any instructions.

- **ON/OFF**

When ON/OFF is 1, the display is on.

When ON/OFF is 0, the display is off.

- **RESET**

When RESET is 1, the system is being initialized. In this condition, no instructions except status read can be accepted.

When RESET is 0, initializing has finished and the system is in the usual operation condition.

Write Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0 ~ D7) into the display data RAM. After writing instruction, Y address is increased by 1 automatically.

Read Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0 ~ D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.



4.3 SOFT EXAMPLE

The 128x64 dot matrix LCD module is formed by one AIP31107 and two AIP31108s. AT89C52 will drive the module by indirect controlling method. When CS1B=L, CS2B=L, CS3=H, the AIP31108 is working. Binding the AIP31108, CS1B and CS2B will be connected GND directly, but the CS3B must be connected the module select terminal. The CS3 of two AIP31108s will be defined as CS1 and CS2.

RS	EQU	P1.1	
RW	EQU	P1.2	
E	EQU	P1.0	
CS1	EQU	P1.3	
CS2	EQU	P1.4	
RST	EQU	P1.5	
DB0~7	EQU	P0	
COM	EQU	5EH	; Instruction data RAM
DAT	EQU	5FH	; display data RAM

(1)、Read Busy flag subprogram

```
BUSYT: CLR    RS
        SETB   RW
BUSYT1: MOV    A, #0FFH
        MOV    P0, A
        SETB   E
        NOP
        NOP
        MOV    A, P0
        JB    ACC.7, BUSYT1
        CLR   E
        RET
```



(2)、Write instruction subprogram

```
COMW:  SETB    CS1      ; According to the AIP31108, setting CS1 and CS2
        LCALL   BUSYT
        LCALL   COMW1
        CLR     CS1      ; According to the AIP31108, setting CS1 and CS2
        RET
COMW1:  CLR     RW
        CLR     RS
        NOP
        NOP
        MOV     P0, COM
        SETB   E
        NOP
        NOP
        CLR     E
        RET
```

(3)、Write data subprogram

```
DATW:  SETB    CS1      ; According to the AIP31108, setting CS1 and CS2
        LCALL   BUSYT
        LCALL   DATW1
        CLR     CS1      ; According to the AIP31108, setting CS1 and CS2
        RET
DATW1:  CLR     RW
        SETB   RS
        NOP
        NOP
        MOV     P0, DAT
        SETB   E
        NOP
        NOP
        CLR     E
        RET
```




(4)、Read data subprogram

```
DATR:  SETB   CS1       ; According to the AIP31108, setting CS1 and CS2
        LCALL  BUSYT
        LCALL  DATR1
        CLR    CS1       ; According to the AIP31108, setting CS1 and CS2
        RET

DATR1:  MOV    COM, #0B8H ; According to the reading location,
                               ;setting the page address

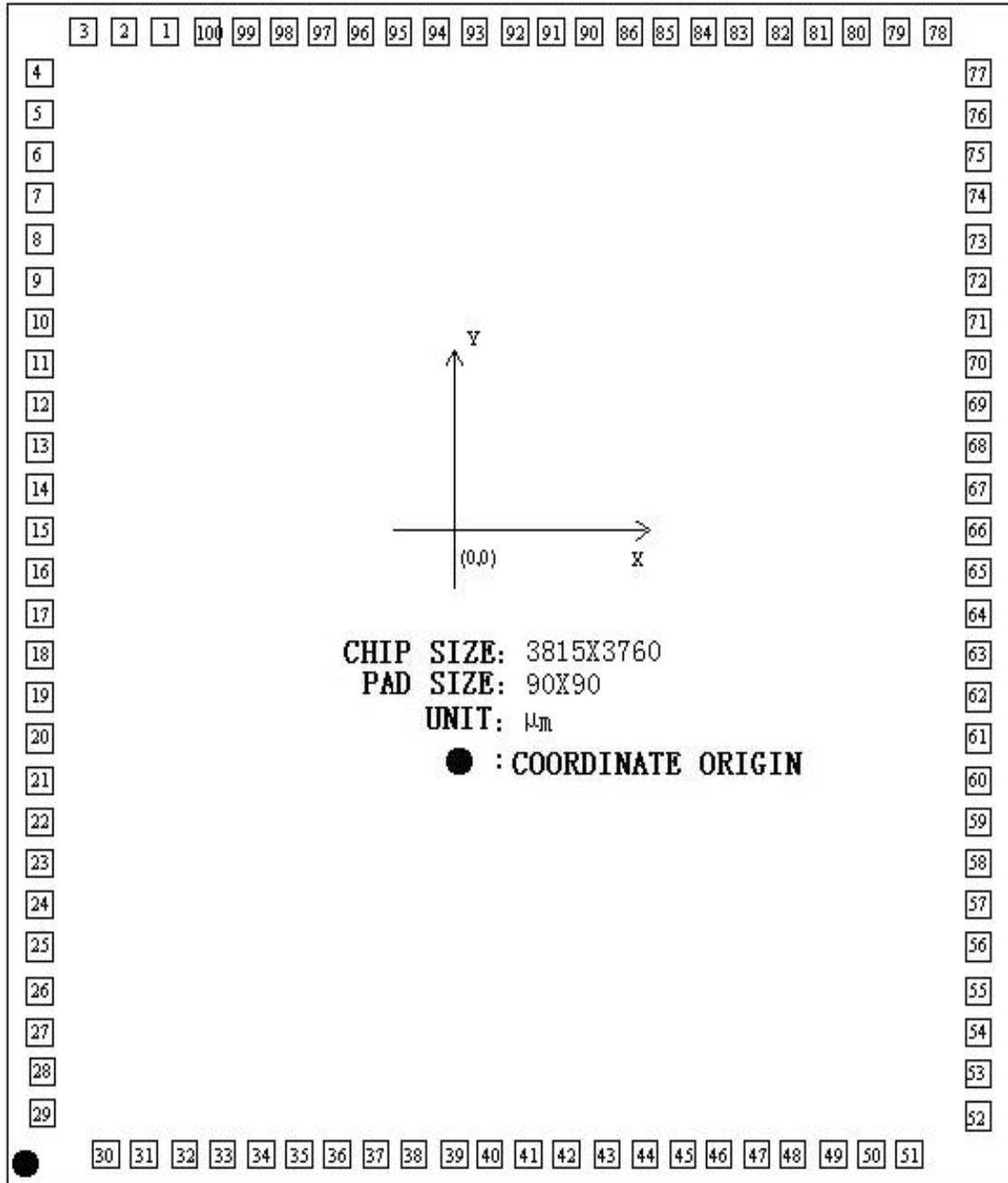
        LCALL  COMW
        MOV    COM, #40H  ; According to the reading location, setting
                               ;the column address

        LCALL  COMW
        SETB   CS1       ; According to the AIP31108, setting CS1 and CS2
        LCALL  BUSYT
        SETB   RW
        SETB   RS
        SETB   E
        NOP
        NOP
        MOV    A, P0
        CLR    E
        CLR    CS1       ; According to the AIP31108, setting CS1 and CS2
        RET
```



5、PAD DIAGRAM AND PAD LOCATION

5.1、PAD DIAGRAM





5.2、PAD Location (UNIT: μm)

NO.	NAME	X	Y	NO.	NAME	X	Y
1	ADC	779.30	3532.45	51	S22	3119.40	75.00
2	M	659.30	3532.45	52	S21	3637.80	498.45
3	VDD	534.30	3532.45	53	S20	3637.80	618.45
4	V3	75.00	3503.45	54	S19	3637.80	738.45
5	V2	75.00	3383.45	55	S18	3637.80	858.45
6	V5	75.00	3263.45	56	S17	3637.80	978.45
7	V0	75.00	3143.45	57	S16	3637.80	1098.45
8	VEE	75.00	3023.45	58	S15	3637.80	1218.45
9	S64	75.00	2901.45	59	S14	3637.80	1338.45
10	S63	75.00	2778.45	60	S13	3637.80	1458.45
11	S62	75.00	2658.45	61	S12	3637.80	1578.45
12	S61	75.00	2538.45	62	S11	3637.80	1698.45
13	S60	75.00	2418.45	63	S10	3637.80	1818.45
14	S59	75.00	2298.45	64	S9	3637.80	1938.45
15	S58	75.00	2178.45	65	S8	3637.80	2058.45
16	S57	75.00	2058.45	66	S7	3637.80	2178.45
17	S56	75.00	1938.45	67	S6	3637.80	2298.45
18	S55	75.00	1818.45	68	S5	3637.80	2418.45
19	S54	75.00	1698.45	69	S4	3637.80	2538.45
20	S53	75.00	1578.45	70	S3	3637.80	2658.45
21	S52	75.00	1458.45	71	S2	3637.80	2778.45
22	S51	75.00	1338.45	72	S1	3637.80	2898.45
23	S50	75.00	1218.45	73	VEE	3637.80	3023.45
24	S49	75.00	1098.45	74	V0	3637.80	3143.45
25	S48	75.00	978.45	75	V5	3637.80	3263.45
26	S47	75.00	858.45	76	V2	3637.80	3383.45
27	S46	75.00	738.45	77	V3	3637.80	3503.45
28	S45	75.00	618.45	78	GND	3179.95	3532.45
29	S44	75.00	498.45	79	DB0	3059.30	3532.45
30	S43	599.40	75.00	80	DB1	2939.30	3532.45



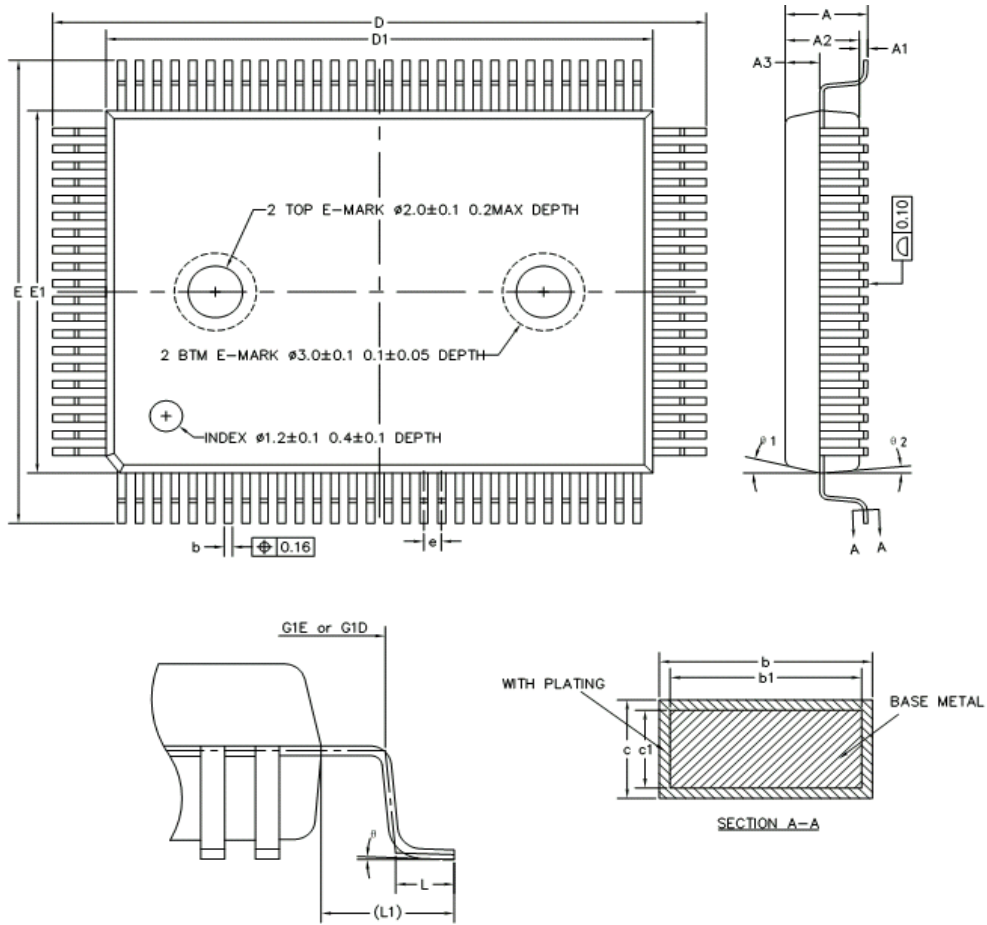
Wuxi I-CORE Electronics Co., Ltd.

31	S42	719.40	75.00	81	DB2	2819.30	3532.45
32	S41	839.40	75.00	82	DB3	2699.30	3532.45
33	S40	959.40	75.00	83	DB4	2579.30	3532.45
34	S39	1079.40	75.00	84	DB5	2459.30	3532.45
35	S38	1199.40	75.00	85	DB6	2339.30	3532.45
36	S37	1319.40	75.00	86	DB7	2219.30	3532.45
37	S36	1439.40	75.00	87	NC		
38	S35	1559.40	75.00	88	NC		
39	S34	1679.40	75.00	89	NC		
40	S33	1799.40	75.00	90	CS3	2099.30	3532.45
41	S32	1919.40	75.00	91	CS2B	1979.30	3532.45
42	S31	2039.40	75.00	92	CS1B	1859.30	3532.45
43	S30	2159.40	75.00	93	RSTB	1739.30	3532.45
44	S29	2279.40	75.00	94	RW	1619.30	3532.45
45	S28	2399.40	75.00	95	RS	1499.30	3532.45
46	S27	2519.40	75.00	96	CL	1379.30	3532.45
47	S26	2639.40	75.00	97	CLK2	1259.30	3532.45
48	S25	2759.40	75.00	98	CLK1	1139.30	3532.45
49	S24	2879.40	75.00	99	E	1019.30	3532.45
50	S23	2999.40	75.00	100	FRM	899.30	3532.45



6、PACKAGE INFORMATION

6.1、QFP100-14x20-0.65



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	-	-	3.30
A1	0.10	-	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	-	0.37
b1	0.27	0.30	0.33
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D	22.00REF		
G1E	16.00REF		
L	0.60	0.80	1.00
L1	1.95REF		
θ	0°	2°	8°
$\theta 1$	11°	13°	15°
$\theta 2$	3°	5°	7°



7、STATEMENTS AND NOTES:

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
Chip	○	○	○	○	○	○
The lead	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。					

7.2 NOTION:

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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