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AK1221

3500MHz High Linearity Mixer

1. Overview

The AK1221 is high linearity mixer. RF and Lo frequency range coverage is from 700 to 3500MHz and IF coverage is from 20 to 200MHz. The RF input provides single-ended 50Ω interface. Lo ports are 50Ω matched and complementary input should be decoupled to the ground. IF output ports are differential open drain outputs. The linearity and power consumption performances can be optimized by the resistance connected to the BIAS Pin.

2. Features

- ☐ Operating Frequency: 700MHz to 3500MHz
- ☐ Linearity vs. Power selectable architecture
  Power Consumption: 45mA, IIP3: +25dBm, Gain: -0.5dB, NF: 14dB
- ☐ Lo input level: 0dBm ±5dB
- ☐ Operating Supply Voltage: 4.75 to 5.25 V
- ☐ Package: 16pin UQFN (0.5mm pitch, 3mm × 3mm × 0.60mm)
- ☐ Operating Temperature Range: -40 to 85°C

3. Table contents

4. Block Diagram

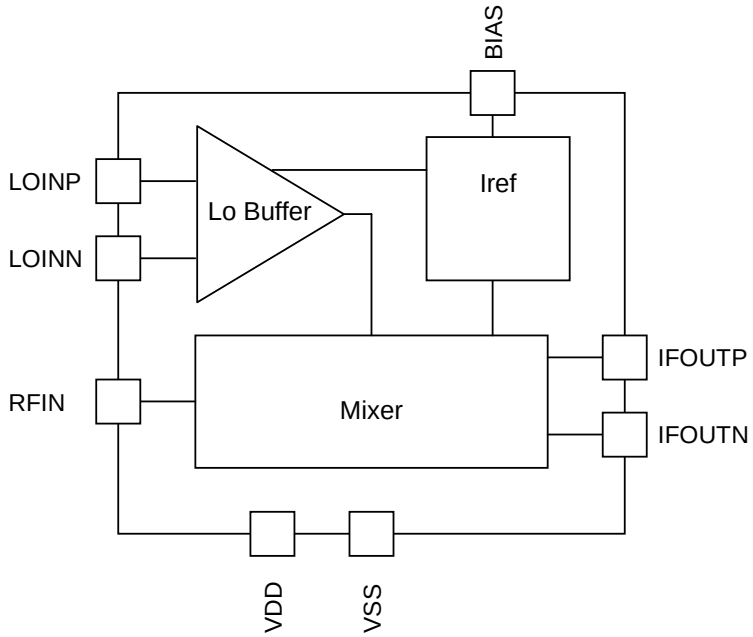


Fig. 1 Block Diagram

5. System Diagram

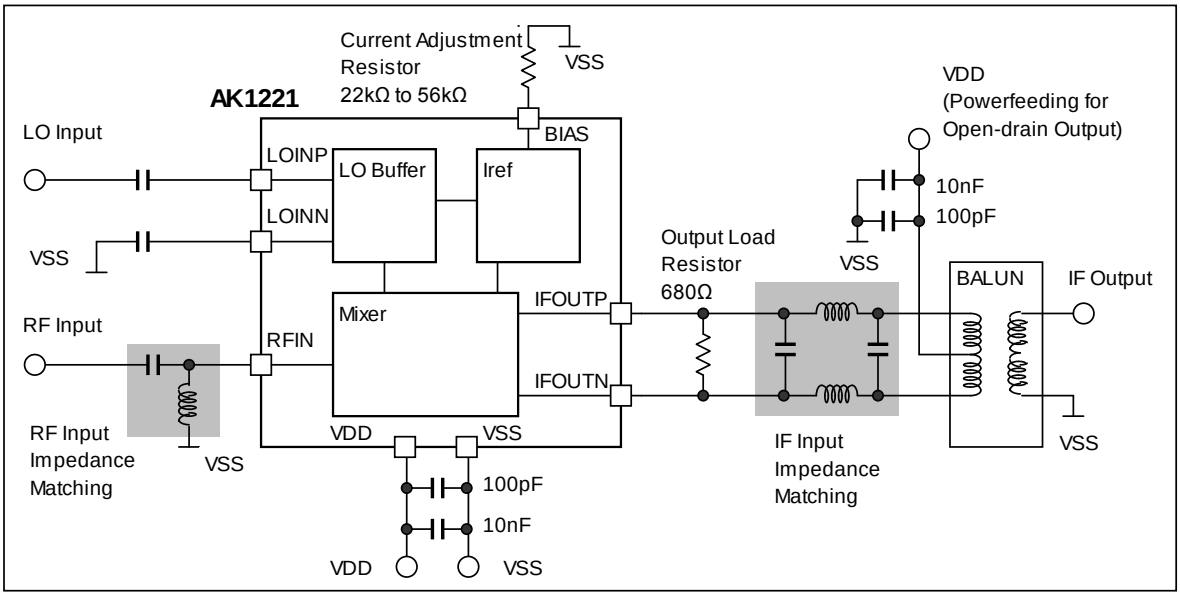


Fig. 2 System Diagram

6. Pin Functional Description

Table 1 Pin Function

No.	Name	I/O	Pin Functions	Remarks
1	RFIN	AI	RF Input	Connecting an inductor between this pin and ground.
2	VSS	G	Ground pin	
3	VSS	G	Ground pin	
4	LOINN	AI	Lo Input Negative	
5	LOINP	AI	Lo Input Positive	
6	VDD	P	Power Supply	
7	VDD	P	Power Supply	
8	VDD	P	Power Supply	
9	VDD	P	Power Supply	
10	BIAS	AIO	Resistance pin for current adjustment	Connecting a resistor between this pin and ground.
11	IFOUTN	AO	IF Output Negative	This pin is open drain output. It needs power feeding via an inductor.
12	IFOUTP	AO	IF Output Positive	This pin is open drain output. It needs power feeding via an inductor.
13	VSS	G	Ground pin	
14	VSS	G	Ground pin	
15	VSS	G	Ground pin	
16	VSS	G	Ground pin	

Note) The exposed pad at the center of the backside should be connected to ground.

AI : Analog input pin	AO : Analog output pin	AIO : Analog I/O pin
P : Power supply pin	G : Ground pin	

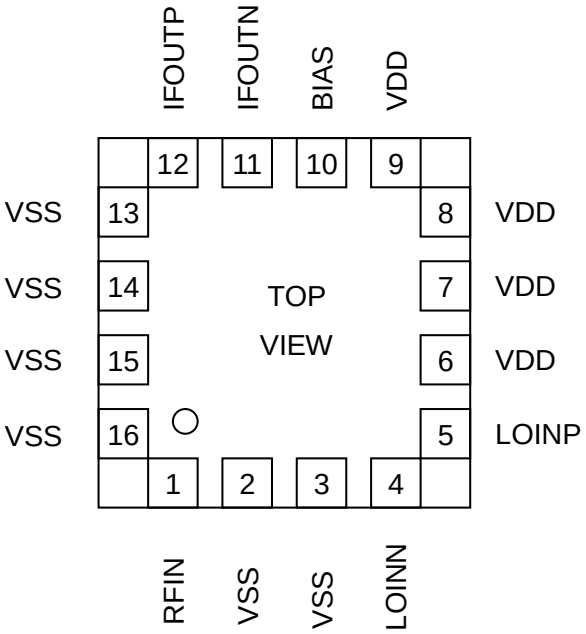


Fig. 3 Package Pin Layout

7. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	-0.3	5.5	V	
RF Input Power	RFPOW		12	dBm	
LO Input Power	LOPOW		12	dBm	
Storage Temperature	Tstg	-55	125	°C	

Exceeding these maximum ratings may result in damage to the AK1221. Normal operation is not guaranteed at these extremes.

8. Recommended Operating Range

Table 3 Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD	4.75	5	5.25	V	

The specifications are applicable within the recommended operating range (supply voltage/operating temperature).

9. Electrical Characteristics

1. Analog Circuit Characteristics

Unless otherwise noted IF output=150MHz, Lo Input Level=-5dBm to +5dBm, Output Load Resistor（RLoad）=680Ω, VDD=4.75 to 5.25V, Ta=-40°C to 85°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
RF Input Frequency		700		3500	MHz	
Lo Input Frequency		700		3500	MHz	
IF output Frequency		20		200	MHz	
Lo Input Power		-5	0	+5	dBm	
Current Adjustment Resistor(BIAS)		22		56	kΩ	
IDD	BIAS=22kΩ		64	87	mA	The total current of VDD pin, IFOUTP pin and IFOUTN pin.
	BIAS=33kΩ		45	64	mA	
	BIAS=56kΩ		30	44	mA	
RFIN=2500MHz, Current Adjustment Resistor =33kΩ						
Conversion Gain		-2.5	-0.5	1.5	dB	
SSB Noise Figure			14	16.5	dB	Design guarantee value
IP1dB		7	10		dBm	
IIP3		21	25		dBm	Design guarantee value

10. Typical Performance

Unless otherwise noted, RF input =2500MHz, Lo input =2350MHz, IF output =150MHz,
Output Load Resistor (RLoad)=680Ω

1. Current Adjustment Resistor vs. IIP, NF, P1dB, Gain, IDD

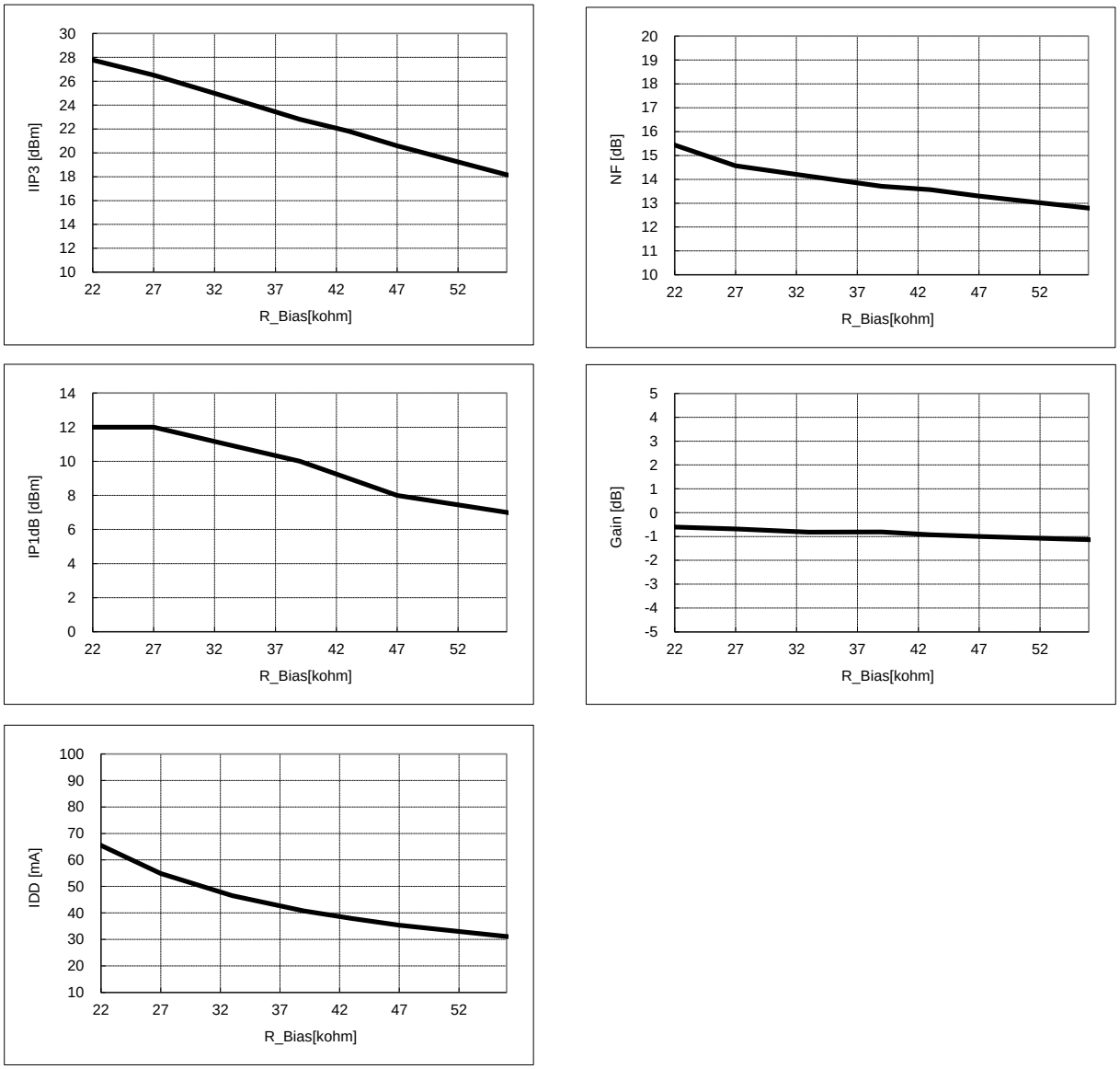


Fig. 4 Current Adjustment Resistor vs. IIP3, NF, P1dB, Gain, IDD

Note) A resistor with 5% tolerance are used.

2. Over temperature vs. IIP3, NF, P1dB, Gain, IDD

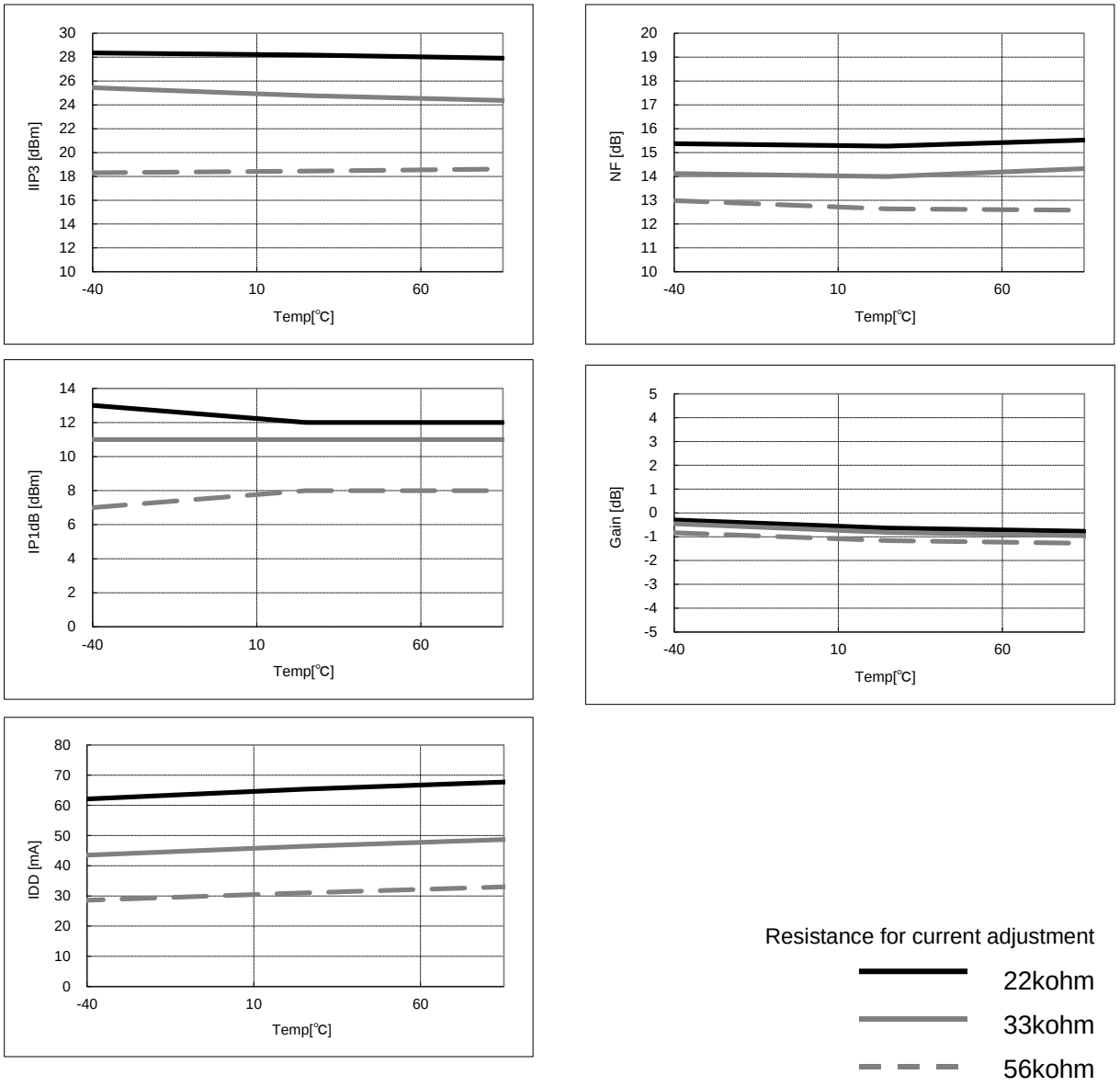


Fig. 5 Over temperature vs. IIP3, NF, IP1dB, Gain, IDD

3. Supply voltage vs. IIP3, NF, P1dB, Gain, IDD

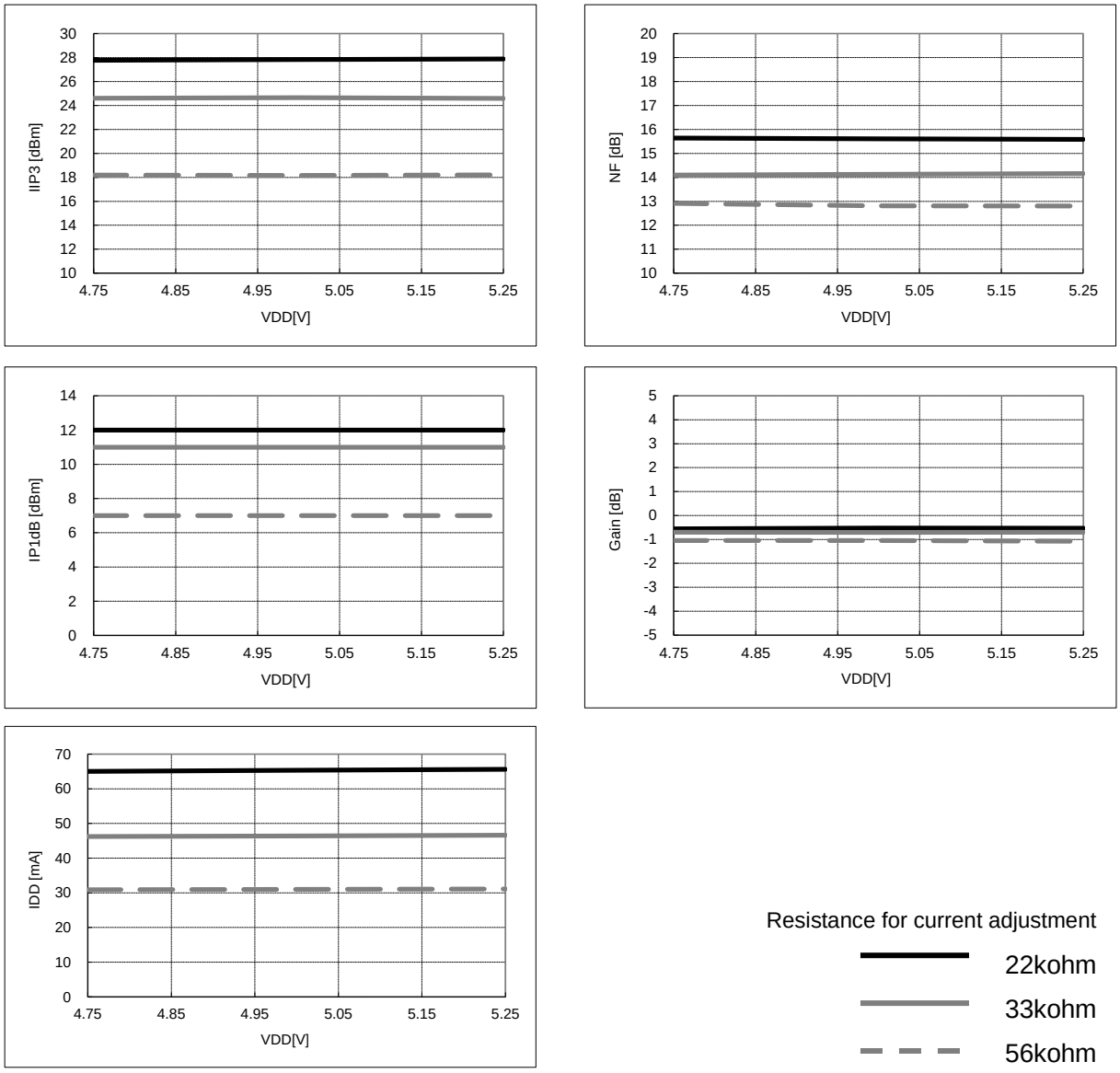


Fig. 6 Supply voltage vs. IIP3, NF, IP1dB, Gain, IDD

4. RF input frequency vs. IIP3, NF, Gain

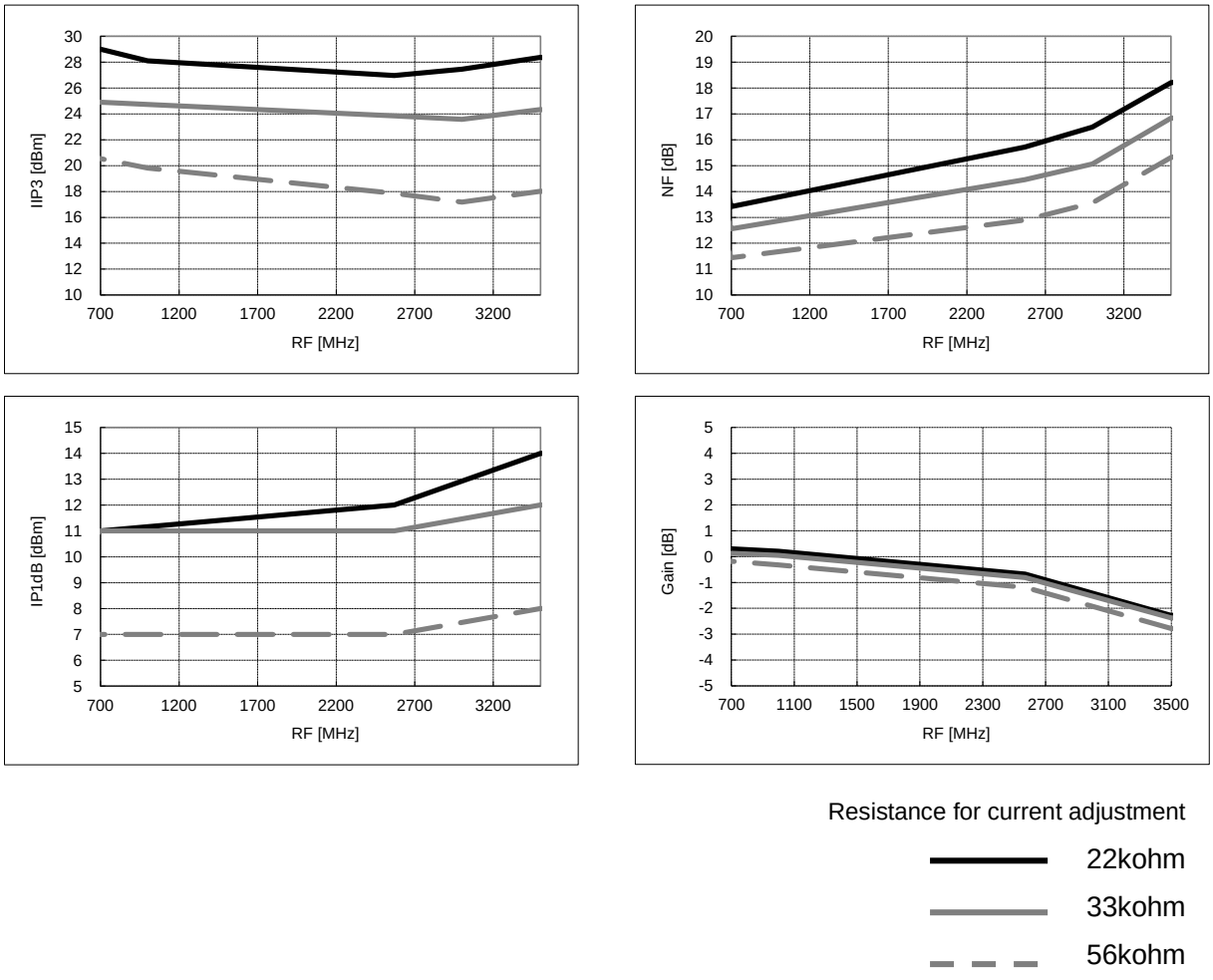


Fig. 7 RF input frequency vs. IIP3, NF, Gain

5. IF input frequency vs. IIP3, NF, Gain

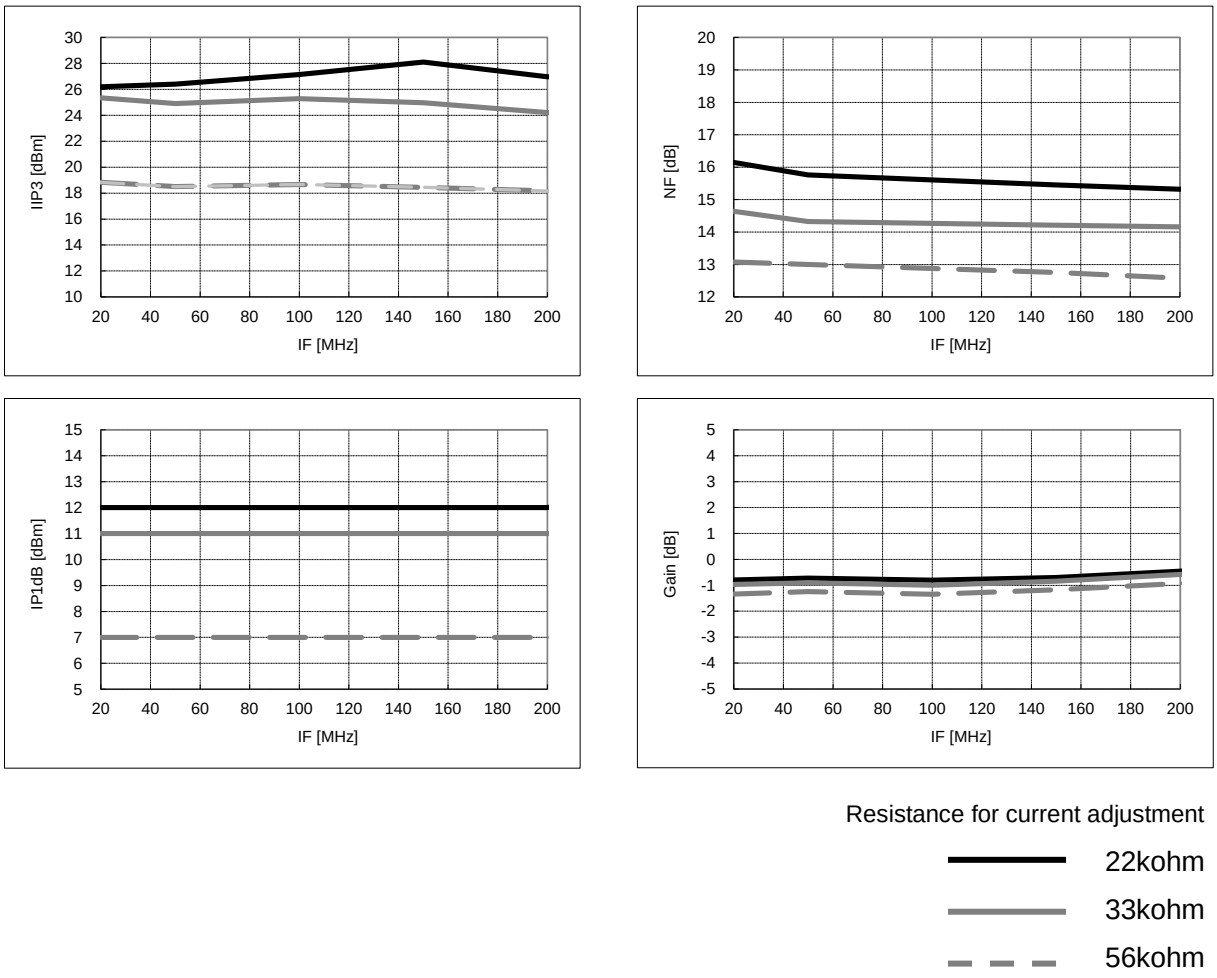


Fig. 8 IF input frequency vs. IIP3, NF, Gain

6. Lo input power vs. IIP3, NF, Gain

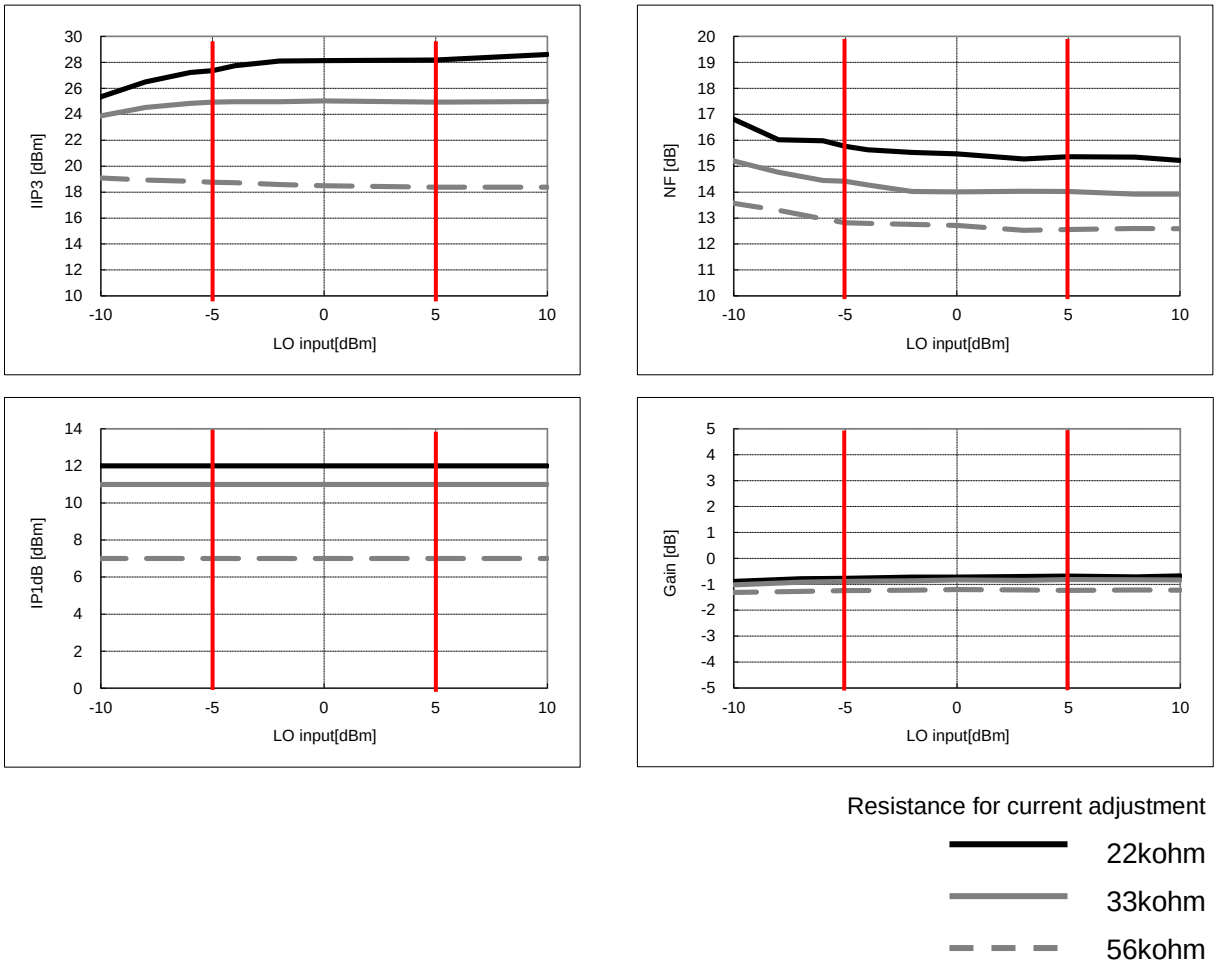


Fig. 9 Lo input power vs. IIP3, NF, Gain

7. Output Load Resistor（RLoad） vs. IIP3, NF, Gain

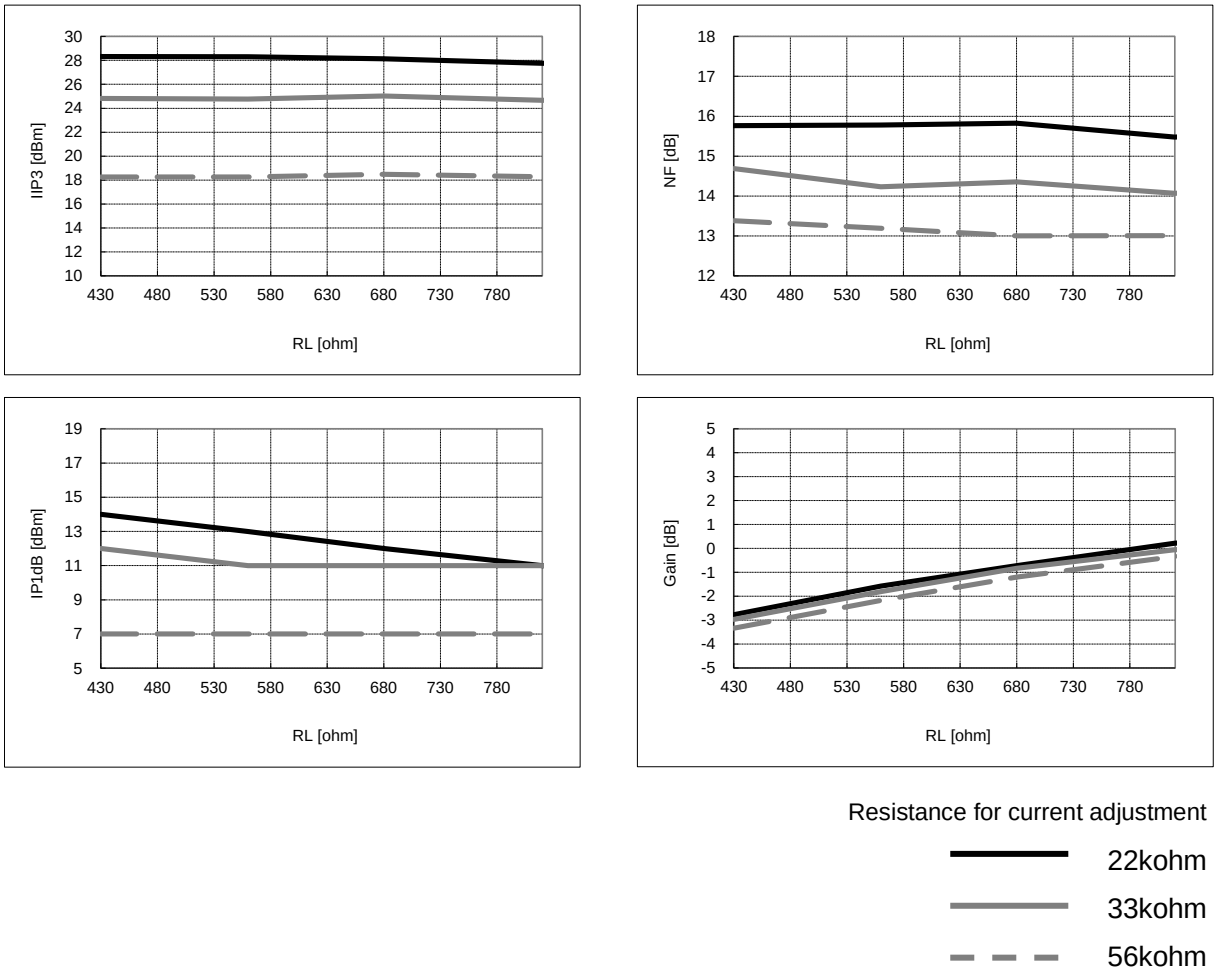


Fig. 10 Output Load Resistor（RLoad） vs. IIP3, NF, Gain

8. Leakage

RFIN=2500MHz,-20dBm,LO input=2350MHz,0dBm,RLoad=680Ω,Ta=25℃ VDD=5V

Parameter	BIAS	Typ.	Unit
RF – LO Leakage	22kΩ	-36	dBc
	56kΩ	-36	dBc
RF – IF Leakage	22kΩ	-61	dBc
	56kΩ	-57	dBc
LO – RF Leakage	22kΩ	-44	dBc
	56kΩ	-44	dBc
LO – IF Leakage	22kΩ	-58	dBc
	56kΩ	-66	dBc

11. Typical Evaluation Board Schematic

1. Typical Evaluation Board Schematic

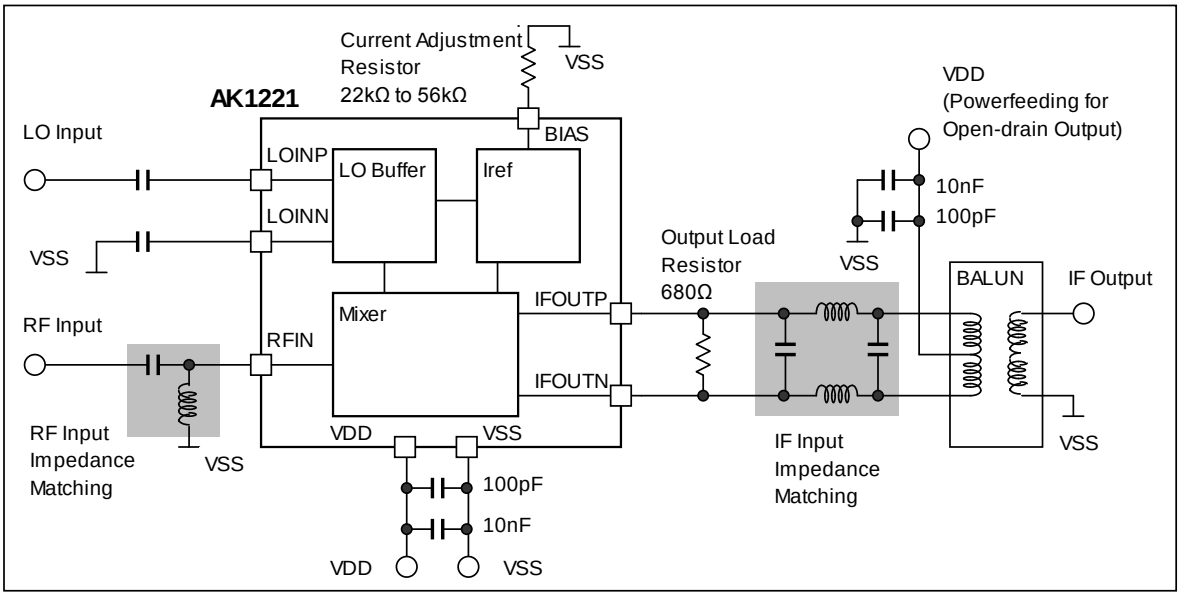


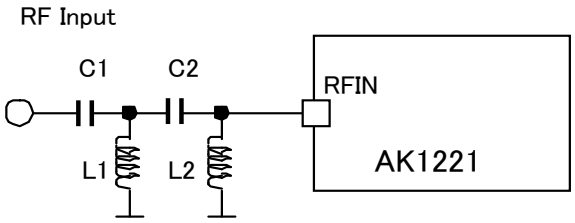
Fig.11 Typical Evaluation Board Schematic

Note 1) The open drain output needs power feeding via a inductor. (IFOUTP pin and IFOUTN pin)

Note 2) It is necessary to adjust impedance matching as to its setting frequency. (RF input and IF output)

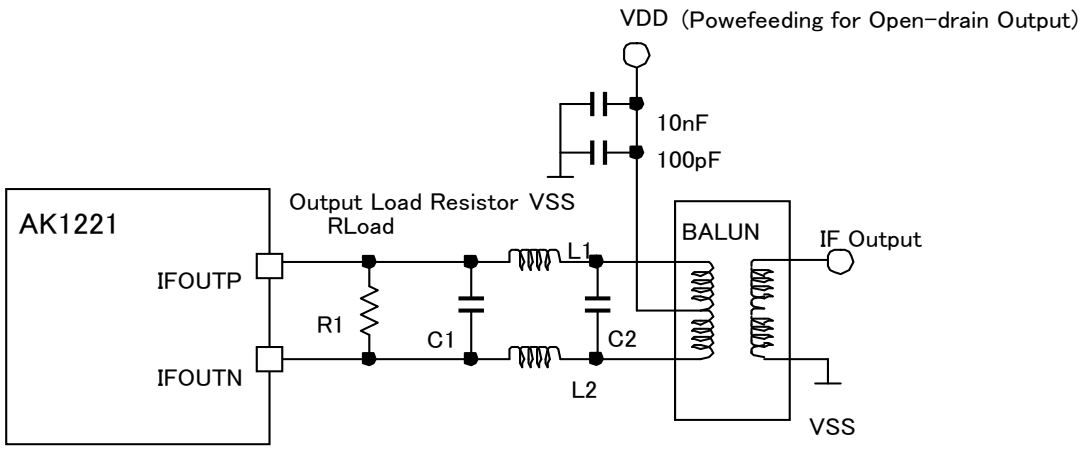
2. Example of impedance matching

2 -1 RFIN



Frequency[MHz]	C1[pF]	C2[pF]	L1[nH]	L2[nH]	Impedance[ohm]
700	none	20	none	39	42.9 - j5.4
2500	39	2.2	1.8	10	61.2 - j12.8
3500	39	1.0	1.0	10	40.7 - j5.1

2 - 2 IFOUT

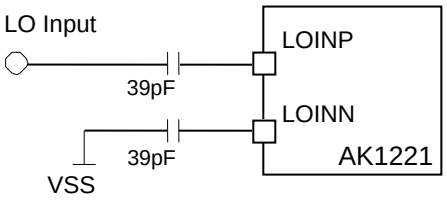


Frequency [MHz]	R1 [ohm]	C1 [pF]	C2 [pF]	L1 [nH]	L2 [nH]	Impedance[ohm]
20	680	15	none	1200 *1	1200 *1	56.6 – j4.5
150	680	1	None	180 *2	180 *2	52.6 – j1.6
200	680	none	none	150 *2	150 *2	47.0 – j11.9

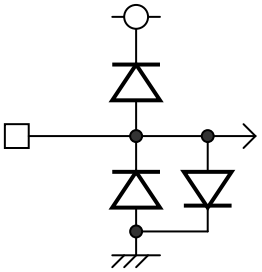
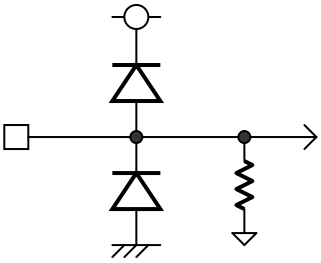
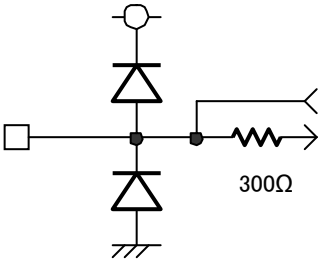
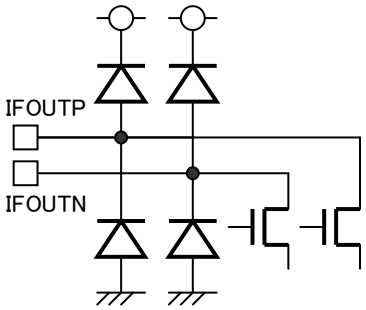
∗1)Murata LQW21A series

∗2)Murata LQW18A series

2 – 3 LOINP/LOINN



12. LSI Interface Schematic

No.	Name	I/O	Function
1	RFIN	I	**RF Input pin** 
4	LOINN	I	**Lo Input pins**
5	LOINP		
10	BIAS	I/O	**Analog I/O pin** 
11	IFOUTN	O	**IF Output pins**
12	IFOUTP		

13. Outer Dimensions

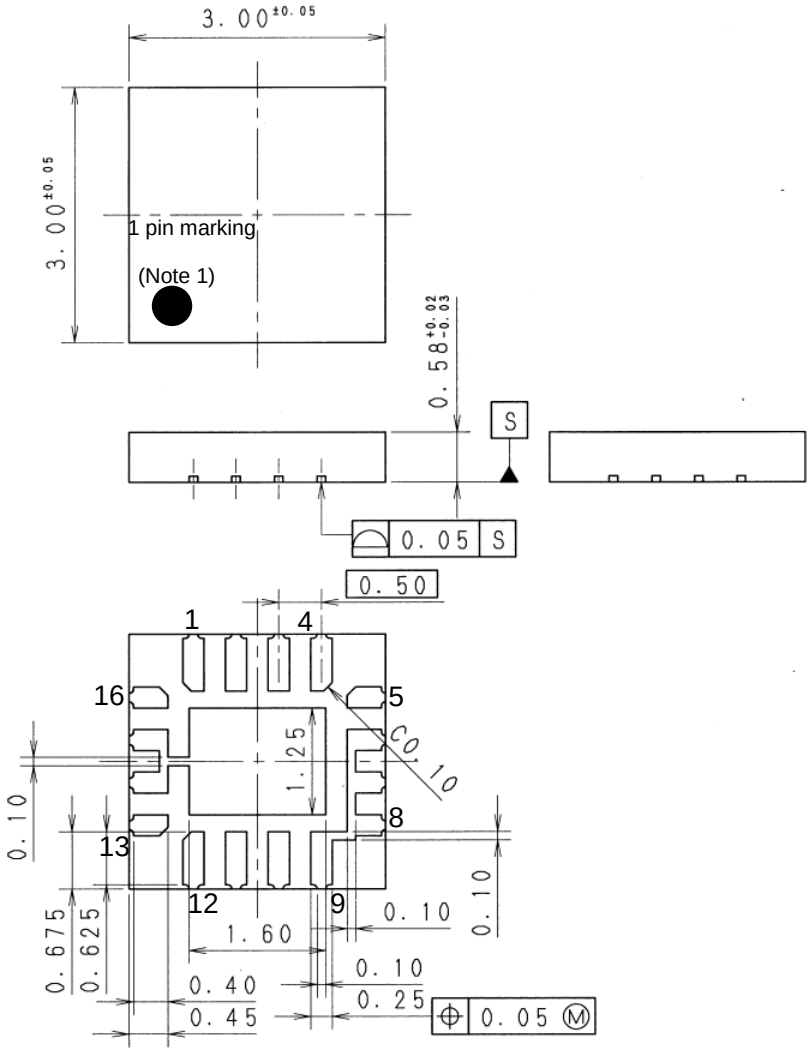


Fig.12 Outer Dimensions

Note 1. 1 pin marking is only a reference for the 1 pin location on the top of package.

14. Marking

(a) Style	:	UQFN
(b) Number of pins	:	16
(c) 1 pin marking:	:	○
(d) Product number	:	1221
(e) Date code	:	YWWL (4 digits)

Y : Lower 1 digit of calendar year (Year 2012 → 2, 2013 → 3 ...)

WW : Week

L : Lot identification, given to each product lot which is made in a week
→ LOT ID is given in alphabetical order (A, B, C…).

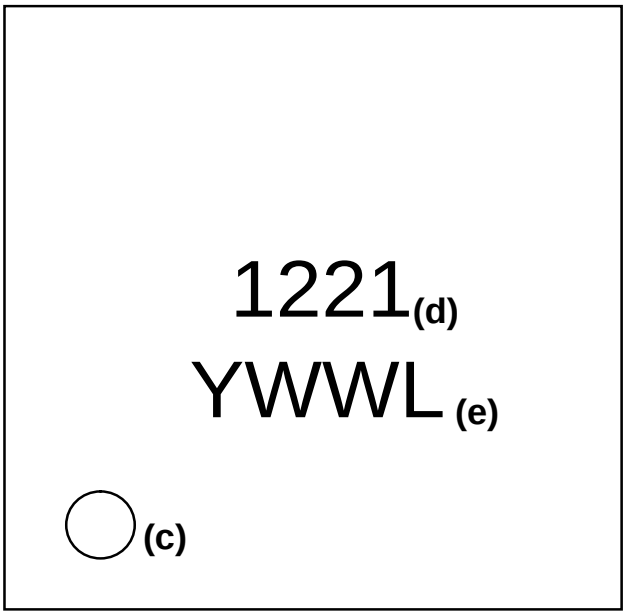


Fig. 13 Marking

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