# AK1222

## 900MHz Low Power Mixer

## 1. Overview

The AK1222 is a low power mixer. RF and LO frequency range coverage from 100 to 900MHz and IF coverage is from 20 to 100MHz. The RF input provides single-ended 50Ω interface. LO ports are 50Ω matched and complementary inputs should be decoupled to the ground. IF output ports are differential open drain outputs.
The linearity and power consumption performances can optimize with the resistance connected to the BIAS pin.

## 2. Features

- ☐ Operating Frequency: 100 to 900MHz
- ☐ Linearity vs Power Selectable architecture
  - Power Consumption:5.3mA, IIP3:+11dBm, Gain:-2dB, NF:12dB
  - Power Consumption:2.9mA, IIP3:+2dBm, Gain:-3.5dB, NF:11.5dB
- ☐ LO input level: 0dBm±5dB
- ☐ Operating Supply Voltage: 4.75 to 5.25 V
- ☐ Package: 16pin UQFN (0.5mm pitch, 3mm x 3mm x 0.60mm)
- ☐ Operating Temperature Range: -40 to 85°C

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## 3. Block Diagram

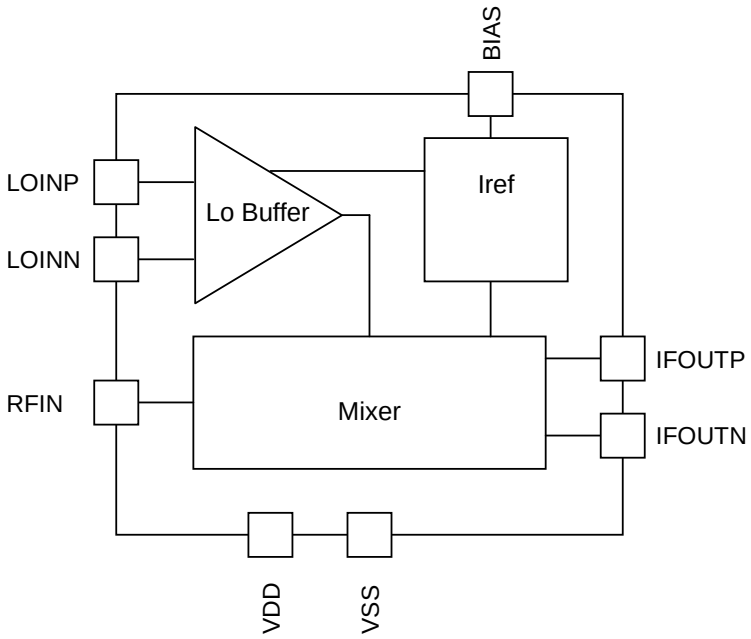



**Fig. 1 Block Diagram**

## 4. System Diagram

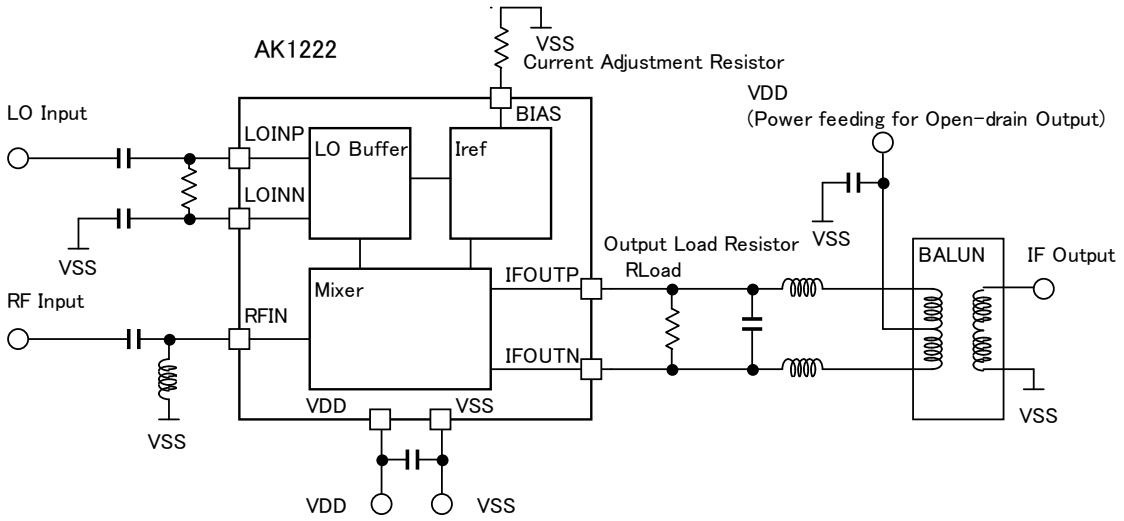



**Fig. 2 System Diagram**

# 5. Pin Functional Description

**Table 1 Pin Function**

| No. | Name | I/O | Pin Functions | Remarks |
|---|---|---|---|---|
| 1 | RFIN | AI | RF Input | Connecting an inductor between this pin and ground. |
| 2 | VSS | G | Ground pin | |
| 3 | LOINN | AI | LO Input Negative | |
| 4 | LOINP | AI | LO Input Positive | |
| 5 | NC | - | Non Connect | |
| 6 | NC | - | Non Connect | |
| 7 | NC | - | Non Connect | |
| 8 | NC | - | Non Connect | |
| 9 | BIAS | AIO | Resistance pin for current adjustment | Connecting a resistor between this pin and ground. |
| 10 | VDD | P | Power Supply | |
| 11 | IFOUTN | AO | IF Output Negative | This pin is open drain output.<br>It needs power feeding via an inductor. |
| 12 | IFOUTP | AO | IF Output Positive | This pin is open drain output.<br>It needs power feeding via an inductor. |
| 13 | NC | - | Non Connect | |
| 14 | NC | - | Non Connect | |
| 15 | NC | - | Non Connect | |
| 16 | NC | - | Non Connect | |

Note) It is recommended to connect NC pins to ground, although it will not make any impact on the electrical characteristics if the pin is open.

| | | |
|---|---|---|
| AI: Analog input pin | AO: Analog output pin | AIO: Analog I/O pin |
| P: Power supply pin | G: Ground pin | |

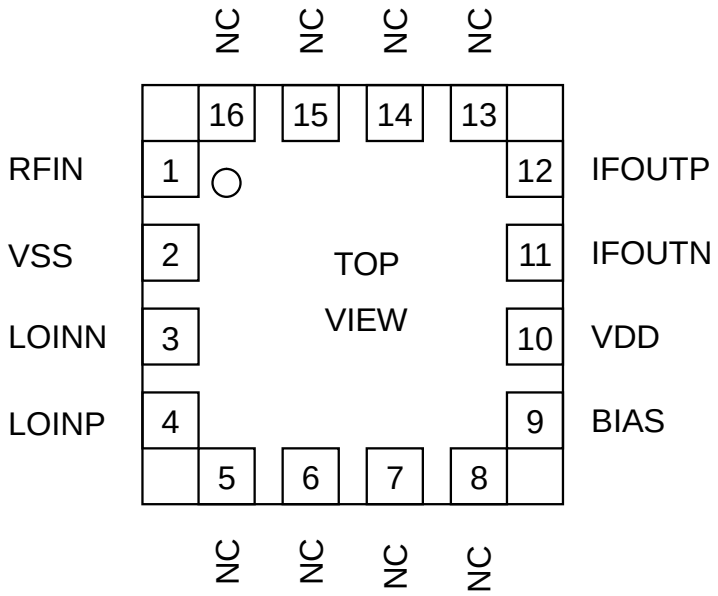



**Fig. 3 Package Pin Layout**

## 6. Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Supply Voltage | VDD | -0.3 | 5.5 | V | |
| RF Input Power | RFPOW | | 7 | dBm | |
| LO Input Power | LOPOW | | 12 | dBm | |
| Storage Temperature | Tstg | -55 | 125 | °C | |

Exceeding these maximum ratings may result in damage to the AK1222. Normal operation is not guaranteed at these extremes.

## 7. Recommended Operating Range

**Table 3 Recommended Operating Range**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Operating Temperature | Ta | -40 | | 85 | °C | |
| Supply Voltage | VDD | 4.75 | 5 | 5.25 | V | |

The specifications are applicable within the recommended operating range (supply voltage/operating temperature).

# 8. Electrical Characteristics

## 1. Analog Circuit Characteristics

Unless otherwise noted IF output=50MHz, LO Input Level=-5dBm to +5dBm,

Output Load Resistor (RLoad)=2.2kΩ, VDD=4.75 to 5.25V, Ta=-40 to 85°C

| Parameter | | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| RF Input Frequency | | 100 | | 900 | MHz | |
| LO Input Frequency | | 100 | | 900 | MHz | |
| IF output Frequency | | 20 | | 100 | MHz | |
| LO Input Power | | -5 | 0 | +5 | dBm | |
| Current Adjustment Resistor(BIAS) | | 22 | | 56 | kΩ | |
| IDD | BIAS=22kΩ | | 5.3 | 7.9 | mA | The total current of VDD pin, IFOUTP pin and IFOUTN pin. |
| | BIAS=56kΩ | | 2.9 | 4.7 | mA | |
| **RFIN=600MHz, Output Load Resistor = 22kΩ** | | | | | | |
| Conversion Gain | | -4 | -2 | 0 | dB | |
| SSB Noise Figure (NF) | | | 12 | 14 | dB | Design guarantee value |
| IP1dB | | -3 | 0 | | dBm | |
| IIP3 | | +8 | +11 | | dBm | |
| **RFIN=600MHz, Output Load Resistor = 56kΩ** | | | | | | |
| Conversion Gain | | -5.5 | -3.5 | -1.5 | dB | |
| SSB Noise Figure (NF) | | | 11.5 | 13.5 | dB | Design guarantee value |
| IP1dB | | -9 | -6 | | dBm | |
| IIP3 | | -1 | +2 | | dBm | |

Note 1) In the shipment test, NC pins and the exposed pad on the center of the back of the package is connected to ground.

# 9. Typical Performance

Unless otherwise noted, RF input =600MHz, LO input =550MHz, IF output =50MHz, Output Load Resistor (RLoad)=2.2kΩ

## 1. Current Adjustment Resistor vs. IIP3, NF, IP1dB, Gain, IDD

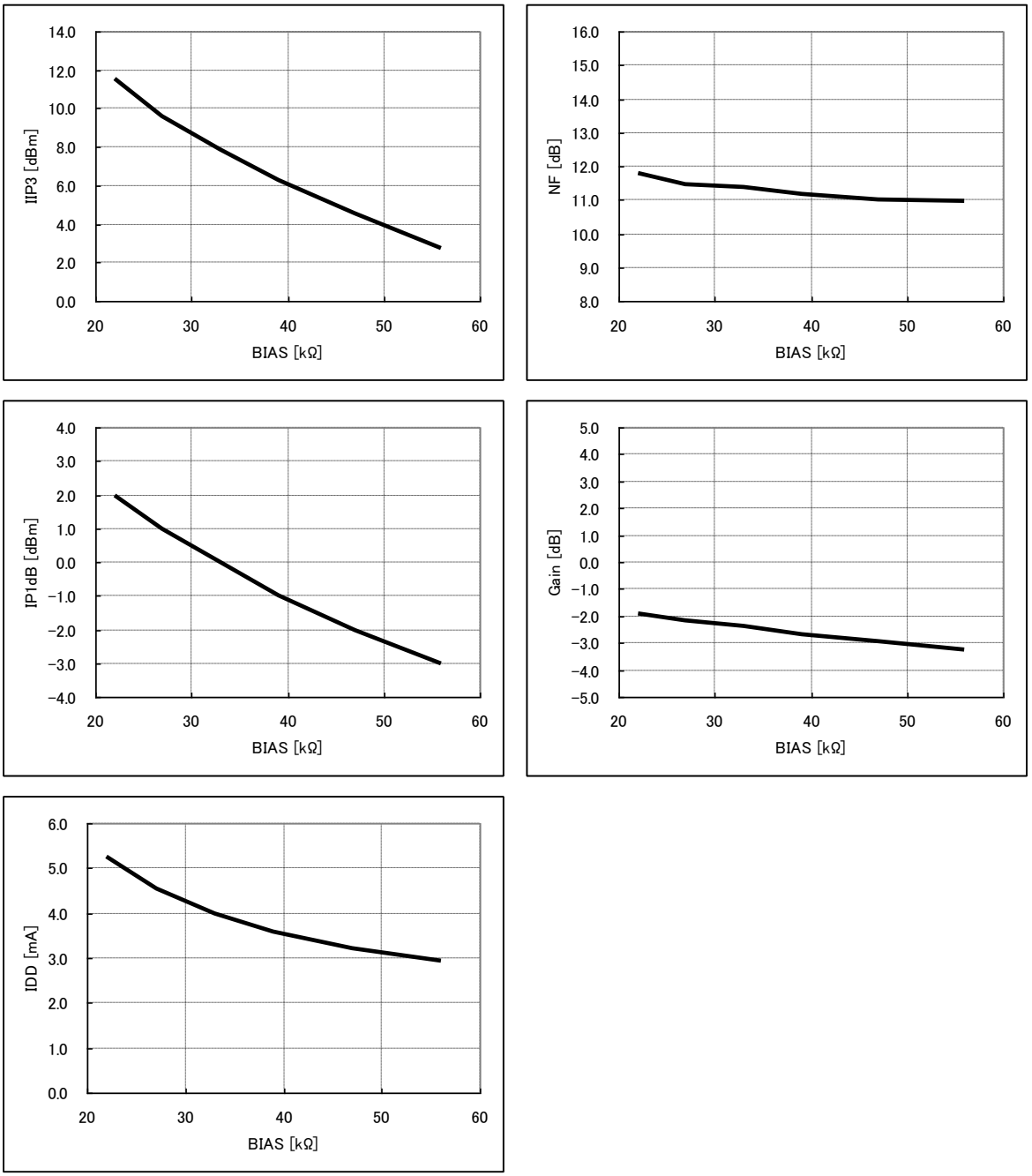



**Fig. 4 Current Adjustment Resistor vs. IIP3, NF, IP1dB, Gain, IDD**

Note 1) A resistor with 5% tolerance are used.

## 2. Over temperature vs. IIP3, NF, IP1dB, Gain, IDD

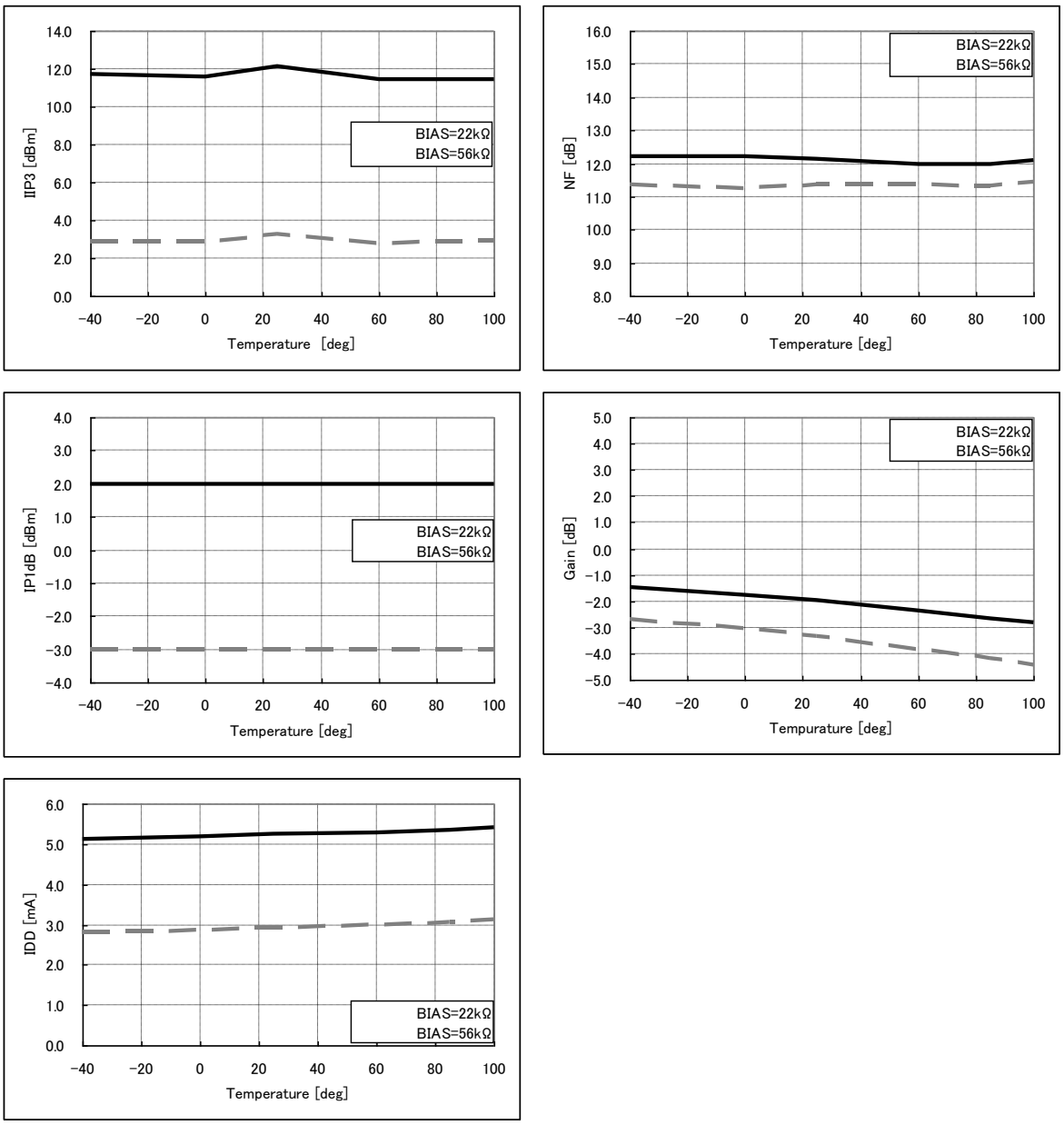



**Fig. 5 Over temperature vs. IIP3, NF, IP1dB, Gain, IDD**

### 3. Supply voltage vs. IIP3, NF, IP1dB, Gain, IDD

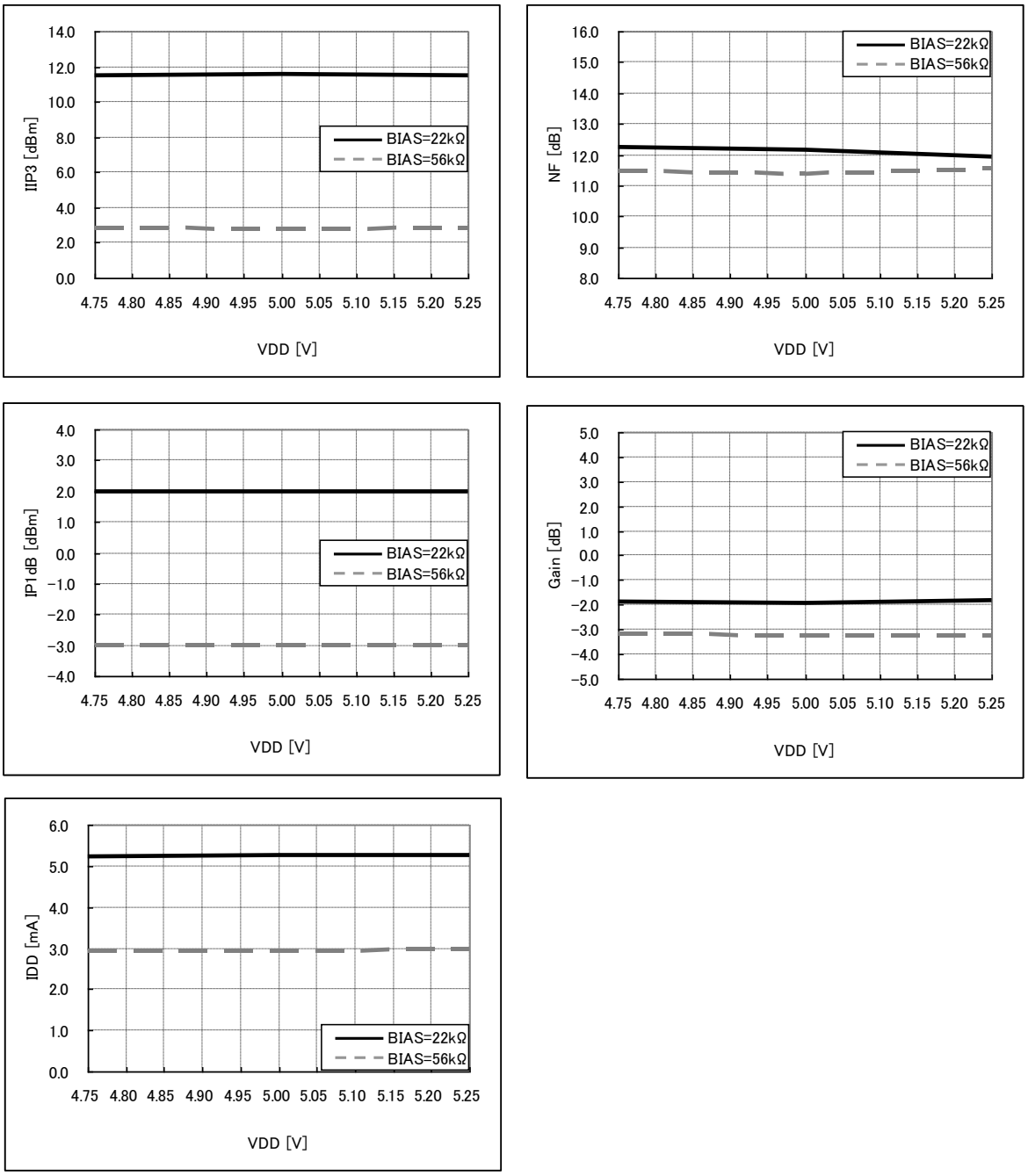



**Fig. 6 Supply voltage vs. IIP3, NF, IP1dB, Gain, IDD**

### 4. RF input frequency vs. IIP3, NF, IP1dB, Gain

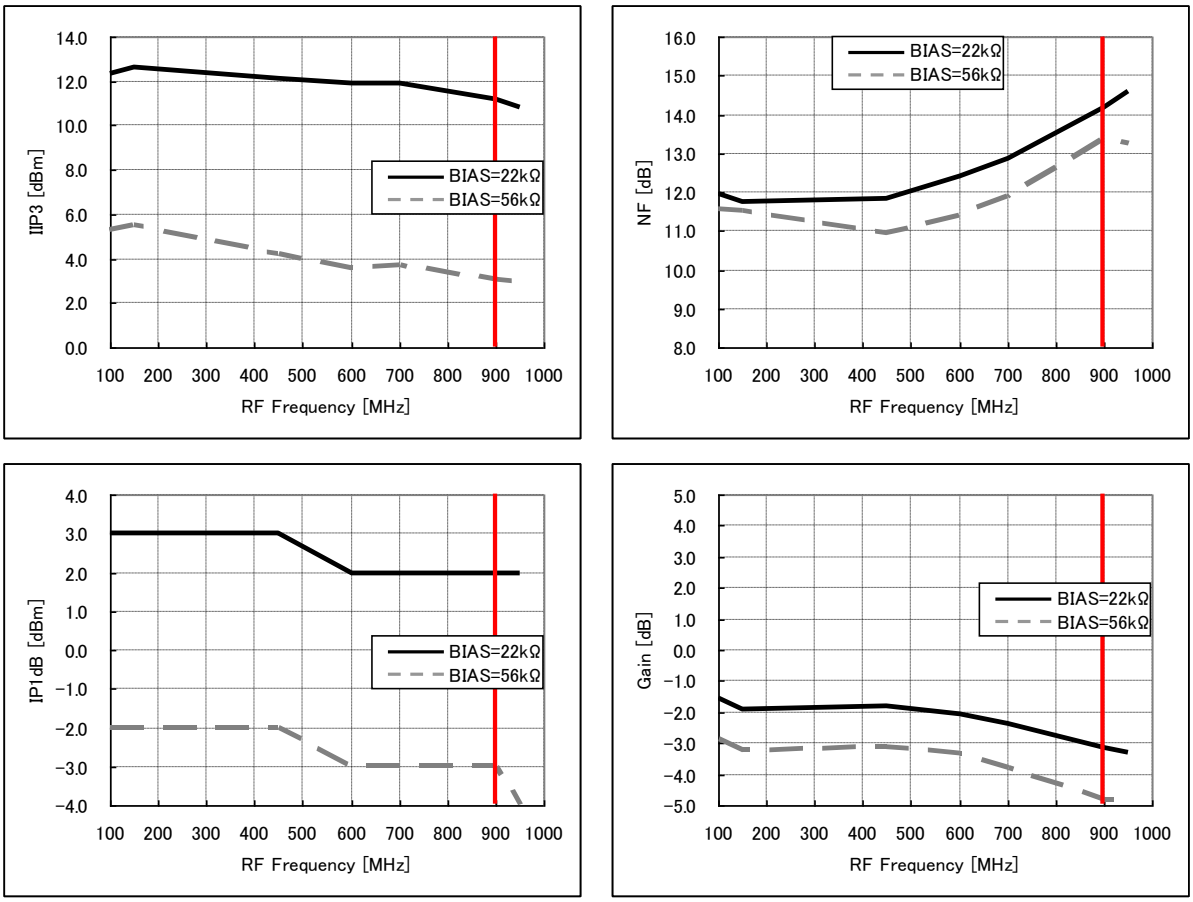



**Fig. 7 RF input frequency vs. IIP3, NF, IP1dB, Gain**

Note 1) AK1222 supports 100MHz to 900MHz RF Input.

**5. IF output frequency vs. IIP3, NF, IP1dB, Gain**

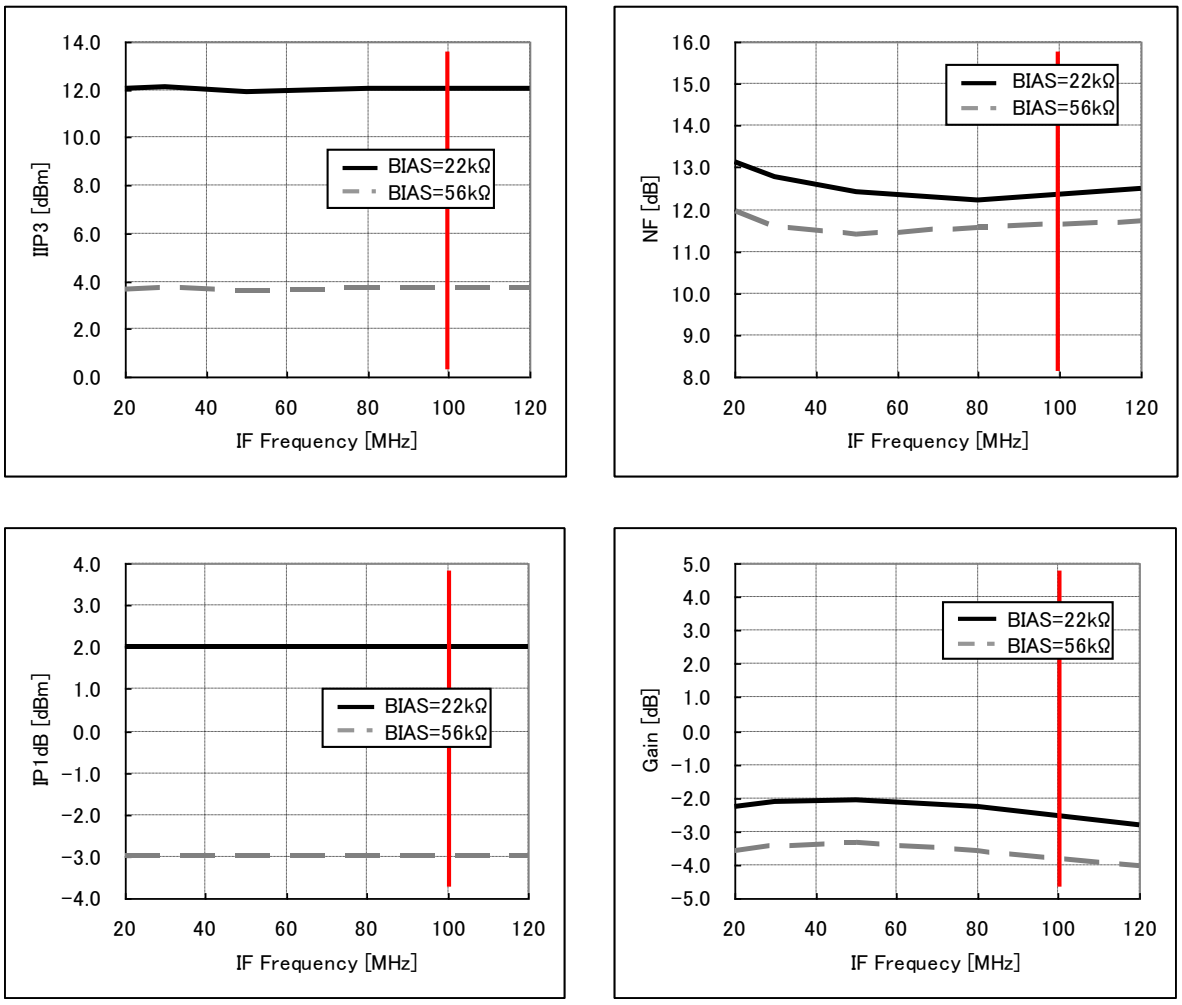



**Fig. 8 IF output frequency vs. IIP3, NF, IP1dB, Gain**

Note 1) AK1222 supports 20MHz to 100MHz IF Output.

**6. LO input power vs. IIP3, NF, IP1dB, Gain**

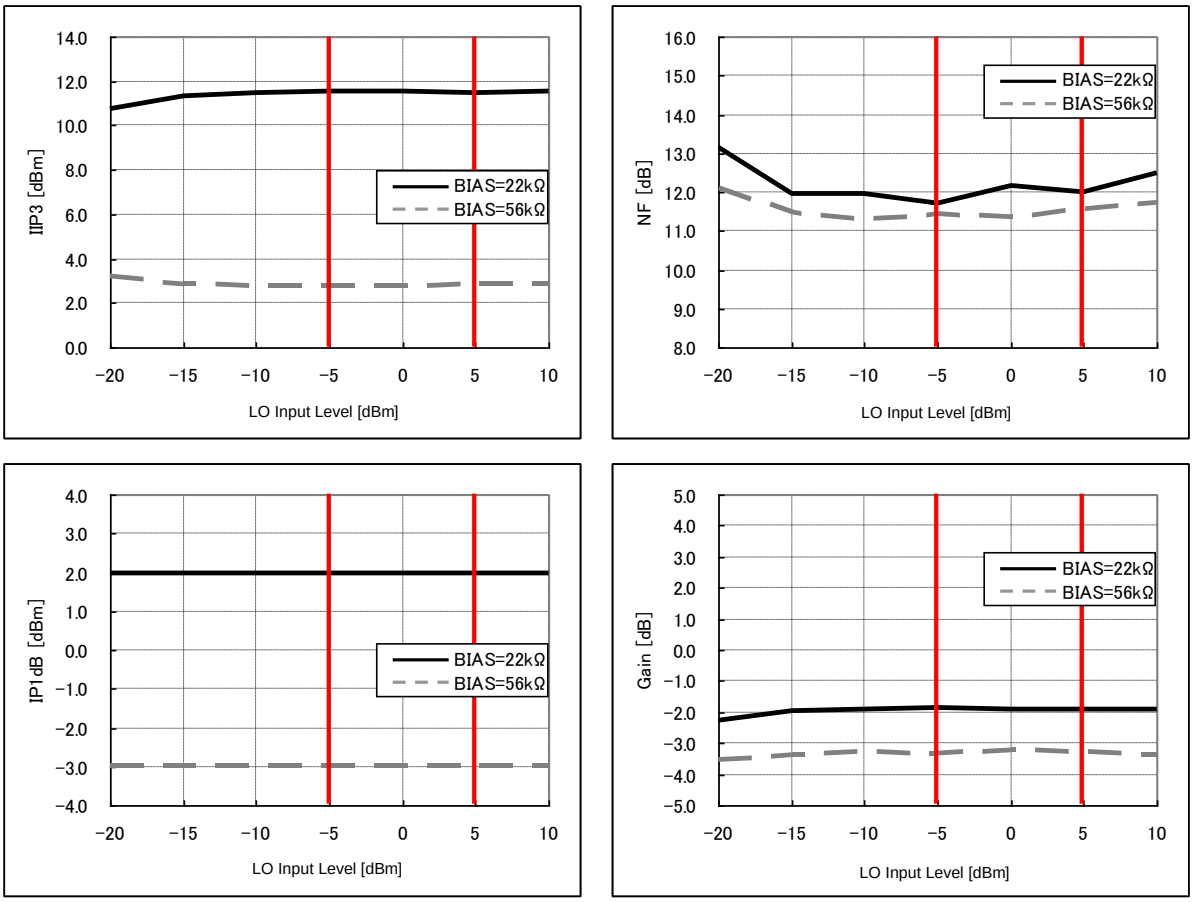



**Fig. 9 LO input power vs. IIP3, NF, IP1dB, Gain**

Note 1) AK1222 supports -5dBm to 5dBm LO input power.

### 7. Output Load Resistor (RLoad) vs. IIP3, NF, IP1dB, Gain

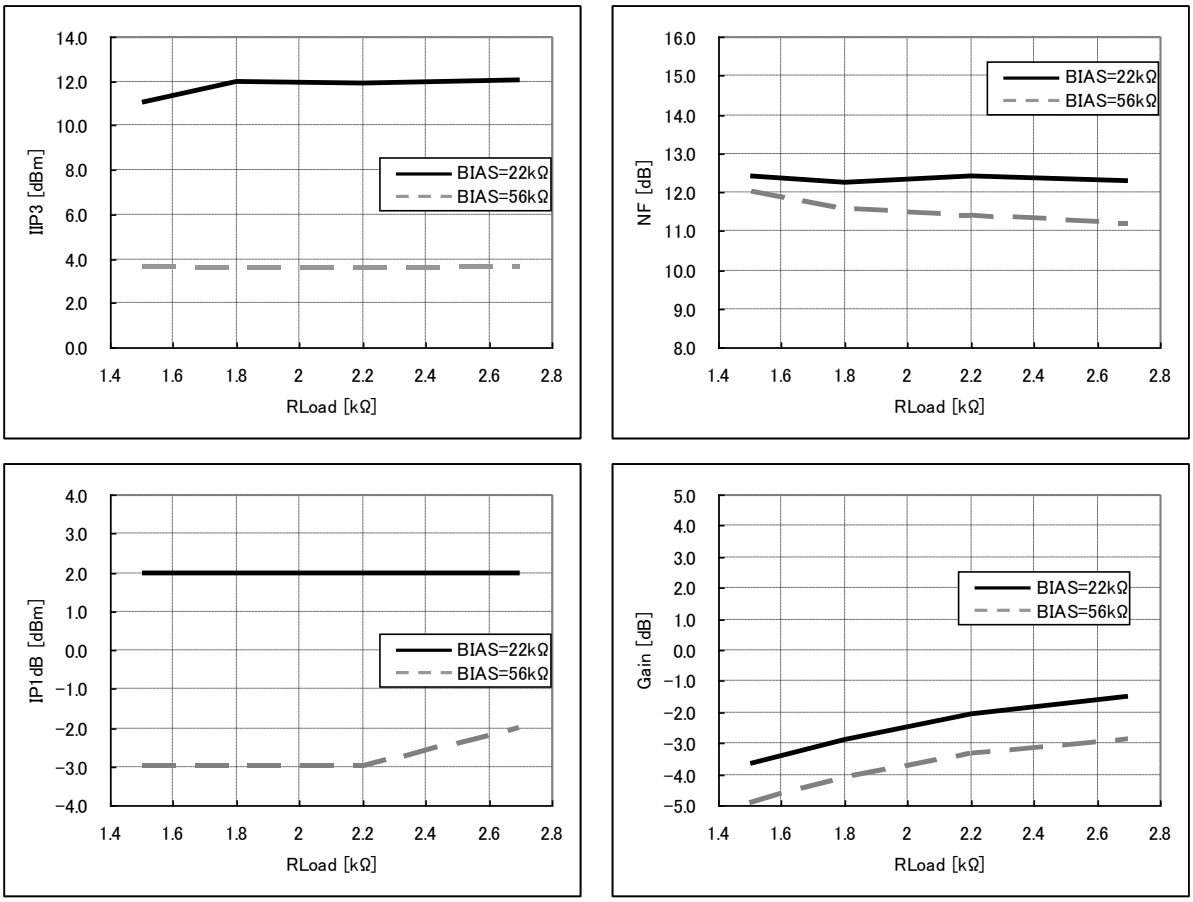



**Fig. 10 Output Load Resistor（RLoad）vs. IIP3, NF, IP1dB, Gain**

### 8. Leakage

RF input=600MHz, -20dBm, LO input=600MHz, 0dBm, Ta=25°C VDD=5V

| Parameter | BIAS | Typ. | Unit |
|---|---|---|---|
| RF – LO Leakage | 22kΩ | -50 | dBc |
| | 56kΩ | -50 | dBc |
| RF – IF Leakage | 22kΩ | -80 | dBc |
| | 56kΩ | -80 | dBc |
| LO – RF Leakage | 22kΩ | -50 | dBc |
| | 56kΩ | -50 | dBc |
| LO – IF Leakage | 22kΩ | -80 | dBc |
| | 56kΩ | -80 | dBc |

# 10. Typical Evaluation Board Schematic

## 1. Typical Evaluation Board Schematic

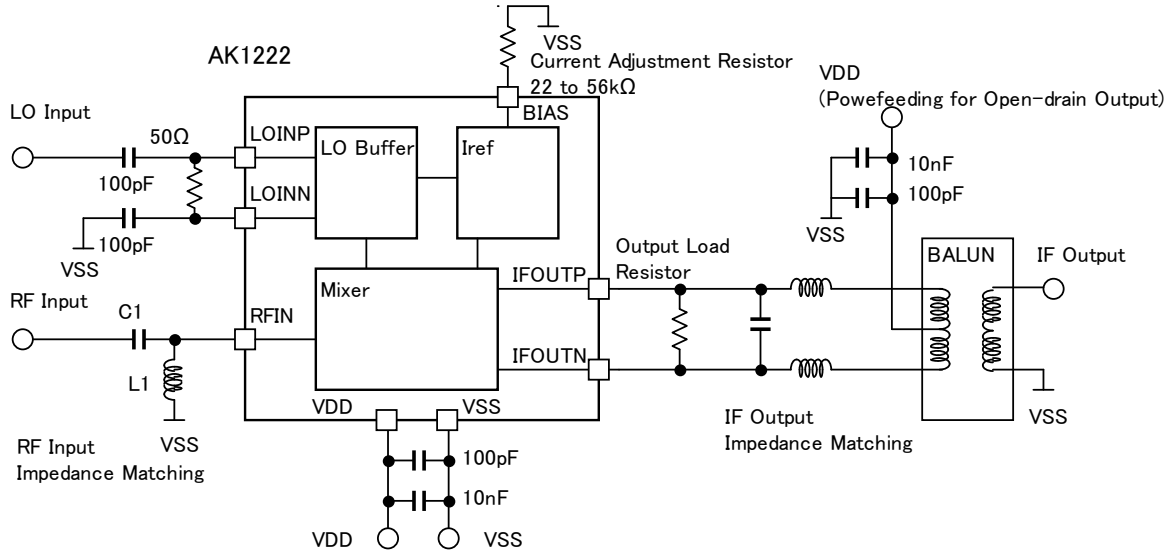


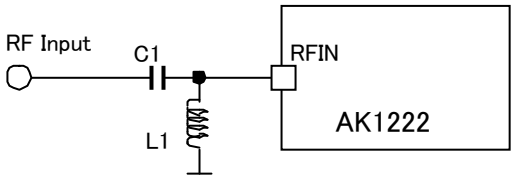

**Fig. 11 Typical Evaluation Board Schematic**

Note 1) The open drain output needs power feeding via a inductor. (IFOUTP pin and IFOUTN)

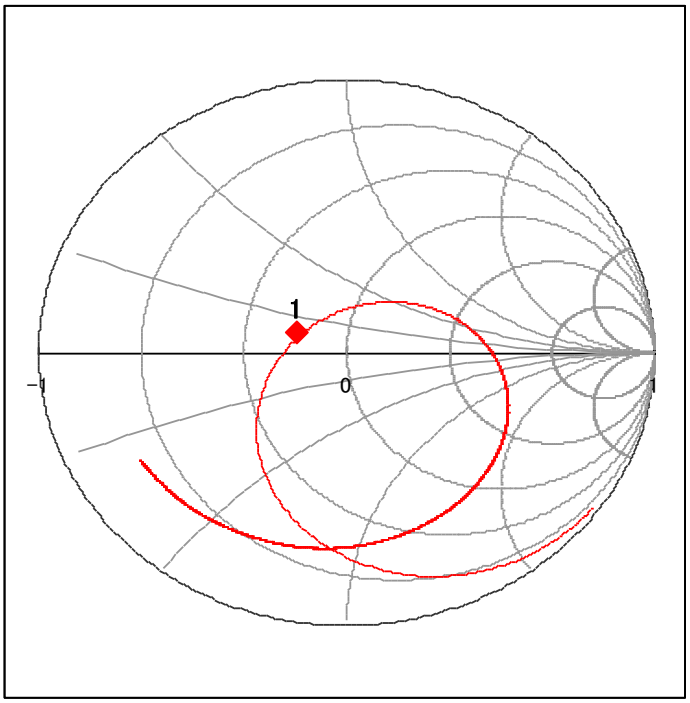
Note 2) It is necessary to adjust impedance matching as to its setting frequency. (RF input and IF output)

## 2. Example of impedance matching

**・RFIN**




| Frequency[MHz] | C1[pF] | L1[nH] |
|---|---|---|
| 150 | 15 | 82 |
| 450 | 5.1 | 22 |
| 600 | 3.6 | 15 |
| 900 | 3.9 | 6.8 |



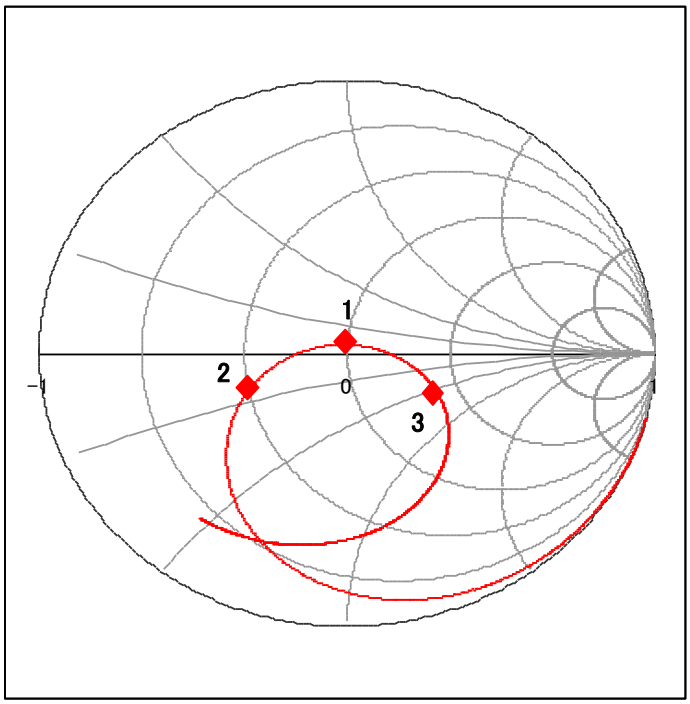

| Frequency[MHz] | C1[pF] | L1[nH] |
|---|---|---|
| 150 | 15 | 82 |

Start 50MHz, Stop 1GHz

Marker 1

150MHz: 36.1Ω　4.2Ω

**Fig. 12 RFIN 150MHz example of impedance matching**

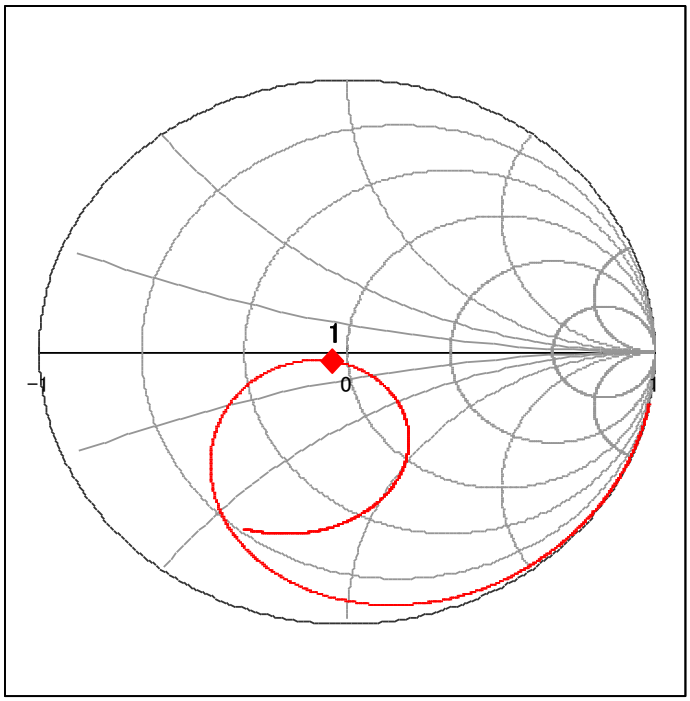



| Frequency[MHz] | C1[pF] | L1[nH] |
|---|---|---|
| 450 | 5.1 | 22 |

Start 50MHz, Stop 1GHz

Marker 1
450MHz: 51.1Ω 3.3Ω
Marker 2
394MHz: 25.1Ω -7.6Ω
Marker 3
524MHz: 85.6Ω -30.1Ω

**Fig. 13 RFIN 450MHz example of impedance matching**

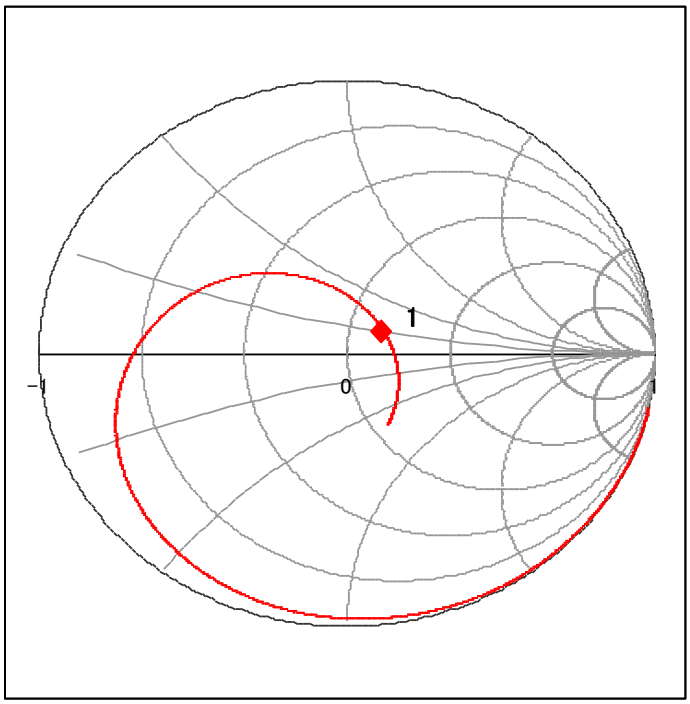



| Frequency[MHz] | C1[pF] | L1[nH] |
|---|---|---|
| 600 | 3.6 | 15 |

Start 50MHz, Stop 1GHz

Marker 1
600MHz: 46.2Ω -3.3Ω

**Fig. 14 RFIN 600MHz example of impedance matching**




| Frequency[MHz] | C1[pF] | L1[nH] |
|---|---|---|
| 900 | 3.9 | 6.8 |

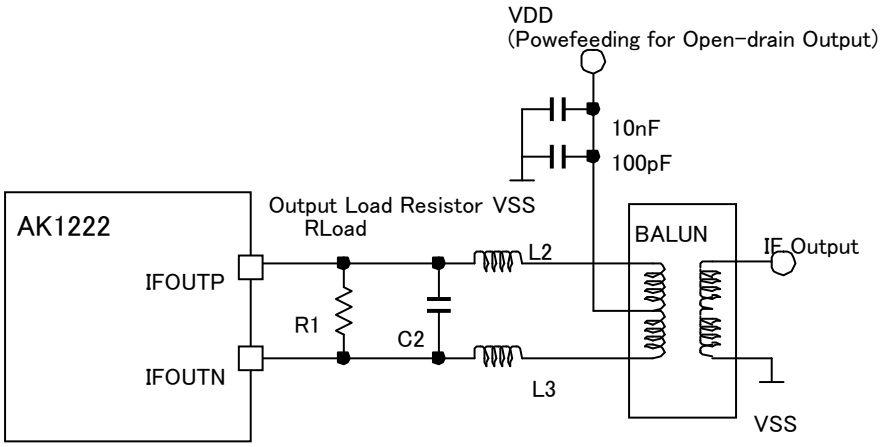
Start 50MHz, Stop 1GHz

Marker 1

900MHz: 61.8Ω 11.0Ω

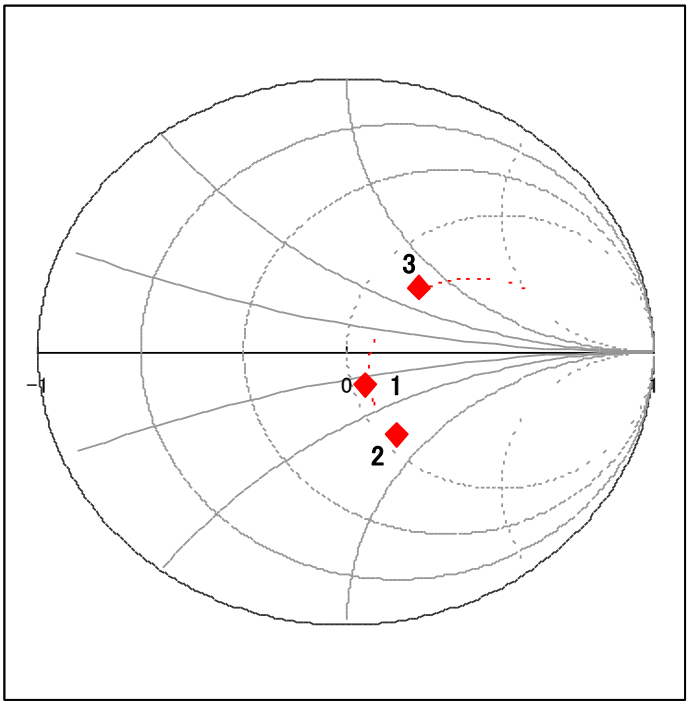
**Fig. 15 RFIN 900MHz example of impedance matching**

**・IFOUT**




| Frequency [MHz] | R1 [kΩ] | C2 [pF] | L2 [nH] | L3 [nH] |
|---|---|---|---|---|
| 30 | 2.2 | 3.9 | 1800 | 1800 |
| 50 | 2.2 | 2.0 | 1000 | 1000 |
| 60 | 2.2 | 0.5 | 1000 | 1000 |
| 80 | 2.2 | N/A | 680 | 680 |
| 100 | 2.2 | N/A | 470 | 470 |

1800nH : Murata LQW21HN1R8J00L
1000nH : Murata LQW21HN1R0J00L
680nH : Murata LQW21HNR68J00L
470nH : Murata LQW21HNR47J00L
BALUN:Mini-Circuits ADT4-6T+

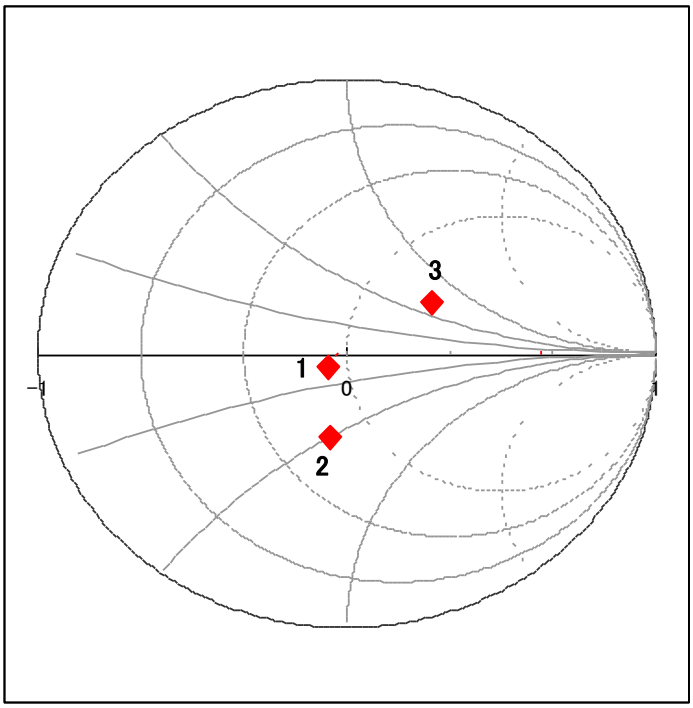



| Frequency [MHz] | R1 [kΩ] | C2 [pF] | L2 [nH] | L3 [nH] |
|---|---|---|---|---|
| 30 | 2.2 | 3.9 | 1800 | 1800 |

Start 10MHz, Stop 140MHz

Marker 1
30MHz: 55.5Ω -19.7Ω
Marker 2
28MHz: 55.7Ω -37.3Ω
Marker 3
36MHz: 72.8Ω 38.4Ω

**Fig. 16 IFOUT 30MHz example of impedance matching**

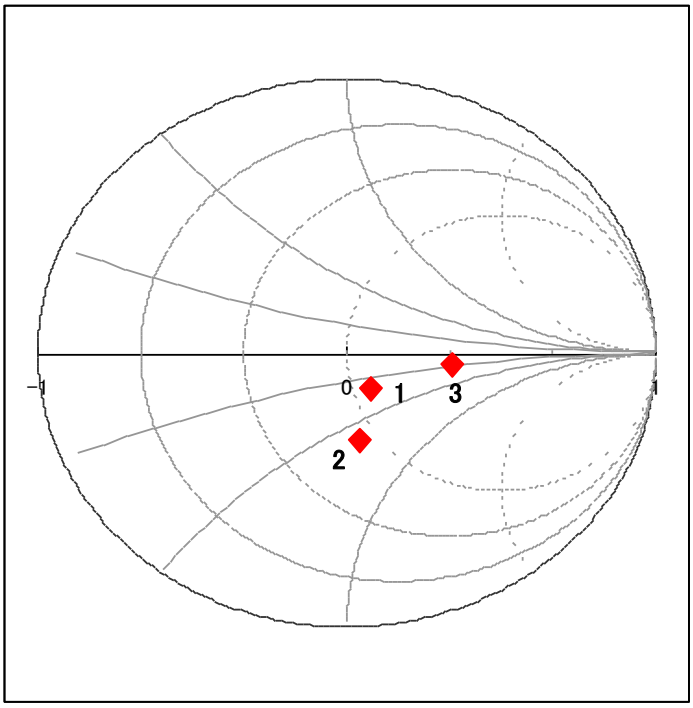



| Frequency [MHz] | R1 [kΩ] | C2 [pF] | L2 [nH] | L3 [nH] |
|---|---|---|---|---|
| 50 | 2.2 | 2 | 1000 | 1000 |

Start 10MHz, Stop 140MHz

Marker 1
50MHz: 43.2Ω -7.5Ω
Marker 2
45MHz: 37.3Ω -28.6Ω
Marker 3
59MHz: 81.6Ω 34.6Ω

**Fig. 17 IFOUT 50MHz example of impedance matching**

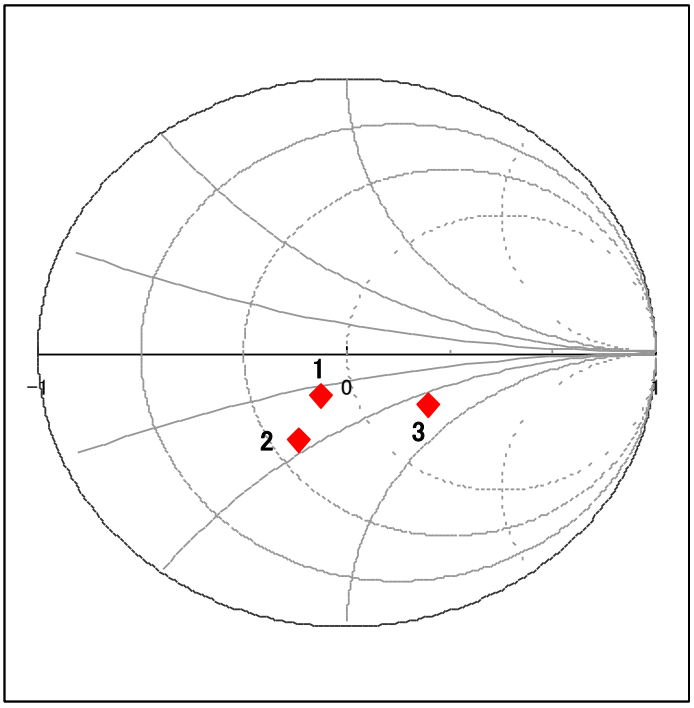



| Frequency [MHz] | R1 [kΩ] | C2 [pF] | L2 [nH] | L3 [nH] |
|---|---|---|---|---|
| 60 | 2.2 | 0.5 | 1000 | 1000 |

Start 10MHz, Stop 140MHz

Marker 1
60MHz: 52.7Ω -19.0Ω
Marker 2
54MHz: 43.4Ω -33.1Ω
Marker 3
70MHz: 100.7Ω -8.4Ω

**Fig. 18 IFOUT 60MHz example of impedance matching**

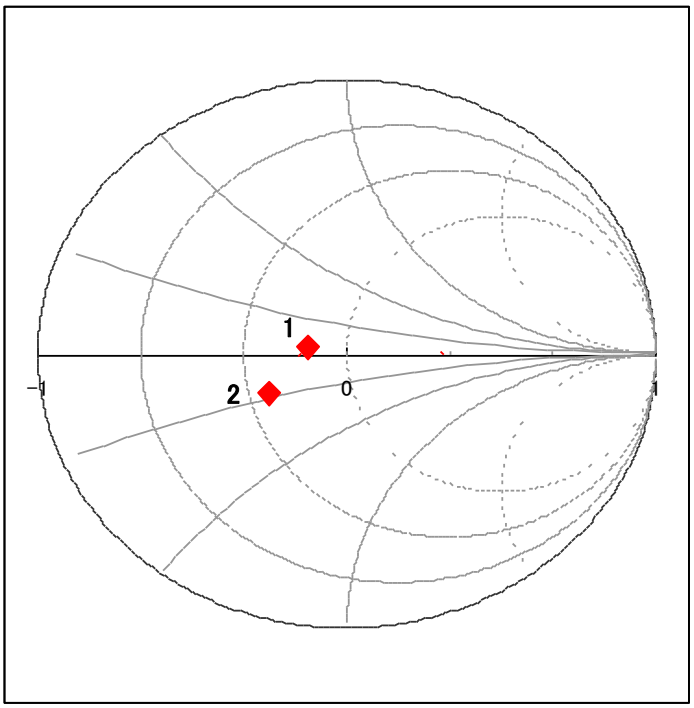



| Frequency [MHz] | R1 [kΩ] | C2 [pF] | L2 [nH] | L3 [nH] |
|---|---|---|---|---|
| 80 | 2.2 | N/A | 680 | 680 |

Start 10MHz, Stop 140MHz

Marker 1
80MHz: 38.5Ω -14.5Ω
Marker 2
75MHz: 31.2Ω -21.3Ω
Marker 3
95MHz: 78.7Ω -33.8Ω

**Fig. 19 IFOUT 80MHz example of impedance matching**




| Frequency [MHz] | R1 [kΩ] | C2 [pF] | L2 [nH] | L3 [nH] |
|---|---|---|---|---|
| 100 | 2.2 | N/A | 470 | 470 |

Start 10MHz, Stop 140MHz

Marker 1
100MHz: 38.9Ω 1.6Ω
Marker 2
90MHz: 26.9Ω -12.2Ω

**Fig. 20 IFOUT 100MHz example of impedance matching**

**・LOINP/LOINN**

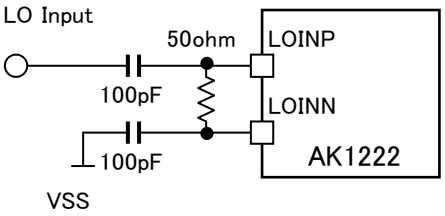
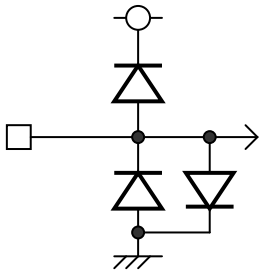
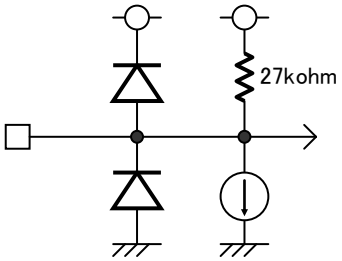
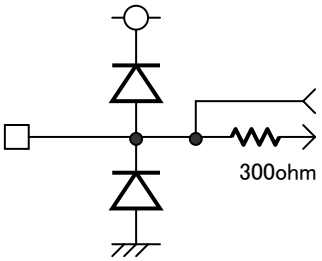
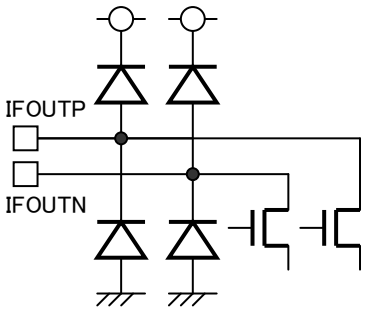



**Fig. 21 LOINP/LOINN example of impedance matching**

## 11. IC Interface Schematic

| No. | Name | I/O | Function |
|---|---|---|---|
| 1 | RFIN | I | **RF input pin**  |
| 3 | LOINN | I | **LO input pins** |
| 4 | LOINP | I |   |
| 9 | BIAS | I/O | **Analog I/O pin**   |
| 11 | IFOUTN | O | **IF output pins** |
| 12 | IFOUTP | O |   |

## 12. Outer Dimensions

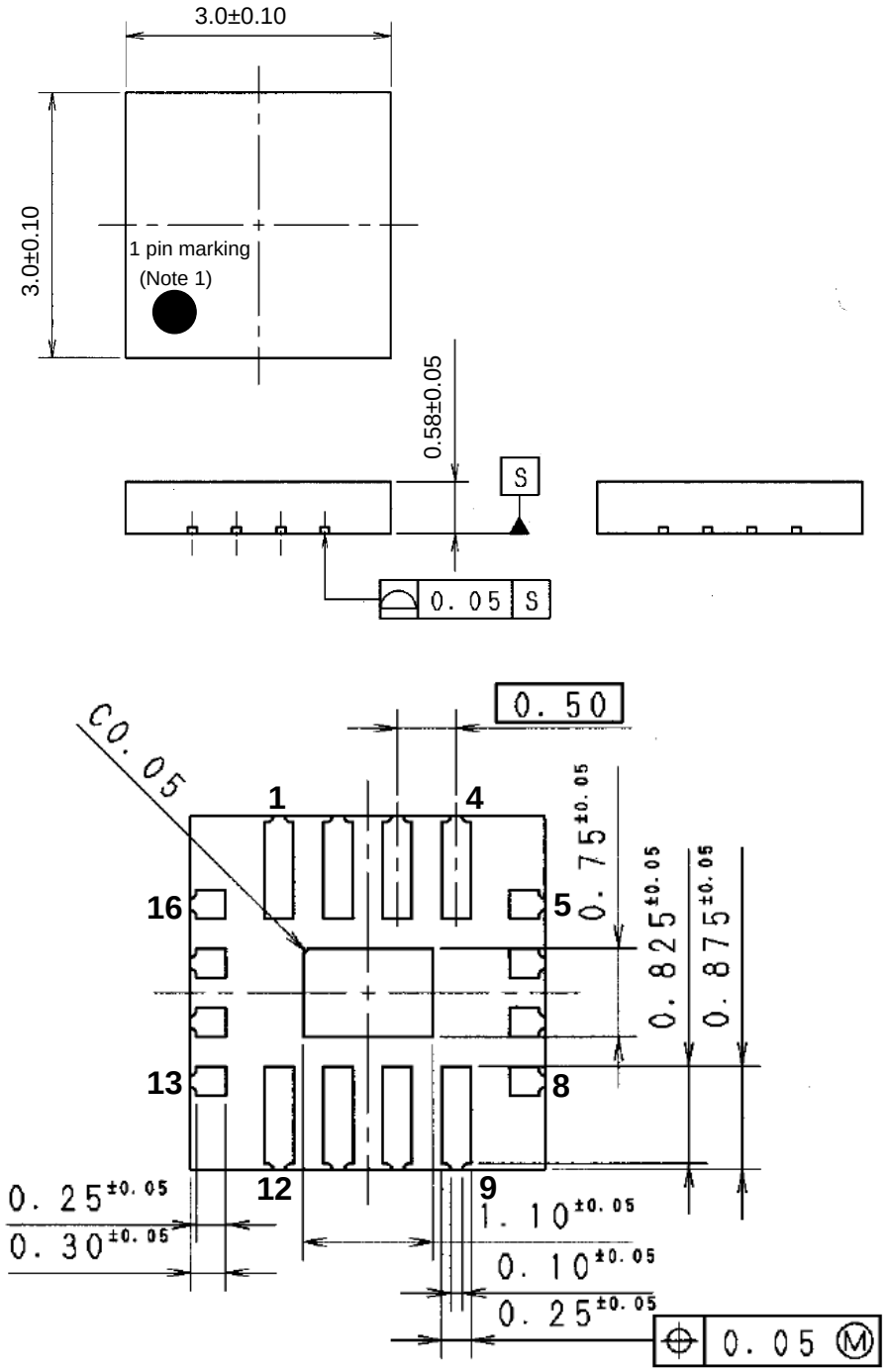



**Fig. 22 Outer Dimensions**

Note 1. 1 pin marking is only a reference for the 1 pin location on the top of package.

## 13. Marking

(a) Style : QFN

(b) Number of pins : 16

(c) 1 pin marking: : ○

(d) Product number : 1222

(e) Date code : YWWL (4 digits)

Y: Lower 1 digit of calendar year (Year 2011 → 1, 2012 → 2 ...)

WW: Week

Lot identification, given to each product lot which is made in a week

→ LOT ID is given in alphabetical order (A, B, C…).

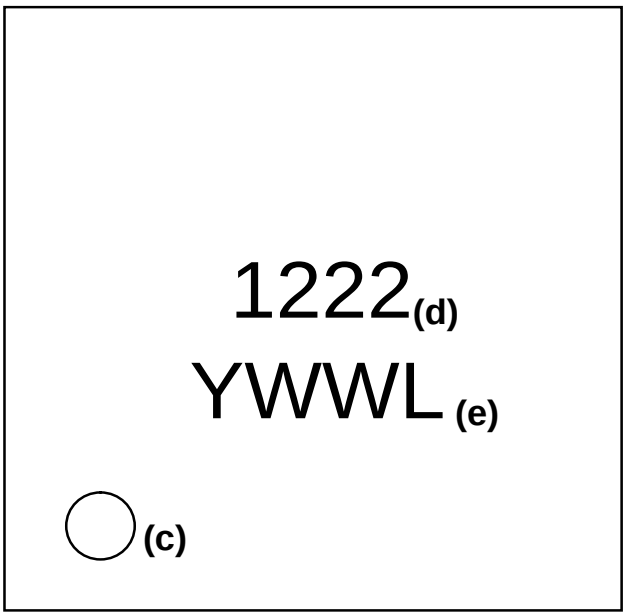



**Fig. 23 Marking**

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