AsahiKASEI
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# AK1224

**900MHz Low Noise Mixer**

## 1. Overview

The AK1224 is a high linearity and low noise mixer. RF frequency range coverage is from 100 to 900MHz and IF coverage is from 20 to 100MHz. AK1224 can be driven by a single ended RF input and a low-power differential LO input that can be driven with a differential or single ended LO signal. IF output ports are differential open drain outputs. The analog circuit characteristics and power consumption performances can be optimized by the resistance connected to the BIAS Pin.

## 2. Feature

- ☐ Operating Frequency: 100MHz to 900MHz
- ☐ Linearity vs. Power selectable architecture:
  Current consumption:21mA, IIP3:+16dBm, Gain:5.5dB, NF:8.5dB
- ☐ Lo input level: 0dBm ±5dB
- ☐ Operating Supply Voltage: 4.75 to 5.25 V
- ☐ Package: 16pin UQFN（0.5mm pitch、3mm × 3mm × 0.60mm）
- ☐ Operating Temperature Range -40 to 85°C

# 3. Table contents

## 4. Block Diagram

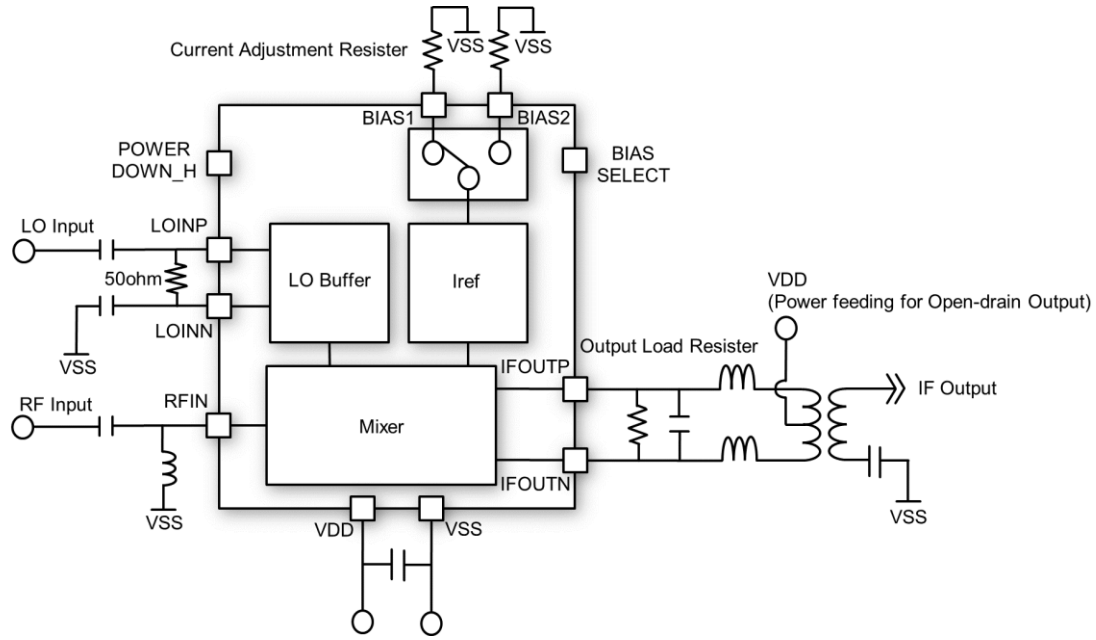



**Fig. 1 Block Diagram**

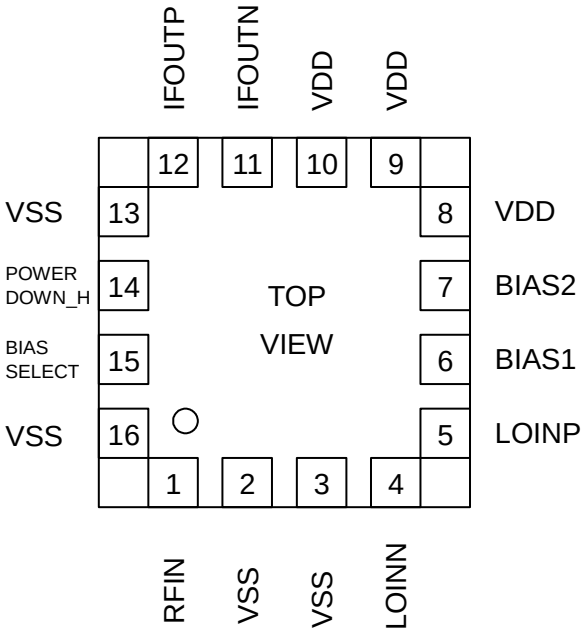



**Fig. 2 Package Pin Layout**

## 5. Pin Function Description

**Table 1 Pin Function**

| No. | Name | I/O | Pin Function | Remarks |
|---|---|---|---|---|
| 1 | RFIN | AI | RF Input | Connecting a inductor between this pin and ground. |
| 2 | VSS | G | Ground pin | |
| 3 | VSS | G | Ground pin | |
| 4 | LOINN | AI | Lo Input Negative | |
| 5 | LOINP | AI | Lo Input Positive | |
| 6 | BIAS1 | AIO | Resistance pin for current adjustment | Connecting a resistor between this pin and ground. |
| 7 | BIAS2 | AIO | Resistance pin for current adjustment | Connecting a resistor between this pin and ground. |
| 8 | VDD | P | Power Supply | VDD |
| 9 | VDD | P | Power Supply | VDD |
| 10 | VDD | P | Power Supply | VDD |
| 11 | IFOUTN | AO | IF Output Negative | This pin is open drain output.<br>It needs power feeding via an inductor. |
| 12 | IFOUTP | AO | IF Output Positive | This pin is open drain output.<br>It needs power feeding via an inductor. |
| 13 | VSS | G | Ground pin | |
| 14 | POWER DOWN_H | DI | Power Down control pin | High: Power OFF<br>Low: Power ON |
| 15 | BIAS SELECT | DI | Bias Resistance select pin | High: Bias2 pin is enable<br>Low: Bias1pin is enable |
| 16 | VSS | G | Ground pin | |

Note) The exposed pad at the center of the backside should be connected to ground.

| | | |
|---|---|---|
| AI:Analog input pin | AO:Analog output pin | AIO:Analog I/O pin |
| P: Power supply pin | G: Ground pin | DI:Digital input pin |

## 6. Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Supply Voltage | VDD | -0.3 | 5.5 | V | |
| RF Input Power | RFPOW | | 12 | dBm | |
| LO Input Power | LOPOW | | 12 | dBm | |
| Storage Temperature | Tstg | -55 | 125 | °C | |

Exceeding these maximum ratings may result in damage to the AK1224. Normal operation is not guaranteed at these extremes.

## 1. Recommended Operating Range

**Table 3 Recommended Operating Range**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Operating Temperature | Ta | -40 | | 85 | °C | |
| Supply Voltage | VDD | 4.75 | 5 | 5.25 | V | |

The specifications are applicable within the recommended operating range (supply voltage/operating temperature).

# 7. Electrical Characteristics

## 1. Analog Circuit Characteristics

Unless otherwise noted IF output=50MHz, Lo Input Level=-5dBm to +5dBm,
Output Load Resistor（RLoad）=2.2kΩ, VDD=4.75 to 5.25V, Ta=-40°C to 85°C

| Parameter | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| RF Input Frequency | 100 | | 900 | MHz | |
| Lo Input Frequency | 100 | | 900 | MHz | |
| IF output Frequency | 20 | | 100 | MHz | |
| Lo Input Power | -5 | 0 | +5 | dBm | |
| Current Adjustment Resistor(BIAS) | 22 | | 100 | kΩ | |
| IDD (BIAS=22kΩ) | 20 | 26 | 36 | mA | The total current of VDD pin, IFOUTP pin and IFOUTN pin. |
| IDD (BIAS=27kΩ) | 16 | 21 | 30 | mA | |
| IDD (BIAS =100kΩ) | 4.5 | 6 | 8.5 | mA | |
| IDD (POWERDOWN_H=VDD) | | 1 | 10 | uA | |
| **RFIN=600MHz, Current Adjustment Resistor=27kΩ** | | | | | |
| Conversion Gain | 3.5 | 5.5 | 7.5 | dB | |
| SSB Noise Figure | | 8.5 | 11 | dB | Design guarantee value |
| IP1dB | -3 | 0 | | dBm | |
| IIP3 | 13 | 16 | | dBm | |

## 2. Digital Circuit Characteristics

This table is for **POWER DOWN_H** pin and **BIAS SELECT** pin.

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| High level input voltage | Vih | | 0.8×VDD | | | V | |
| Low level input voltage | Vil | | | | 0.2×VDD | V | |
| High level input current | Iih | Vih = VDD=5.25V | -1 | | 1 | μA | |
| Low level input current | Iil | Vil = 0V, VDD1=5.25V | -1 | | 1 | μA | |

## 8. Typical Performance

Unless otherwise noted, RF input =600MHz, Lo input =550MHz, IF output =50MHz,
Output Load Resistor (RLoad)=2.2kΩ

### 1. Current Adjustment Resistor vs. IIP, NF, P1dB, Gain, IDD

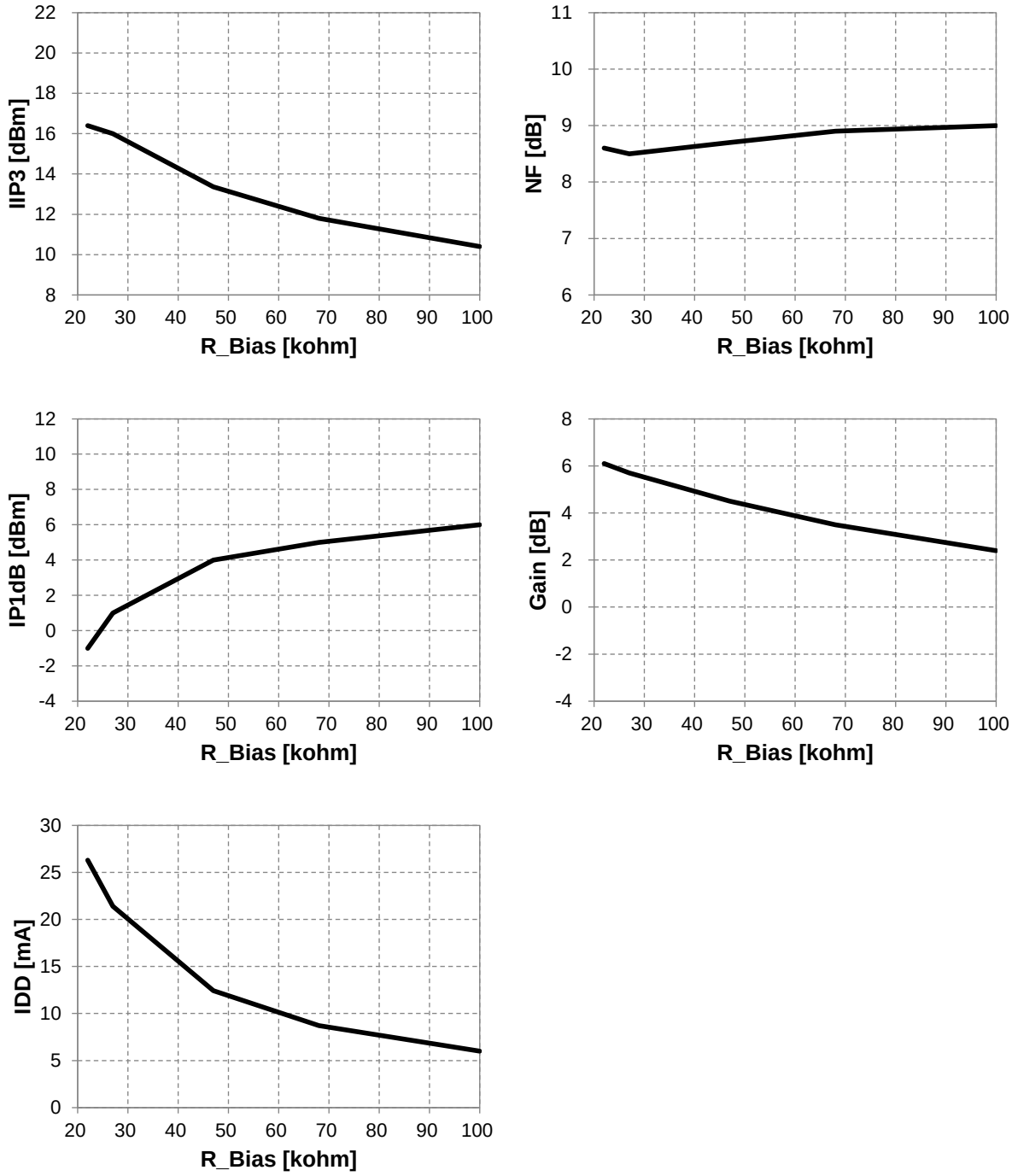



**Fig. 3 Current Adjustment Resistor vs. IIP3, NF, P1dB, Gain, IDD**

Note ) A resistor with 5% tolerance are used.

## 2. Over temperature vs. IIP3, NF, P1dB, Gain, IDD

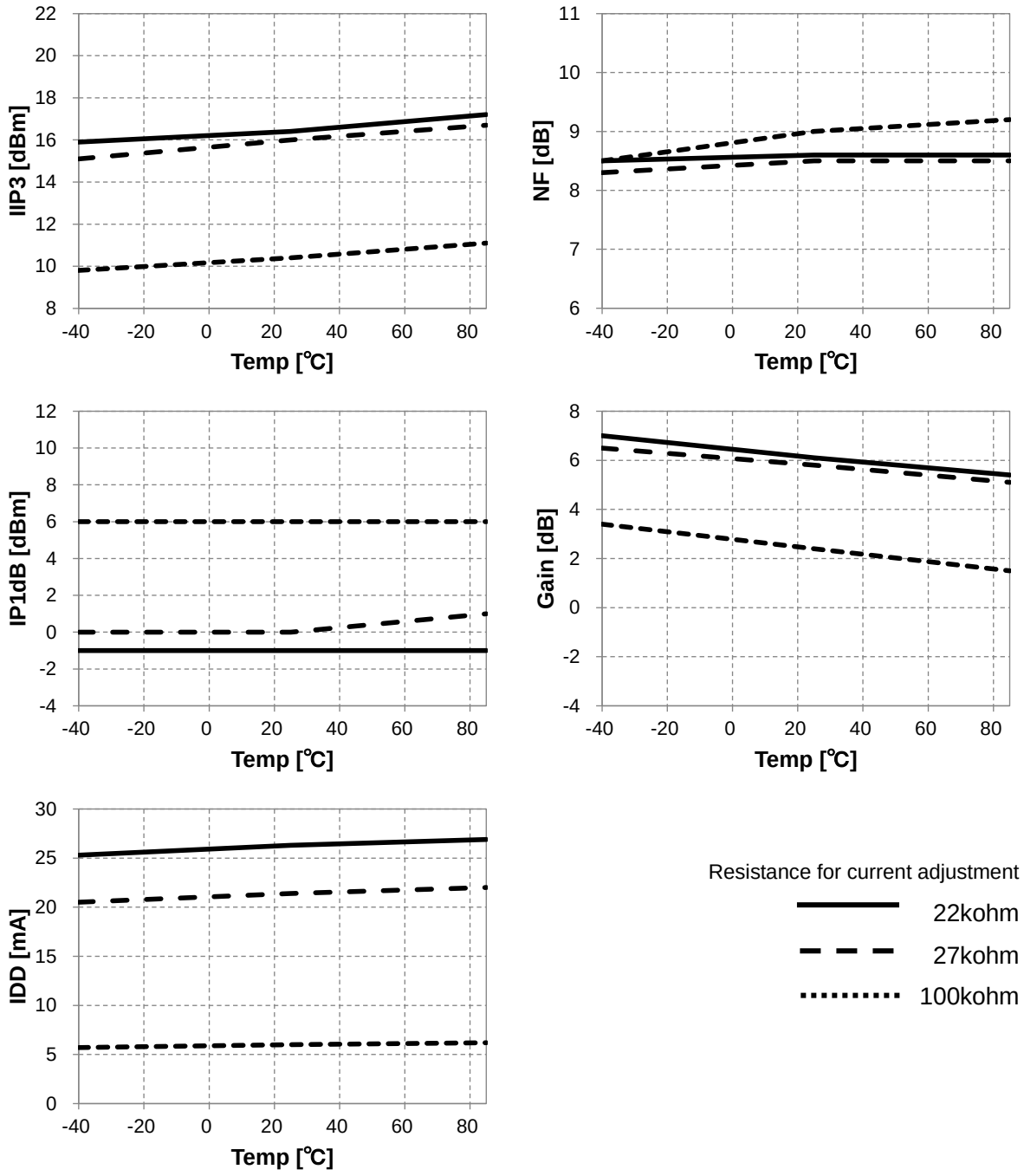



**Fig. 4 Over temperature vs. IIP3, NF, IP1dB, Gain, IDD**

### 3. Supply voltage vs. IIP3, NF, P1dB, Gain, IDD

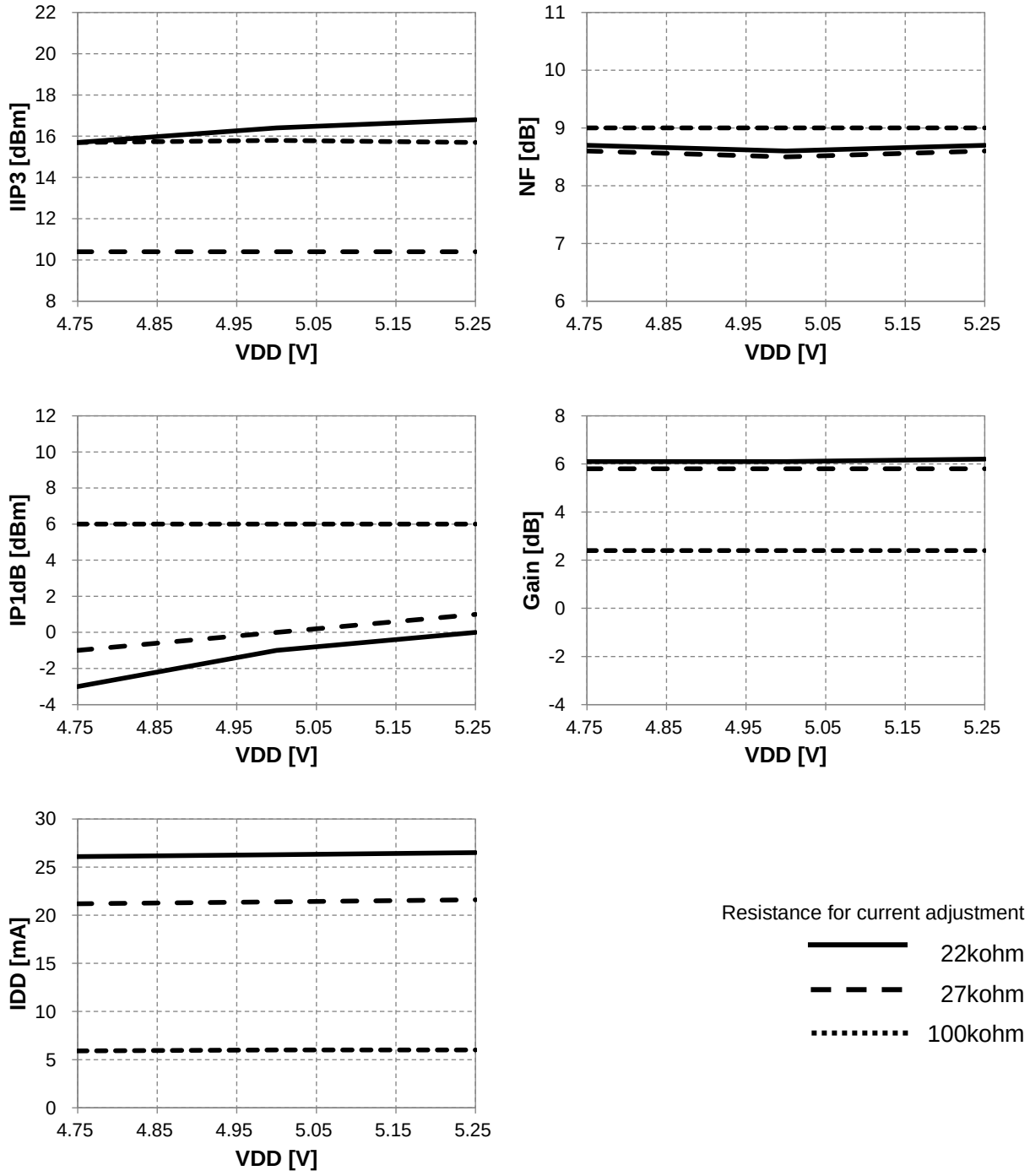



**Fig. 5 Supply voltage vs. IIP3, NF, IP1dB, Gain, IDD**

## 4. RF input frequency vs. IIP3, NF, Gain

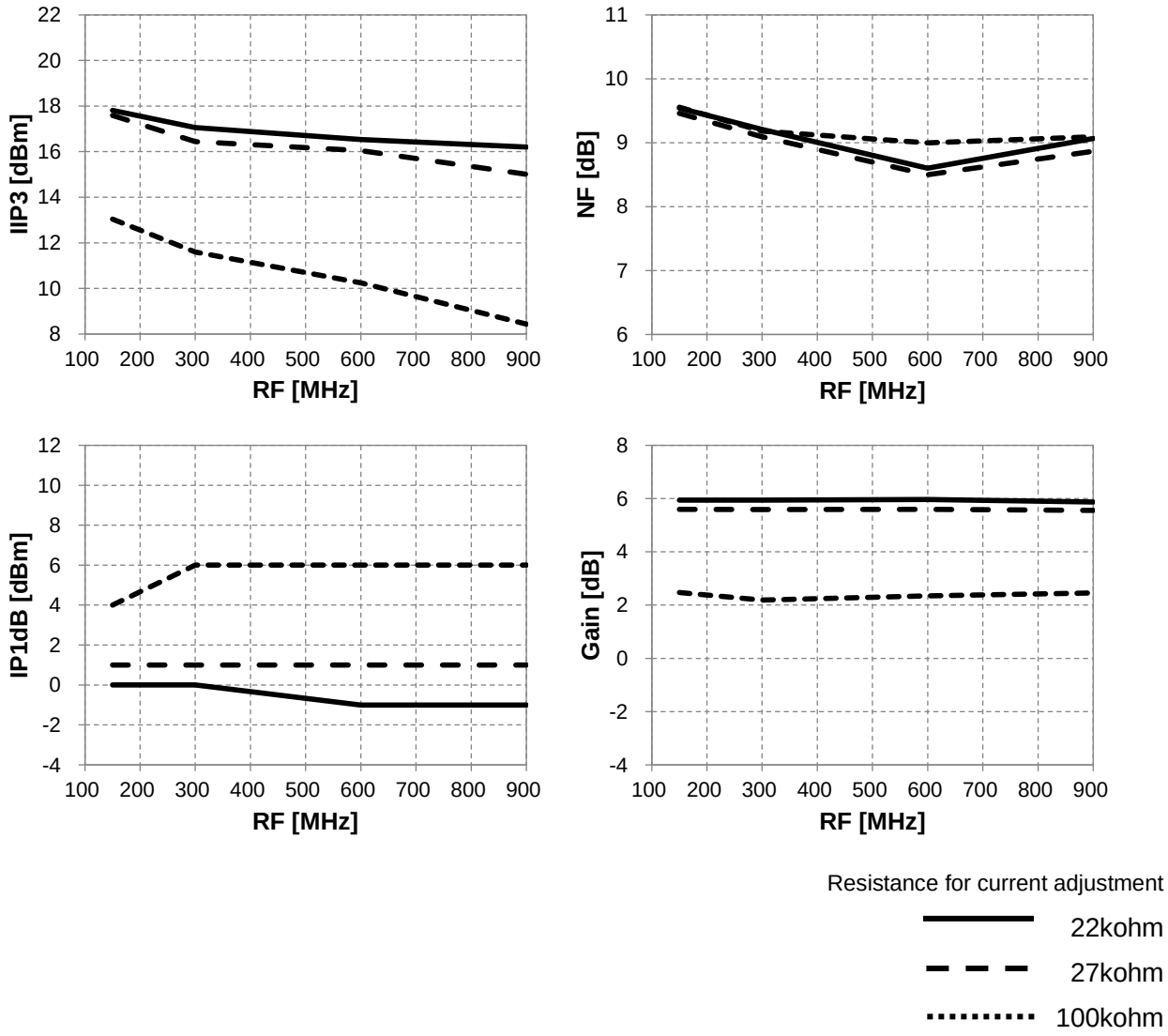



**Fig. 6 RF input frequency vs. IIP3, NF, Gain**

## 5. IF input frequency vs. IIP3, NF, Gain

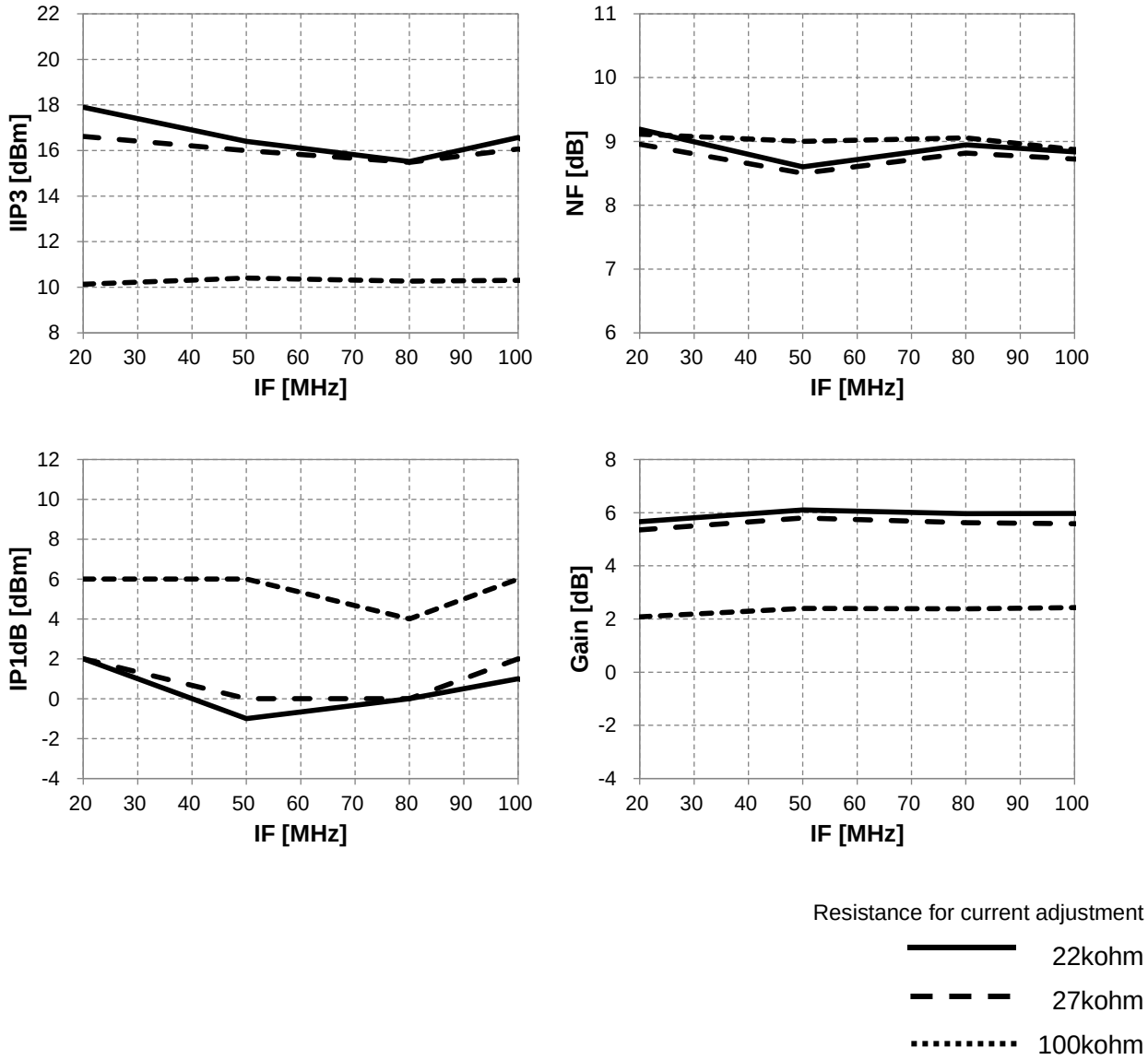



**Fig. 7 IF input frequency vs. IIP3, NF, Gain**

## 6. Lo input power vs. IIP3, NF, Gain

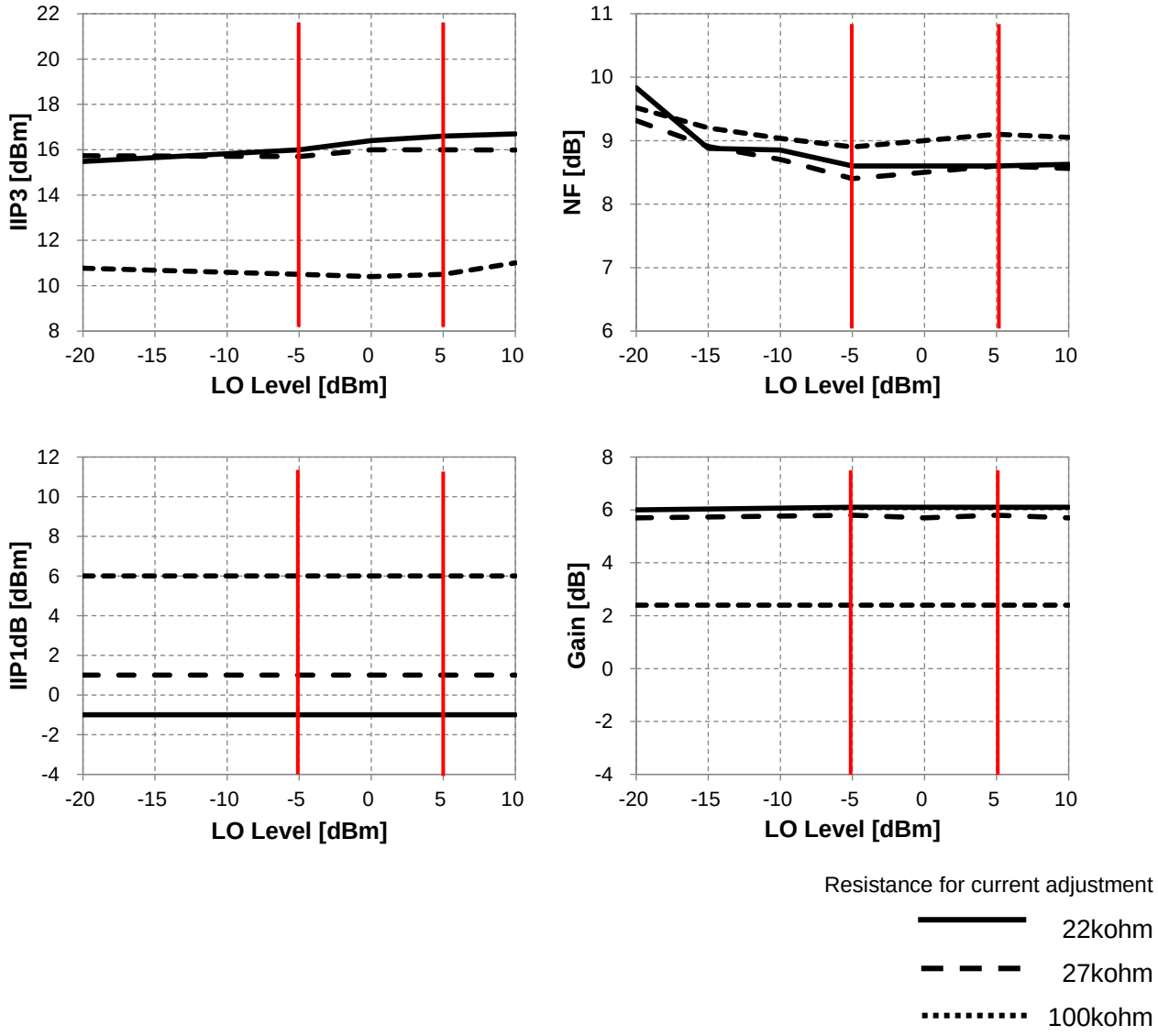



**Fig. 8 Lo input power vs. IIP3, NF, Gain**

## 7. Output Load Resistor（RLoad） vs. IIP3, NF, Gain

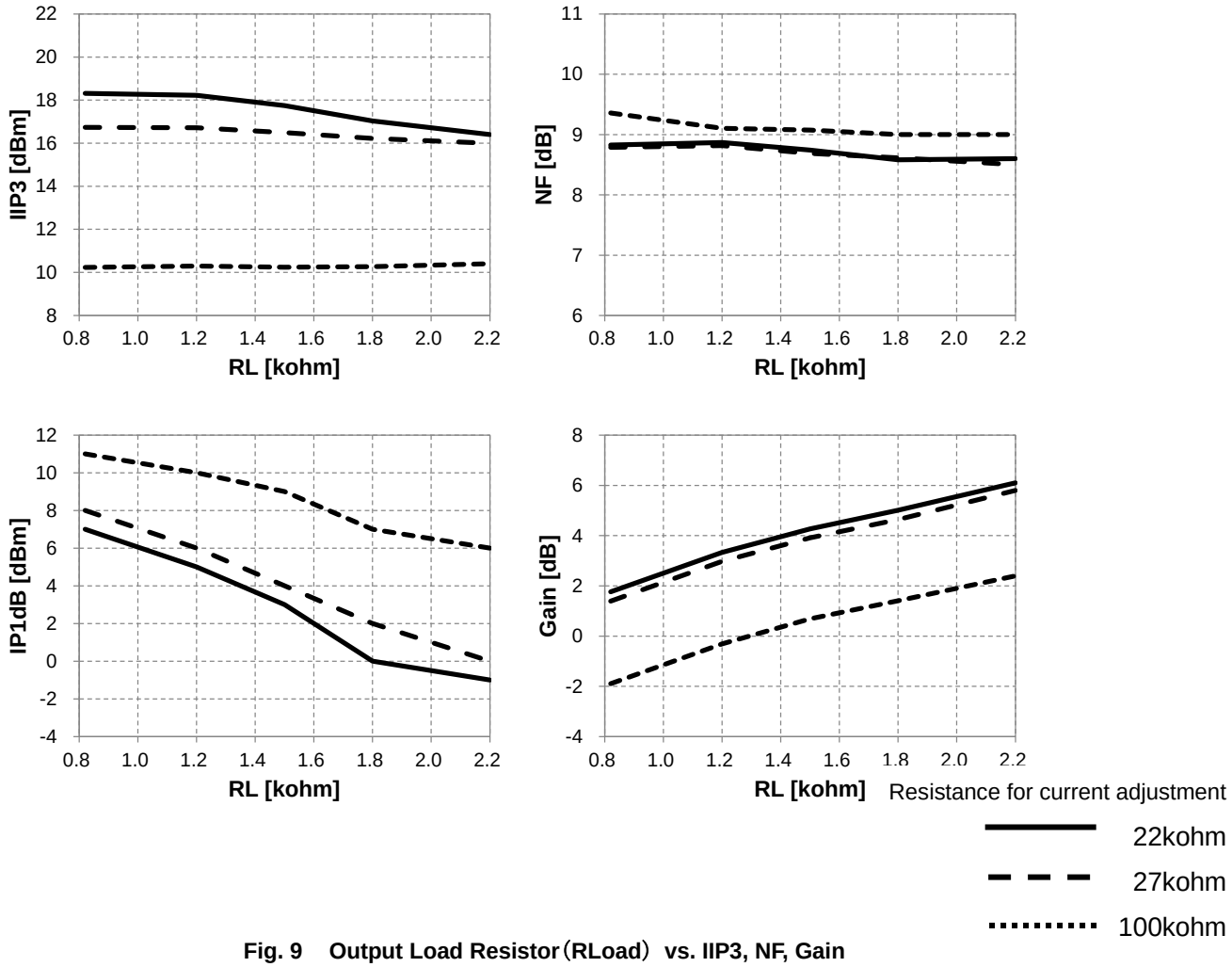



**Fig. 9 Output Load Resistor（RLoad） vs. IIP3, NF, Gain**

## 8. Leakage

RFIN=600MHz,-20dBm, LO input=550MHz,0dBm, RLoad=2.2kΩ, Ta=25℃ VDD=5V

| Parameter | BIAS | Typ. | Unit |
|---|---|---|---|
| RF – LO Leakage | 22kΩ | -60 | dBc |
| | 100kΩ | -58 | dBc |
| RF – IF Leakage | 22kΩ | -59 | dBc |
| | 100kΩ | -60 | dBc |
| LO – RF Leakage | 22kΩ | -52 | dBc |
| | 100kΩ | -55 | dBc |
| LO – IF Leakage | 22kΩ | -57 | dBc |
| | 100kΩ | -56 | dBc |

# 9. Typical Evaluation Board Schematic

1. Typical Evaluation Board Schematic

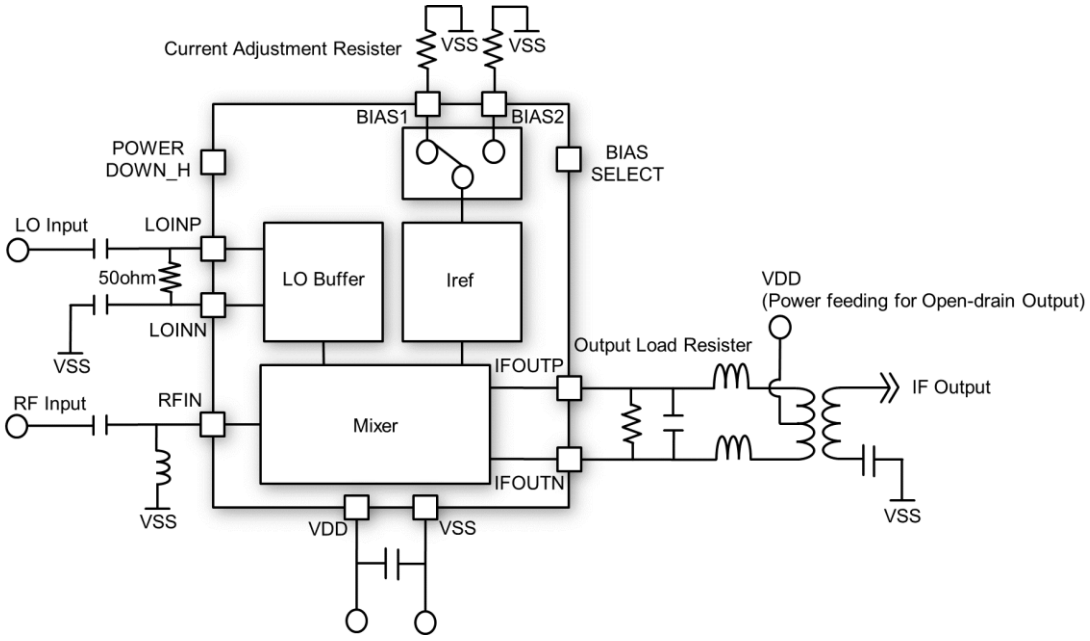



**Fig.10 Typical Evaluation Board Schematic**

Note) The exposed pad at the center of the backside should be connected to ground.

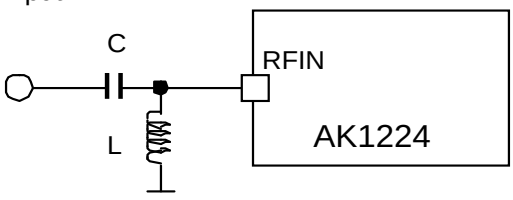
Note) The open drain output needs power feeding via a inductor. (IFOUTP pin and IFOUTN pin)

Note) It is necessary to adjust impedance matching as to its setting frequency. (RF input and IF output)

2. Example of impedance matching

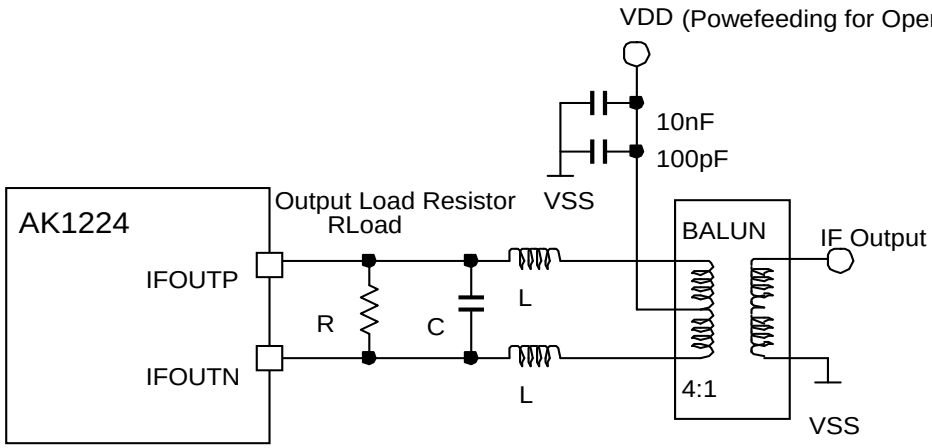
・RFIN

RF Input




| Frequency[MHz] | C1[pF] | L[nH] | Impedance[ohm] |
|---|---|---|---|
| 100 | 68 | 220 | 49.3 - j5.4 |
| 600 | 15 | 22 | 48.3 - j0.7 |
| 900 | 12 | 12 | 44.48 – j1.0 |

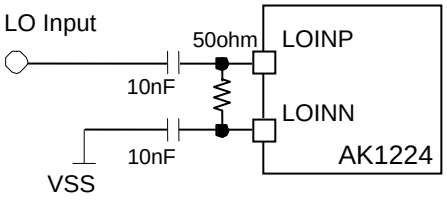
・IFOUT



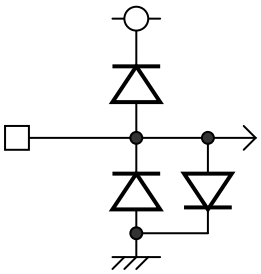
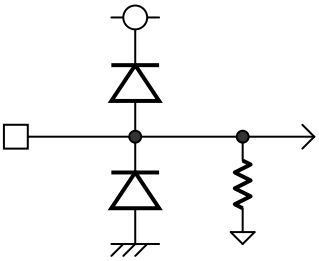
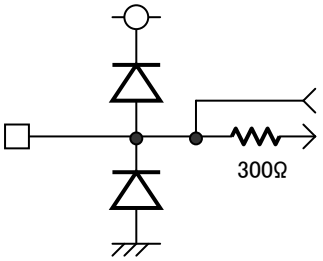
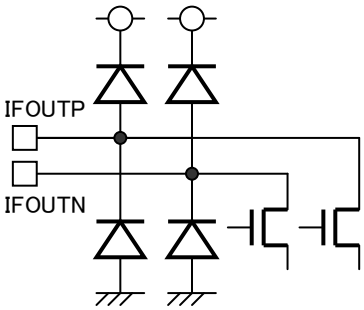

| Frequency [MHz] | R1 [kohm] | C [pF] | L [nH] | Impedance[ohm] |
|---|---|---|---|---|
| 20 | 2.2 | 10 | 2200 *1 | 51.2 – j11.6 |
| 50 | 2.2 | 3.3 | 1000 *1 | 51.6 – j0.6 |
| 100 | 2.2 | 1.2 | 470 *1 | 48.6 – j5.7 |

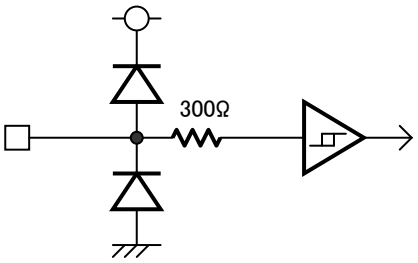
*1)Murata LQW series

・LOINP/LOINN



## 10. LSI Interface schematic

| No. | Name | I/O | Function |
|---|---|---|---|
| 1 | RFIN | I | RF Input pin  |
| 4 | LOINN | I | LO Input pins |
| 5 | LOINP | |  |
| 6 | BIAS1 | I/O | Analog I/O pins |
| 7 | BIAS2 | |   |
| 11 | IFOUTN | O | IF Output pins |
| 12 | IFOUTP | |   |

| | | | |
|---|---|---|---|
| 14 | Power Down_H | I | Digital Input pins   |
| 15 | BIAS Select | | |

## 11. Outer Dimensions

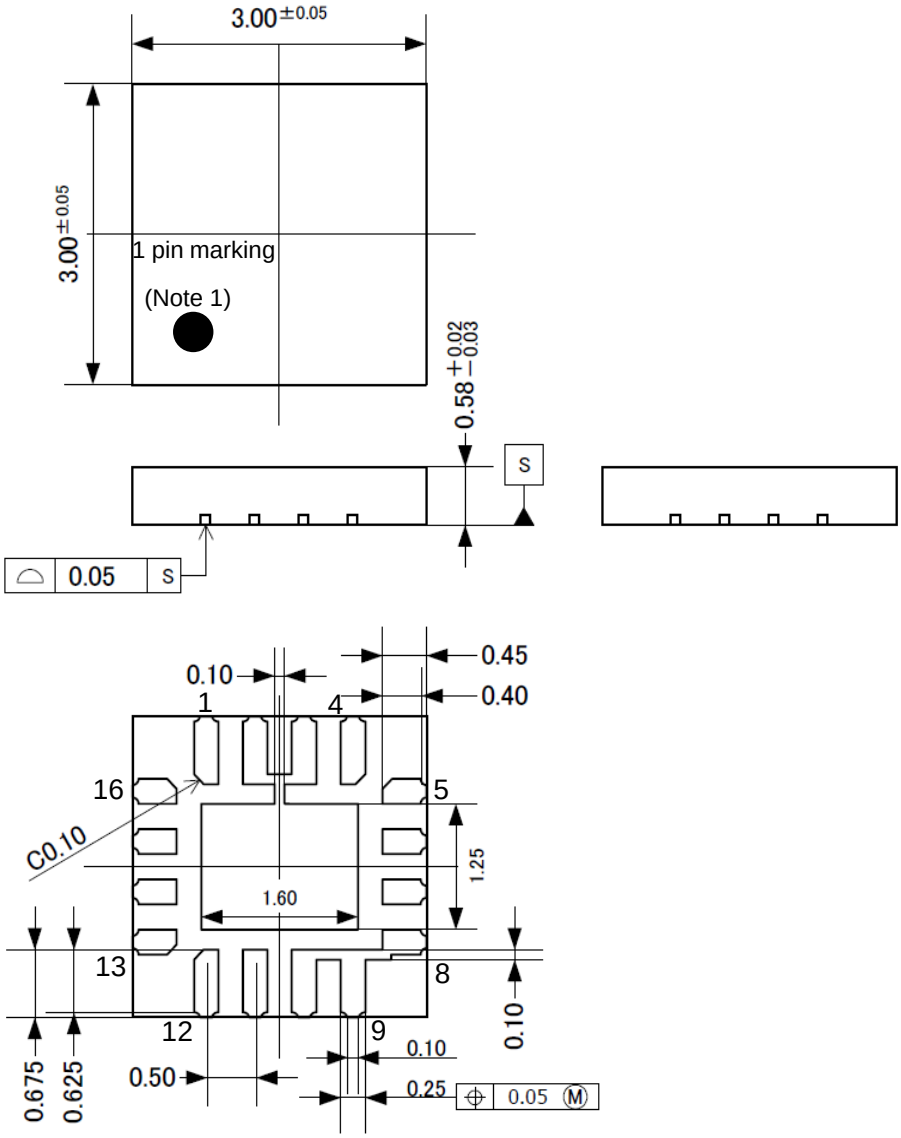



**Fig.11 Outer Dimensions**

Note 1. 1 pin marking is only a reference for the 1 pin location on the top of package.

## 12. Marking

(a) Style : UQFN

(b) Number of pins : 16

(c) 1 pin marking : ○

(d) Product number : 1224

(e) Date code : YWWL (4 digits)

Y : Lower 1 digit of calendar year (Year 2012 → 2, 2013 → 3 ...)

WW : Week

L : Lot identification, given to each product lot which is made in a week
→ LOT ID is given in alphabetical order (A, B, C…).

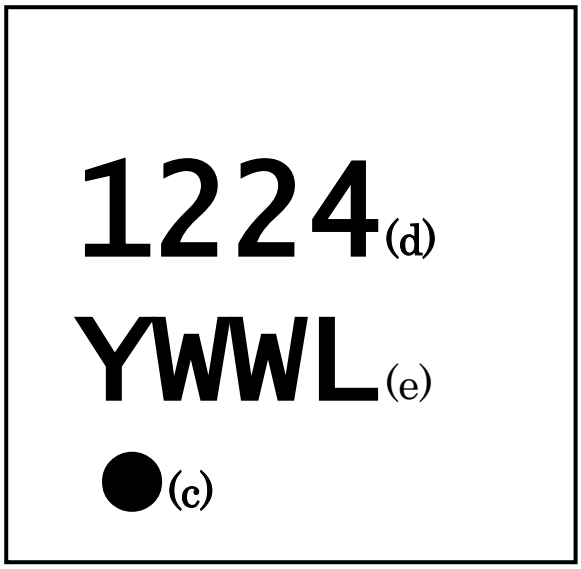



**Fig.12 Marking**

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