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AK1547

4GHz Low Noise Integer-N Frequency Synthesizer

1. Overview

The AK1547 is an Integer-N PLL (Phase Locked Loop) frequency synthesizer, covering a wide range of frequency from 500MHz to 4GHz. Consisting of a highly accurate charge pump, a reference divider, a programmable divider and a dual-modulus prescaler (P/P+1), this product provides high performance, very low Phase Noise and small footprints.

An ideal PLL can be achieved by combining the AK1547 with the external loop filter and VCO (Voltage Controlled Oscillator). Access to the registers is controlled via a 3-wire serial interface. The operating supply voltage is from 2.7V to 5.5V, and the charge pump circuit and the serial interface can be driven by individual supply voltage.

2. Features

- Operating frequency : 500MHz to 4GHz
- Programmable charge pump current : 650 μ A to 5200 μ A typical with 8steps
The current range can be controlled by an external resistor.
- Fast lock mode for improved lock time : The programmable timer can switch two charge pump current setting.
- Supply Voltage : 2.7 to 5.5 V (PVDD, AVDD pins)
- Separate Charge Pump Power Supply : PVDD to 5.5V (CPVDD pin)
- Excellent Phase Noise : -218dBc/Hz
- On-chip lock detection feature of PLL : Selectable Phase Frequency Detector (PFD) Output or digital filtered lock detect
- Package : 20pin QFN (0.5mm pitch, 4mm \times 4mm \times 0.75mm)
- Operating temperature : -40 $^{\circ}$ C to 85 $^{\circ}$ C



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In this specification, the following notations are used for specific signal and register names.

[Name] : Pin name

<Name> : Register group name (Address name)

{Name} : Register bit name



3. Block Diagram

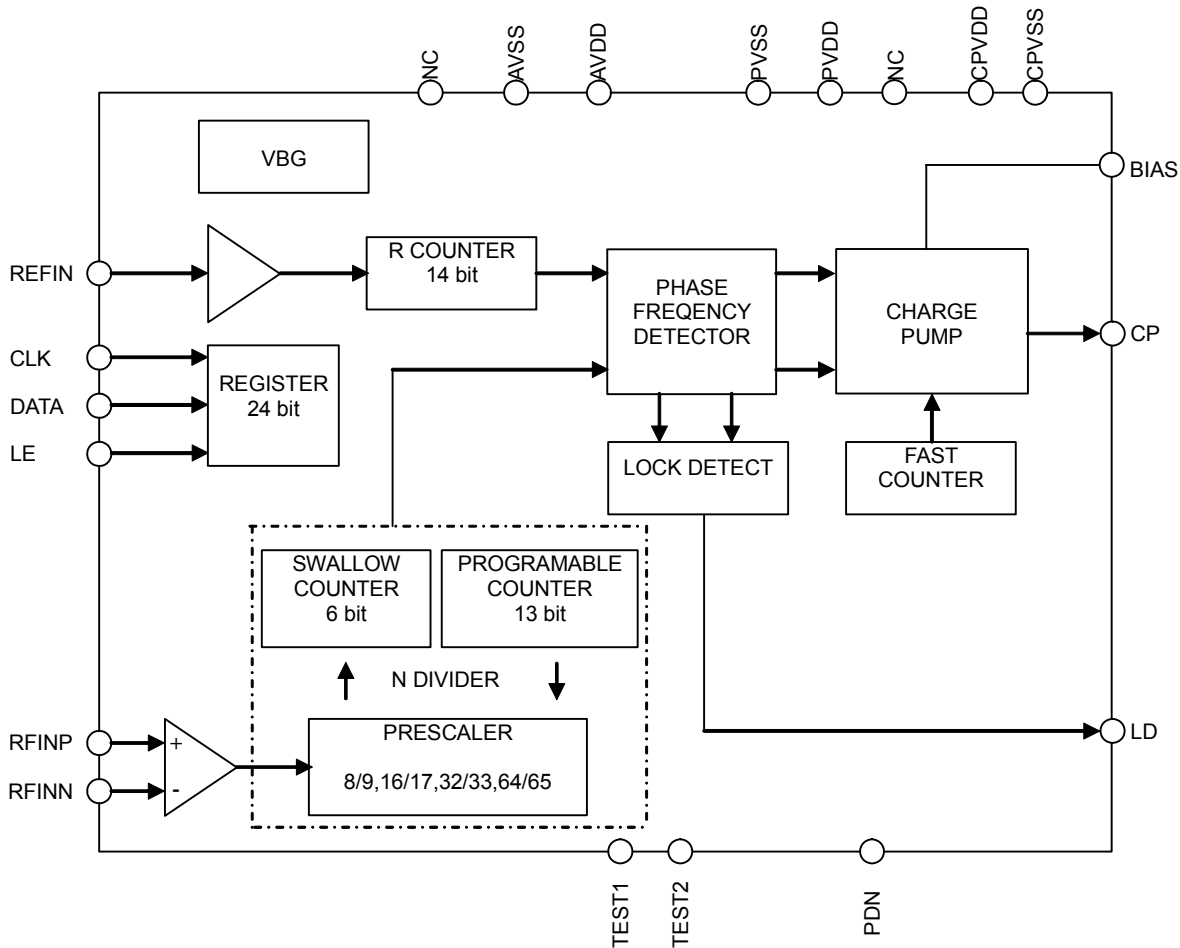


Fig. 1 Block Diagram



4. Pin Functional Description and Assignments

Table 1 Pin Functions

No.	Name	I/O	Pin Functions	Power down (Note 1)	Remarks
1	CPVSS	G	Charge pump ground		
2	TEST1	DI	Test pin 1		Internal pull-down, Schmidt trigger input
3	AVSS	G	Analog ground		
4	RFINN	AI	Complementary input to the RF Prescaler		
5	RFINP	AI	Input to the RF Prescaler		
6	AVDD	P	Power supply for analog blocks		
7	NC				
8	REFIN	AI	Reference signal input		
9	PVSS	G	Peripherals ground		
10	TEST2	DI	Test pin 2		Internal pull-down, Schmidt trigger input
11	PDN	DI	Power down		Schmidt trigger input
12	CLK	DI	Serial clock input		Schmidt trigger input
13	DATA	DI	Serial data input		Schmidt trigger input
14	LE	DI	Load enable input		Schmidt trigger input
15	LD	DO	Lock detect output	"Low"	
16	PVDD	P	Power supply for peripherals		
17	NC				
18	CPVDD	P	Power supply for charge pump		
19	BIAS	AIO	Resistance pin for setting charge pump current		
20	CP	AO	Charge pump output	"Hi-Z"	

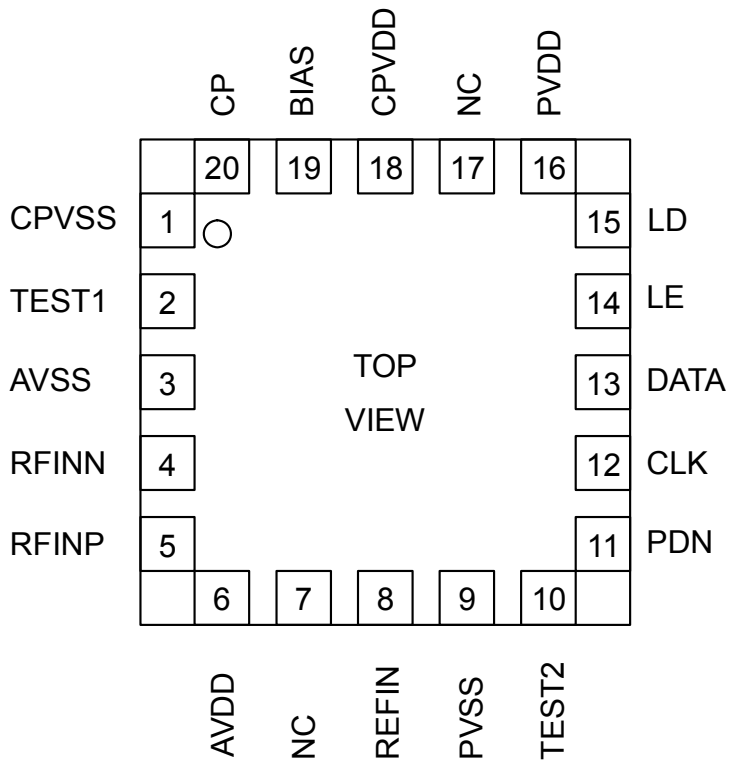
Note 1) "Power Down" means the state of [PDN]="Low" after power on.

The following table shows the meaning of abbreviations used in the "I/O" column.

AI: Analog input pin	AO: Analog output pin	AIO: Analog I/O pin	DI: Digital input pin
DO: Digital output pin	P: Power supply pin	G: Ground pin	



2. Pin Assignments



20pin QFN (0.5mm pitch, 4mm×4mm)

Fig. 2 Pin Assignments



5. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD1	-0.3	6.5	V	[AVDD], [PVDD] (Note 1)
	VDD2	-0.3	6.5	V	[CPVDD] (Note 1)
Ground Level	VSS1	0	0	V	[AVSS], [PVSS]
	VSS2	0	0	V	[CPVSS]
Analog Input Voltage	VAIN	VSS1-0.3	VDD1+0.3	V	[RFINN], [RFINP], [REFIN] (Notes 1 & 2)
Digital Input Voltage	VDIN	VSS1-0.3	VDD1+0.3	V	[CLK], [DATA], [LE], [PDN], [TEST1], [TEST2] (Notes 1 & 2)
Input Current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	125	°C	

Note 1) 0V reference for all voltages.

Note 2) Maximum must not be over 6.5V.

Exceeding these maximum ratings may result in damage to the AK1547. Normal operation is not guaranteed at these extremes.

6. Recommended Operating Range

Table 3 Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD1	2.7	5.0	5.5	V	Applied to the [AVDD],[PVDD] pins
	VDD2	VDD1		5.5	V	Applied to the [CPVDD] pin

Note 1) VDD1 and VDD2 can be driven individually within the Recommended Operating Range.

Note 2) All specifications are applicable within the Recommended Operating Range (operating temperature / supply voltage).



7. Electrical Characteristics

1. Digital DC Characteristics

Table 4 Digital DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
High level input voltage	Vih		0.8×VDD1			V	Note 1)
Low level input voltage	Vil				0.2×VDD1	V	Note 1)
High level input current 1	Iih1	Vih = VDD1=5.5V	-1		1	μA	Note 2)
High level input current 2	Iih2	Vih = VDD1=5.5V	27	55	110	μA	Note 3)
Low level input current	Iil	Vil = 0V, VDD1=5.5V	-1		1	μA	Note 1)
High level output voltage	Voh	Ioh = -500μA	VDD1-0.4			V	Note 4)
Low level output voltage	Vol	Iol = 500μA			0.4	V	Note 4)

Note 1) Applied to the [CLK], [DATA], [LE], [PDN], [TEST1] and [TEST2] pins.

Note 2) Applied to the [CLK], [DATA], [LE] and [PDN] pins.

Note 3) Applied to the [TEST1] and [TEST2] pins.

Note 4) Applied to the [LD] pin.

2. Serial Interface Timing

<Write-In Timing>

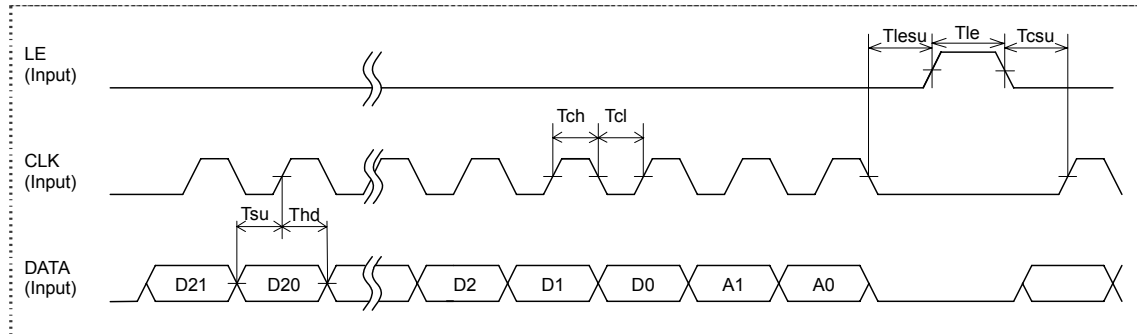


Fig. 3 Serial Interface Timing Chart

Table 5 Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock L level hold time	Tcl	25			ns	
Clock H level hold time	Tch	25			ns	
Clock setup time	Tcsu	10			ns	
Data setup time	Tsu	10			ns	
Data hold time	Thd	10			ns	
LE setup time	Tlesu	10			ns	
LE pulse width	Tle	25			ns	



3. Analog Circuit Characteristics

The resistance of 27kΩ is connected to the [BIAS] pin.

VDD1=2.7V to 5.5V, VDD2=VDD1 to 5.5V, $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Remarks
RF Characteristics					
Input Sensitivity	-10		0	dBm	
Input Frequency	500		4000	MHz	
REFIN Characteristics					
Input Sensitivity	0.4		VDD1	Vpp	
Input Frequency	5		104	MHz	
Maximum Allowable Prescaler Output Frequency			125	MHz	
Phase Detector					
Phase Detector Frequency			55	MHz	
Charge Pump					
Charge Pump Maximum Value		5200		μA	
Charge Pump Minimum Value		650		μA	
Icp TRI-STATE Leak Current		1		nA	$0.6 \leq V_{cpo} \leq VDD2 - 0.7$, $T_a = 25^{\circ}\text{C}$
Mismatch between Source and Sink Currents (Note 1)			10	%	$V_{cpo} = VDD2/2$, $T_a = 25^{\circ}\text{C}$
Icp vs. Vcpo (Note 2)			15	%	$0.5 \leq V_{cpo} \leq VDD2 - 0.5$, $T_a = 25^{\circ}\text{C}$
Current Consumption					
IDD1			10	μA	[PDN]="0" or {PD1}=1
IDD2 (Note3, Note4)		12	18	mA	[PDN]="1", {PD1}=0, IDD for VDD1
IDD3 (Note3)		0.8	1.6	mA	[PDN]="1", {PD1}=0, IDD for VDD2

Note 1) Mismatch between Source and Sink Currents : $\frac{(|I_{sink}| - |I_{source}|)}{(|I_{sink}| + |I_{source}|)/2} \times 100$ [%]

Note 2) See "Charge Pump Characteristics - Voltage vs. Current". Vcpo is the output voltage at [CP].

$$I_{cp} \text{ vs. } V_{cpo} : \frac{\{1/2 \times (|I_1| - |I_2|)\}}{\{1/2 \times (|I_1| + |I_2|)\}} \times 100$$
 [%]

Note 3) When [PDN] = "1" and {PD1}=0, the total power supply current of the AK1547 is "IDD2+IDD3+ Charge pump current".

Note 4) RFIN=4GHz, 5dBm input, REFIN=100MHz, 10dBm input, PRESCALER=32,
Phase Detector Frequency=1MHz

Resistance Connected to the BIAS Pin for Setting Charge Pump Output Current

Parameter	Min.	Typ.	Max.	Unit	Remarks
BIAS resistance	22	27	33	kΩ	

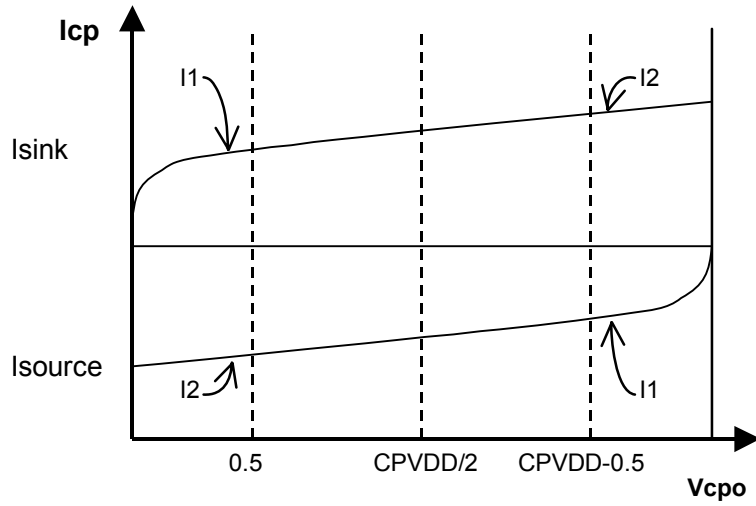


Fig. 4 Charge Pump Characteristics - Voltage (V_{cpo}) vs. Current (I_{cp})



8. Block Functional Descriptions

1. Frequency Setup

The following formula is used to calculate the frequency setting for the AK1547.

$$\text{Frequency setting (external VCO output frequency)} = F_{\text{PFD}} \times N$$

Where :

- N : Dividing number $N = [(P \times B) + A]$
- F_{PFD} : Phase detector frequency $F_{\text{PFD}} = [\text{REFIN}]$ pin input frequency / R counter dividing number
- P : Prescaler Value (See <Address2>:{Pre[1:0]})
- B : B (Programmable) counter value (See <Address1>:{B[12:0]})
- A : A (Swallow) counter value (See <Address1>:{A[5:0]})

Calculation example

The output frequency of external reference frequency oscillator is 10MHz, and F_{PFD} is 200kHz and VCO frequency is 2460MHz.

AK1547 setting :

$$R \text{ (Reference counter)} = 10000000 / 200000 = 50 \text{ (<Address0>:{R[13:0]} = "50")}$$

$$P = 32 \text{ (<Address2>:{PRE[1:0]} = "10\text{Bin}")}$$

$$B = 384 \text{ (<Address1>:{B[12:0]} = "384")}$$

$$A = 12 \text{ (<Address1>:{A[5:0]} = "12")}$$

$$\text{Frequency setting} = 200\text{kHz} \times [(32 \times 384) + 12] = 2460\text{MHz}$$

Lower limit for setting consecutive dividing numbers

In AK1547, it is impossible to set consecutive dividing numbers below the lower limit. The lower limit, N_{min} , depends on the Prescaler setting, and can be calculated by the following formula;

$$N_{\text{min}} = P^2 - P$$

The dividing number below N_{min} can't be set for succession. For example, in the case of $P=16$, 240 and over can be set as consecutive dividing number.



2. Charge Pump, Loop Filter

The current setting of charge pump can switch with the built-in timer for Fast Lock.

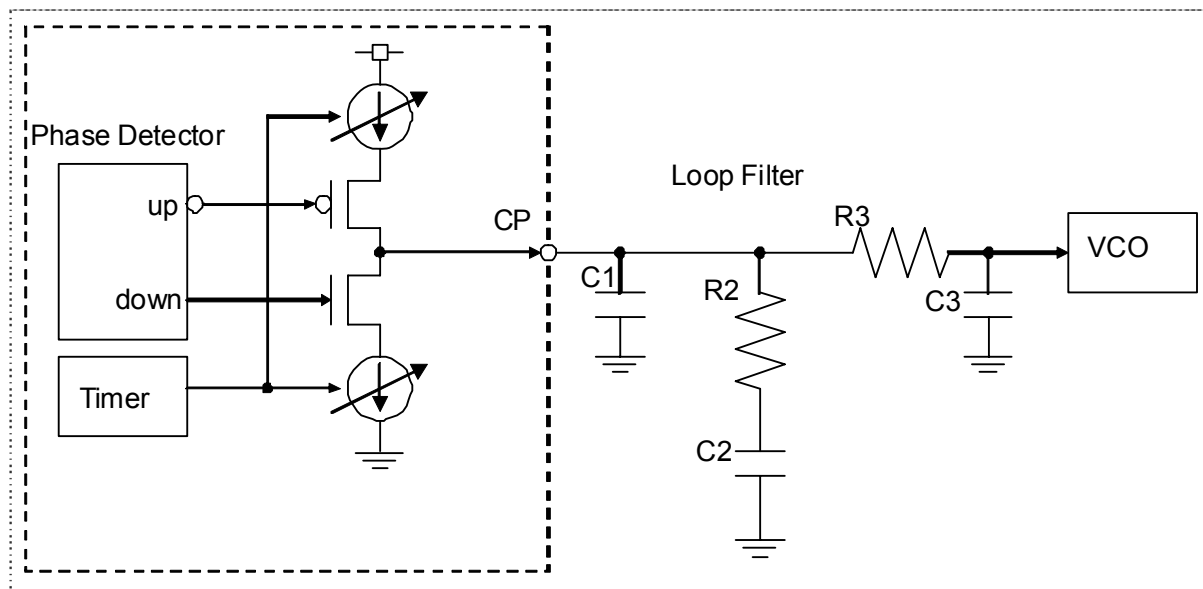


Fig. 5 Loop Filter Schematic

The charge pump current for normal operation (CP1) is determined by the setting in {CP1[2:0]}, which is a 3-bit address of {D[15:13]} in <Address2> and a value of the resistance connected to the [BIAS] pin. The charge pump current for the Fast Lock Up mode operation (CP2) is determined by the setting in {CP2[2:0]}, which is a 3-bit address of D[18:16] in <Address2> and a value of the resistance connected to the [BIAS] pin.

The following formula shows the relationship among the resistance value, the register setting and the electric current value.

$$\text{charge pump minimum current (Icp_min) [A]} = 17.46 / \text{Resistance connected to the BIAS pin } [\Omega]$$

$$\text{charge pump current (Icp) [A]} = \text{Icp_min [A]} \times (\{\text{CP1}\} \text{ or } \{\text{CP2}\} \text{ setting} + 1)$$

The allowed value range for the resistance connected to the [BIAS] pin is from 22 to 33k Ω for both normal and Fast Lock Up mode operations.



3. Fast Lock Up Mode

Setting {FAST[1:0]} in <Address2> to “11Bin” and {CPGAIN} in <Address1> to “1” enables the Fast Lock Up mode for the AK1547.

The Fast Lock Up mode is enabled only during the time period set by the timer according to the counter value in {TIMER[3:0]} in <Address2>. The charge pump current is set to the value specified by {CP2}. When the specified time period elapses, the Fast Lock Up mode operation is switched to the normal operation. And {CPGAIN} in <Address1> is reset to “0”.

{TIMER[3:0]} in <Address2> is used to set the time period for this mode. The following formula is used to calculate the time period :

$$\text{Switchover time} = 1 / F_{\text{PFD}} \times \text{Counter Value}$$

$$\text{Counter Value} = 3 + (\text{Timer}[3:0] \text{ setting} \times 4)$$

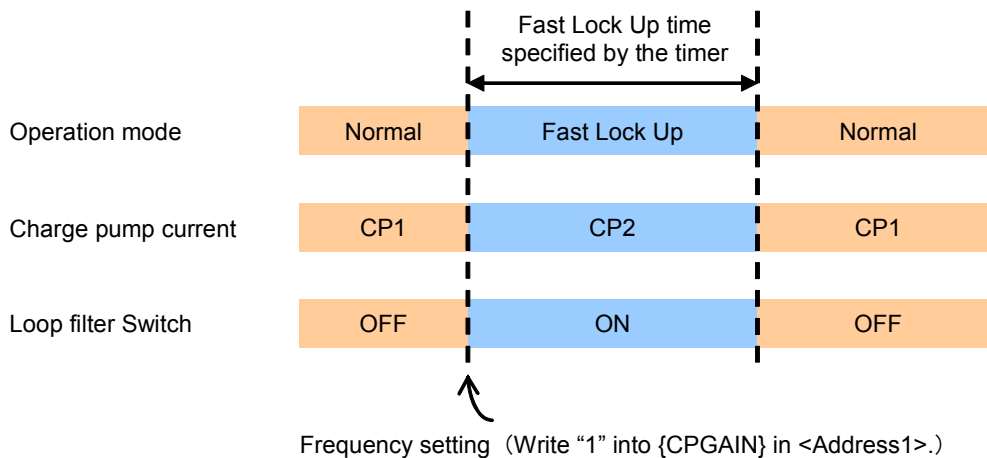


Fig. 6 Fast Lock Up Mode Timing Chart

4. Lock Detect

Lock detect output can be selected by {LD[2:0]} in <Address2>. When {LD} is set to "101Bin", the phase detector outputs an un-manipulated phase detection (comparison) result. (This is called "analog lock detect".) When {LD} is set to "001Bin", the lock detect signal is output according to the on-chip logic. (This is called "digital lock detect".)

The lock detect can be done as following (Case of $R > 1$):

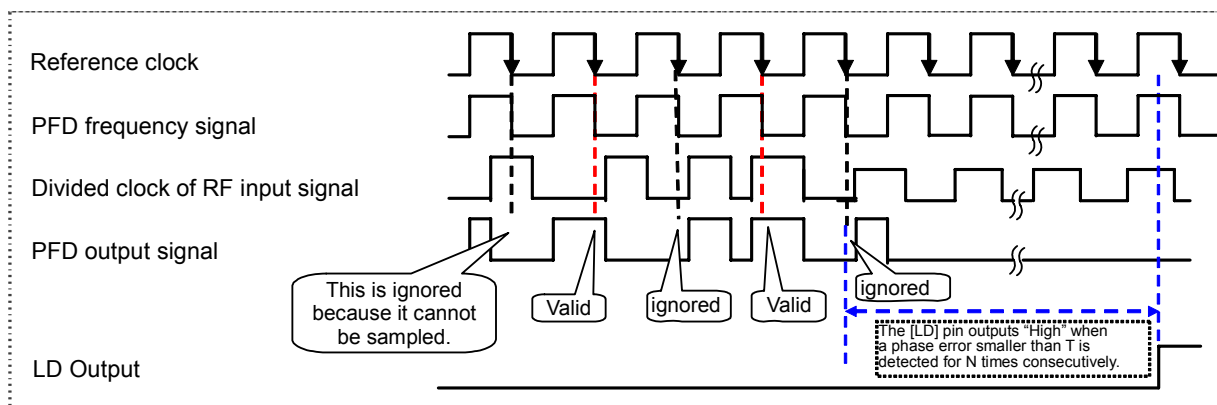
The [LD] pin is in unlocked state (which outputs "Low") when a frequency setup is made.

In the digital lock detect, the [LD] pin outputs "High" (which means the locked state) when a phase error smaller than a cycle of [REFIN] clock (T) is detected for N times consecutively. When a phase error larger than T is detected for N times consecutively while the [LD] pin outputs "High", then the [LD] pin outputs "Low" (which means the unlocked state). The counter value N can be set by {LDP} in <Address0>. The N is different between "unlocked to locked" and "locked to unlocked".

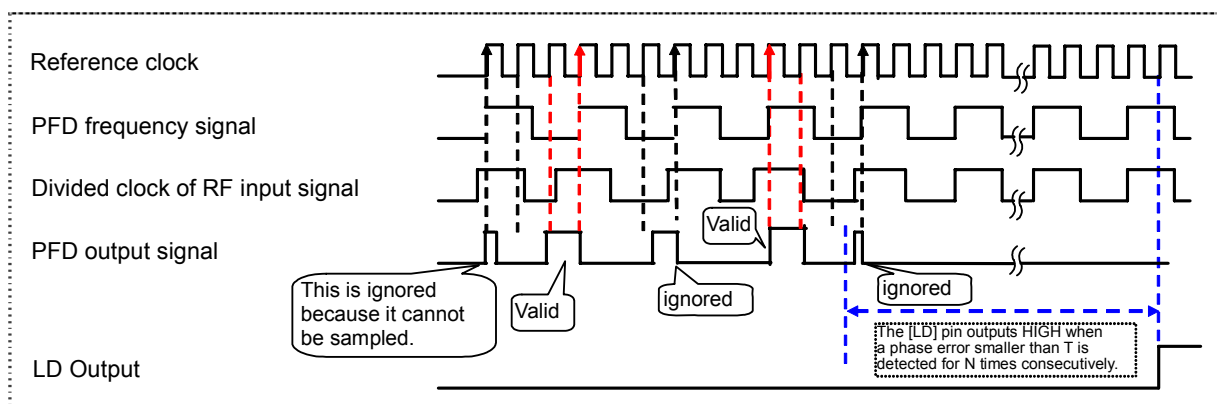
Table 6 Lock Detect Precision

{LDP}	unlocked to locked	locked to unlocked
0	$N=15$	$N=3$
1	$N=31$	$N=7$

The lock detect signal is shown below:



Case of " $R = 1$ "



Case of " $R > 1$ "

Fig. 7 Digital Lock Detect Operations

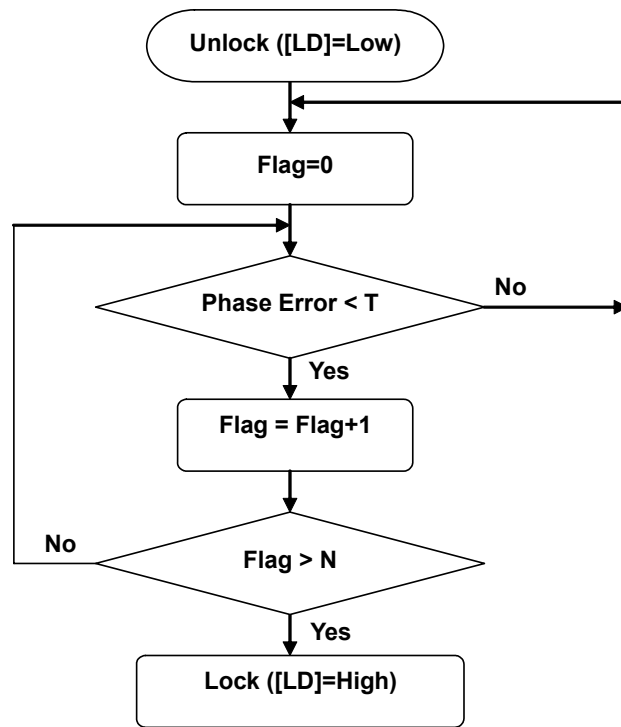


Fig. 8 Unlock to Lock Operation Flow

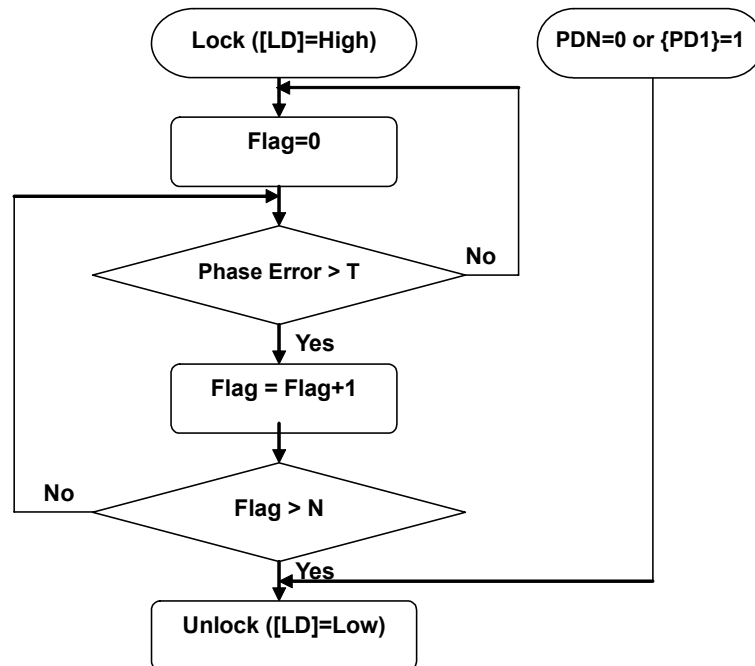


Fig. 9 Lock to Unlock Operation Flow

5. Reference counter

The reference input can be set with a dividing number in the range of 1 to 16383 using {R [13:0]}, which is a 14-bit address of {D[13:0]} in <Address0>. 0 cannot be set as a dividing number.

6. Prescaler

The dual modulus prescaler ($P/P + 1$) and the swallow counter are used to provide a large dividing ratio. The prescaler is set by {PRE[1:0]}, which is a 2-bit latch of {D[21:20]} in <Address2>.

{PRE[1:0]}="00Bin", P=8, Dual modulus prescaler 8/9

{PRE[1:0]}="01Bin", P=16, Dual modulus prescaler 16/17

{PRE[1:0]}="10Bin", P=32, Dual modulus prescaler 32/33

{PRE[1:0]}="11Bin", P=64, Dual modulus prescaler 64/65

The Maximum Allowable Prescaler Output Frequency is 125MHz. "P" must be set as "RF Input Frequency/P \leq 125MHz".

7. Power-down and Power-save mode

It is possible to operate in the power-down or power-save mode if necessary by using the external control pin.

Power On

Follow the power-up sequence.

Normal Operation

Table 7 Power-down and Power-save mode

[PDN]	<Address2>		Function
	{PD2}	{PD1}	
"Low"	X	X	Power Down
"High"	X	0	Normal Operation
"High"	0	1	Asynchronous Power Down
"High"	1	1	Synchronous Power Down

X

: Don't care ("0" is recommended)



9. Register Map

Name	Data	Address	
R Counter	D21 - D0	0	0
N Counter (A and B)		0	1
Function		1	0
Initialization		1	1

Name	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
R Count	0	0	0	LDP	0	0	0	0	R [13]	R [12]	R [11]	R [10]	R [9]	R [8]	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	0x0
N Count	0	0	CP GAIN	B [12]	B [11]	B [10]	B [9]	B [8]	B [7]	B [6]	B [5]	B [4]	B [3]	B [2]	B [1]	B [0]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	0x1
Func.	PRE [1]	PRE [0]	PD2	CP2 [2]	CP2 [1]	CP2 [0]	CP1 [2]	CP1 [1]	CP1 [0]	TIME R [3]	TIME R [2]	TIME R [1]	TIME R [0]	FAST [1]	FAST [0]	CP HIZ	CP POLA	LD [2]	LD [1]	LD [0]	PD1	CNTR RST	0x2
Initial.	PRE [1]	PRE [0]	PD2	CP2 [2]	CP2 [1]	CP2 [0]	CP1 [2]	CP1 [1]	CP1 [0]	TIME R [3]	TIME R [2]	TIME R [1]	TIME R [0]	FAST [1]	FAST [0]	CP HIZ	CP POLA	LD [2]	LD [1]	LD [0]	PD1	CNTR RST	0x3



Notes for writing into registers

After powers on AK1547, the initial registers value are not defined. It is required to write the data in all addresses in order to commit it.

[Examples of writing into registers]

(Ex. 1) Power-On

- Bring [PDN] to "0 (Low)"
- Apply VDD
- Program Address0, Address1 and Address2 ({PD1}="1" is recommended)
- Bring [PDN] to "1 (High)"
- Program {PD1} in Address2 to "0"

(Ex. 2) Changing frequency settings : Initialization

- Program Address3
- Program Address1

(Ex. 3) Changing frequency settings : Counter reset

- Program Address2. As part of this, load "1" to both {PD1} and {CNTR_RST}.
- Program Address1
- Program Address2. As part of this, load "0" to both {PD1} and {CNTR_RST}.

(Ex. 4) Changing frequency settings : PDN pin method

- Bring [PDN] to "0 (Low)"
- Program Address1
- Bring [PDN] to "1 (High)"



10. Function Description - Registers

< Address0 : R Counter >

D[21:19]	D18	D[17:14]	D[13:0]	Address
0	LDP	0	R[13:0]	00

D[21:19], D[17:14] : These bits are set to the following for normal operation

D21	D20	D19		D17	D16	D15	D14
0	0	0		0	0	0	0

LDP : Lock Detect Precision

The counter value for digital lock detect can be set.

D18	Function	Remarks
0	15 times Count	unlocked to locked
	3 times Count	locked to unlocked
1	31 times Count	unlocked to locked
	7 times Count	locked to unlocked


R[13:0] : Reference clock division number

The following settings can be selected for the reference clock division.

The allowed range is 1 (1/1 division) to 16383 (1/16383 division). 0 cannot be set.

The maximum frequency for F_{PFD} is 55MHz.

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1/1 division	
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1/2 division	
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1/3 division	
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1/4 division	
DATA															
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1/16381 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1/16382 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1/16383 division	



< Address1 : N Counter >

D[21:20]	D19	D[18:6]	D[5:0]	Address
0	CPGAIN	B[12:0]	A[5:0]	01

D21, D20 : These bits are set to the following for normal operation

D21	D20
0	0

CPGAIN : Sets the charge pump current

When {FAST[1:0]} is NOT "11Bin" :

D19	Function	Remarks
0	CP1 is enabled	
1	CP2 is enabled	

When {FAST[1:0]} is "11Bin" :

D19	Function	Remarks
0	CP1 is enabled	
1	CP2 is enabled during switchover time	Fast Lock Up Mode

B[12:0] : B (Programmable) counter value

D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	1	3 Dec	
DATA														
1	1	1	1	1	1	1	1	1	1	1	0	1	8189 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Dec	


A[5:0] : A (Swallow) counter value

D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	
0	0	0	0	0	1	1 Dec	
0	0	0	0	1	0	2 Dec	
0	0	0	0	1	1	3 Dec	
DATA							
1	1	1	1	0	1	61 Dec	
1	1	1	1	1	0	62 Dec	
1	1	1	1	1	1	63 Dec	

*** Requirements for A[5:0] and B[12:0]**

The data at A[5:0] and B[12:0] must meet the following requirements:

$$A[5:0] \geq 0, B[12:0] \geq 3, B[12:0] \geq A[5:0]$$

See "Frequency Setup" in section "Block Functional Descriptions" for details of the relationship between a frequency division number N and the data at A[5:0] and B[12:0].



< Address2 : Function >

D[21:20]	D19	D[18:16]	D[15:13]	D[12:9]	D[8:7]
PRE[1:0]	PD2	CP2[2:0]	CP1[2:0]	TIMER[3:0]	FAST[1:0]

D6	D5	D[4:2]	D1	D0	Address
CPHIZ	CPPOLA	LD[2:0]	PD1	CNTR_RST	02

PRE[1:0] : Selects a dividing ratio for the prescaler

The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 125MHz.

D21	D20	Function	Remarks
0	0	P=8, Dual modulus prescaler 8/9	
0	1	P=16, Dual modulus prescaler 16/17	
1	0	P=32, Dual modulus prescaler 32/33	
1	1	P=64, Dual modulus prescaler 64/65	

PD2, PD1 : Power Down Select

[PDN]	<Address2>		Function
	{PD2}	{PD1}	
"Low"	X	X	Power Down
"High"	X	0	Normal Operation
"High"	0	1	Asynchronous Power Down
"High"	1	1	Synchronous Power Down

X : Don't care ("0" is recommended)

{PD2}=1 and {PD1}=1 : All circuits powers down at the timing when the Phase detector frequency signal reverses.

{PD2}=0 and {PD1}=1 : All circuits goes into Power Down during the rise up of LE signal that latches "1" into {PD1}.

The registers can be written even in [PDN]=0.



CP2[2:0] : Charge pump current setting 2

CP1[2:0] : Charge pump current setting 1

AK1547 provides two setting for charge pump current. They can be set by {CP1} and {CP2}.

The following formula shows the relationship among the resistance value, the register setting and the electric current.

Charge pump minimum current (I_{cp_min})[A] = 17.46 / Resistance connected to the BIAS pin [Ω]

Charge pump current (I_{cp}) [A] = I_{cp_min} [A] \times ({CP1} or {CP2} setting +1)

The following table shows the typical I_{cp} for each status.

Icp (typical)						Remarks
D18	D17	D16	Bias Resistance			
D15	D14	D13	33 k Ω	27 k Ω	22 k Ω	
0	0	0	529	647	794	
0	0	1	1058	1293	1587	
0	1	0	1587	1940	2381	
0	1	1	2116	2587	3175	
1	0	0	262.7	3233	3968	
1	0	1	3175	3880	4762	
1	1	0	3704	4527	5555	
1	1	1	4233	5173	6349	

[Unit : μ A]

TIMER[3:0] : Sets the switchover time for CP2-to-CP1

This is enabled when {FAST[1:0]} is "11Bin" and {[CPGAIN]= "1".

The charge pump current is set into value {CP2[2:0]} designate during switchover time. It goes to be {CP1[2:0]} setting value after the time out.

The following formula shows the relationship between the switchover time and the counter value.

$$\text{Switchover time} = 1 / F_{\text{PFD}} \times \text{Counter Value}$$

$$\text{Counter Value} = 3 + \text{Timer}[3:0] \times 4$$



The following table shows the relationship between counter value and {TIMER[3:0]}.

D12	D11	D10	D9	Function	Remarks
0	0	0	0	3 Counts	
0	0	0	1	7 Counts	
0	0	1	0	11 Counts	
0	0	1	1	15 Counts	
0	1	0	0	19 Counts	
0	1	0	1	23 Counts	
0	1	1	0	27 Counts	
0	1	1	1	31 Counts	
1	0	0	0	35 Counts	
1	0	0	1	39 Counts	
1	0	1	0	43 Counts	
1	0	1	1	47 Counts	
1	1	0	0	51 Counts	
1	1	0	1	55 Counts	
1	1	1	0	59 Counts	
1	1	1	1	63 Counts	

FAST[1:0] : Enables or disables the Fast Lock mode

When {FAST[1:0]} is "11Bin", {CPGAIN} of function latch is the Fast Lock mode bit. When Fast Lock is enabled, charge pump current is set to the value of {CP2} setting during the switchover time under the control of the timer counter. After the timeout, {CPGAIN} is reset into "0" and charge pump current goes to be {CP1} setting value.

D8	D7	{CPGAIN}	Function	Remarks
X	0	0	CP1 is enabled	
		1	CP2 is enabled	
0	1	0	CP1 is enabled	
		1	CP2 is enabled	
1	1	0	CP1 is enabled	
		1	CP2 is enabled during switchover time	Fast Lock Up Mode. {CPGAIN} is reset to "0" after timeout.

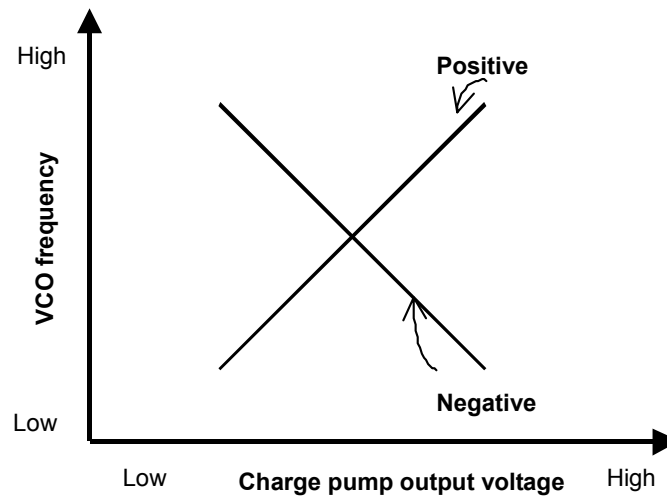
CPHIZ : TRI-STATE output setting for charge pump

D6	Function	Remarks
0	Charge pumps are activated.	Use this setting for normal operation.
1	TRI-STATE	Note 1)

Note 1) The charge pump output is turned OFF and put in the high-impedance (Hi-Z) state.

CPPOLA : Selects positive or negative output polarity for CP1 and CP2

D5	Function	Remarks
0	Negative	
1	Positive	


LD : Selects output from [LD] pin

D4	D3	D2	Function	Remarks
0	0	0	DVSS	
0	0	1	Digital lock detect	
0	1	0	N divider output	
0	1	1	DVDD	
1	0	0	R divider output	
1	0	1	Analog lock detect	Open Drain
1	1	0	DVSS	
1	1	1	DVSS	

**CNTR_RST : Counter Reset**

D0	Function	Remarks
0	Normal operation	
1	R and N counters are reset.	

< Address3 : Initialization >

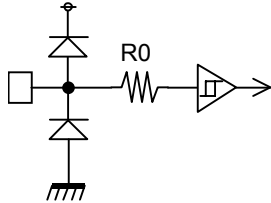
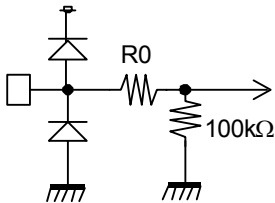
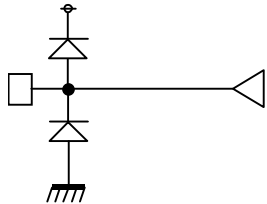
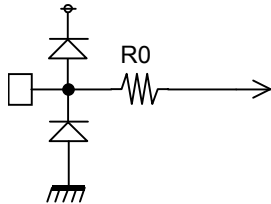
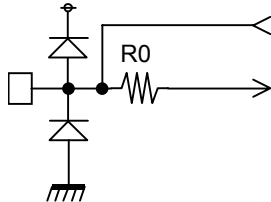
This function is same as <Address2>.

When this register is accessed, the following occurs :

- Address2 is loaded.
- An internal pulse resets the R counter, N counter and {TIMER} settings to load-state conditions, and also charge pump to Tri-state.
- Writing Address1 activates the R and N counter, {TIMER} and charge pump. {TIMER} is enabled when {FAST}="11Bin" and {CPGAIN}="1".



11. IC Interface Schematic

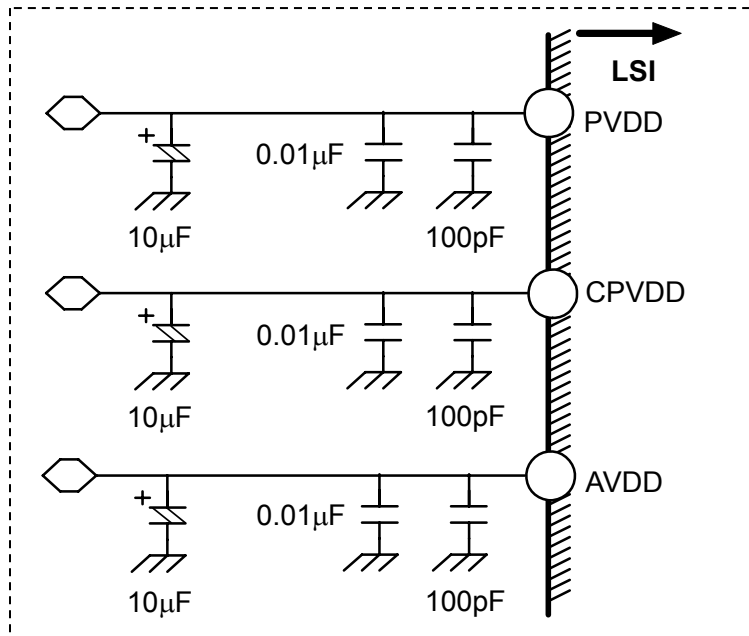
No.	Pin name	I/O	R0(Ω)	Cur(μA)	Function
11	PDN	I	300		Digital input pin 
12	CLK	I	300		
13	DATA	I	300		
14	LE	I	300		
2	TEST1	I	300		Digital input pin (Pull-Down) 
10	TEST2	I	300		
15	LD	O			Digital output pin 
8	REFIN	I	300		Analog input pin 
19	BIAS	IO	300		Analog input/output pin 



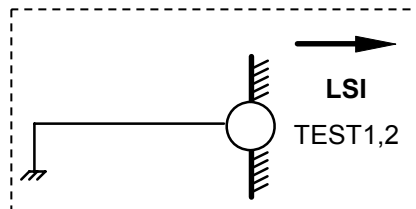
No.	Pin name	I/O	R0(Ω)	Cur(μA)	Function
20	CP	O			<p>Analog output pin</p>
4	RFINN	I	12k	20	<p>Analog input pin (RF input pin)</p>
5	RFINP	I	12k	20	

12. Recommended Connection Schematic of Off-Chip Component

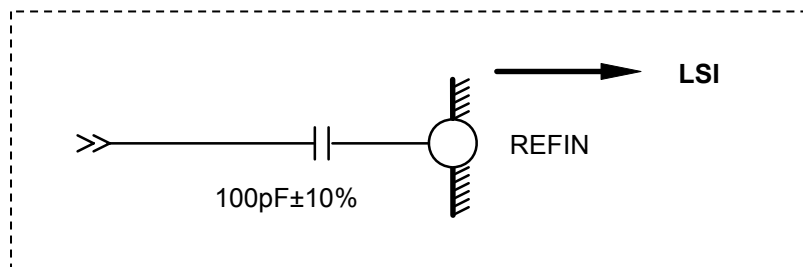
1. Power Supply Pins



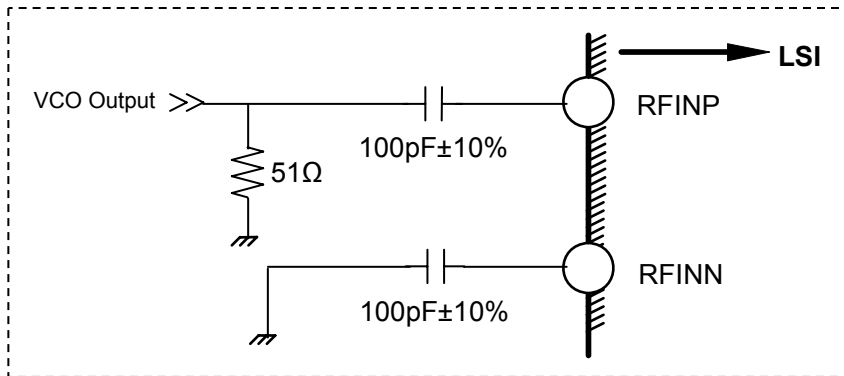
2. TEST1, TEST2



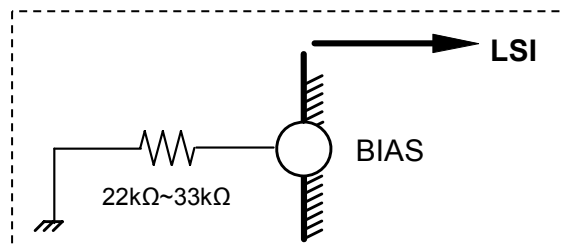
3. REFIN



4. RFINP, RFINN

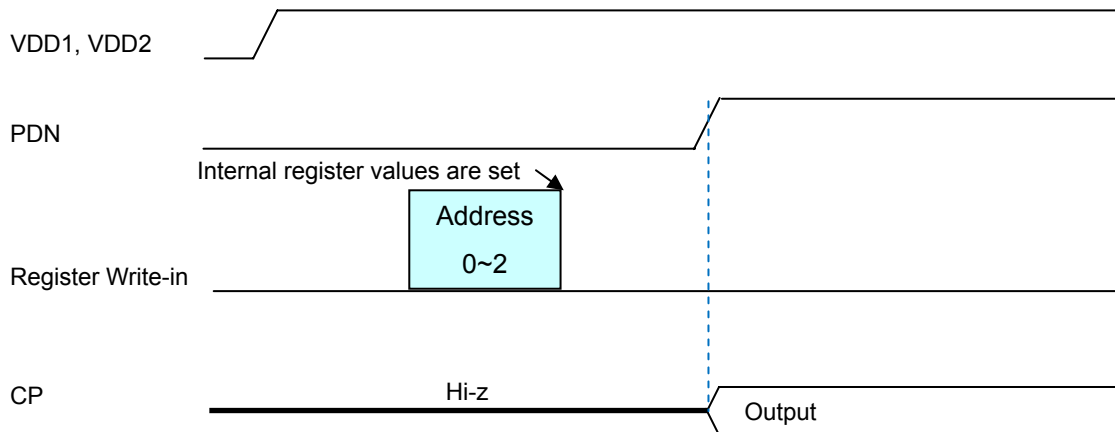


5. BIAS



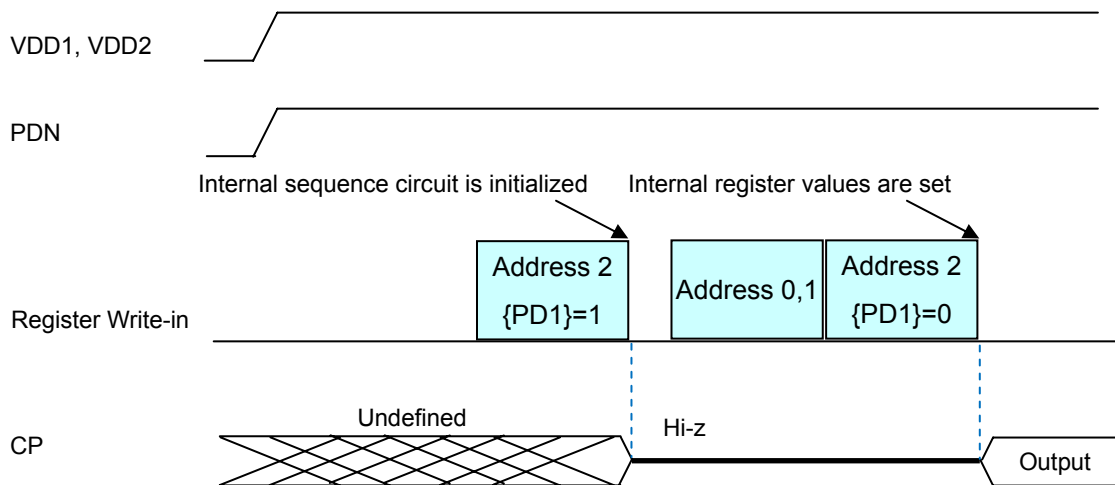


13. Power-Up Timing Chart (Recommended Flow)



Note1) After VDD1 and VDD2 is powered up, the initial setting of registers is undefined. It is required to write in Address0, 1 and 2.

Fig. 10 Power Up Sequence (Recommended)



Note2) When VDD1,VDD2 and PDN are synchronously powered up, internal sequence circuit is not initialized. So the circuit starts working on undefined status. Therefore, register {PD1} must be set to "1" before register setting.

Fig. 11 Power Up Sequence (VDD1/VDD2/PDN synchronous power-up)

14. Frequency Setting Timing Chart (Recommended Flow)

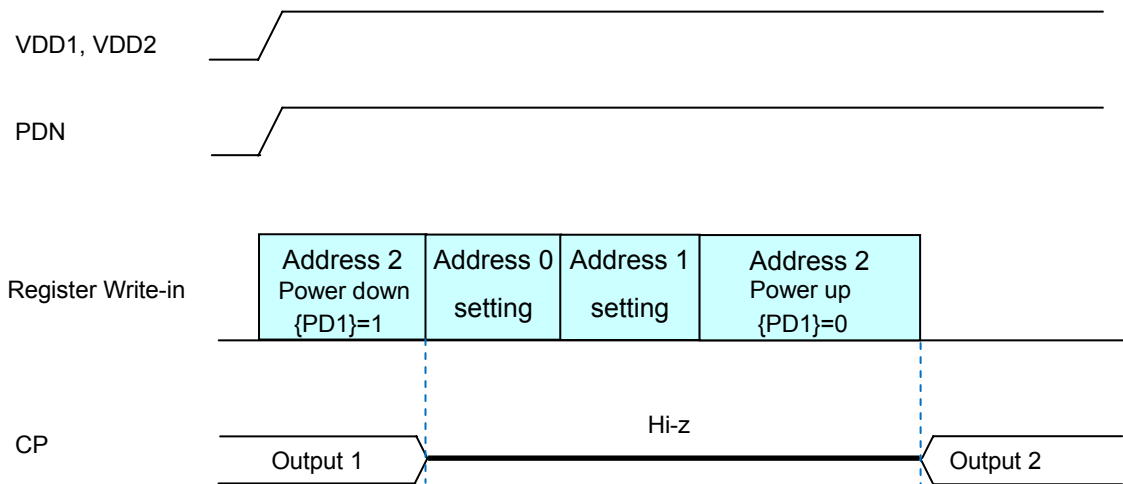


Fig. 102 Frequency settings (controlled by {PD1})

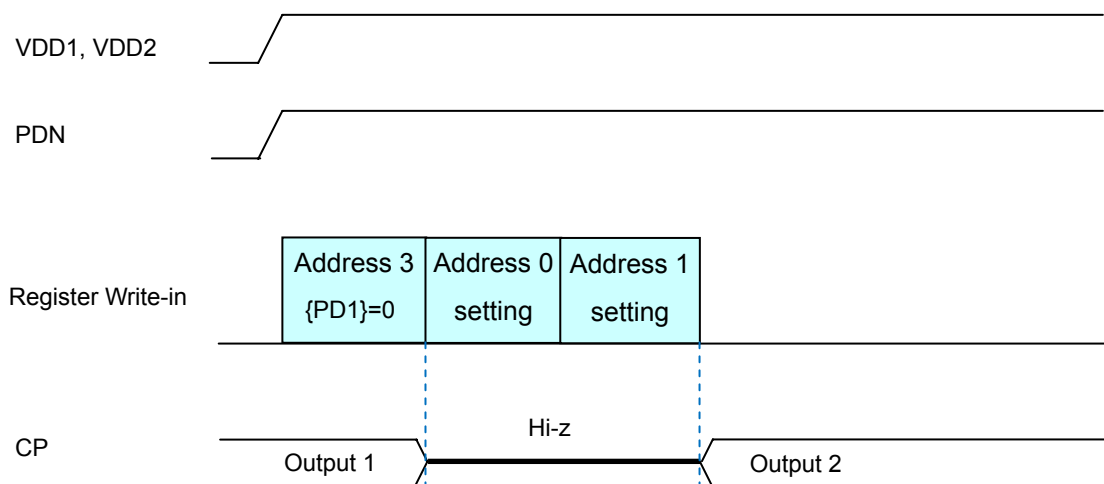


Fig. 113 Frequency settings (controlled by INITIAL register)

注) The function of Address3 is the same as Address2. Before writing in Address3, be sure to set {PD1}=0. Access to Address3 resets CP to Hi-Z, then set Address0 and 1. Access to Address1 restarts CP to operating.



15. Typical Evaluation Board Schematic

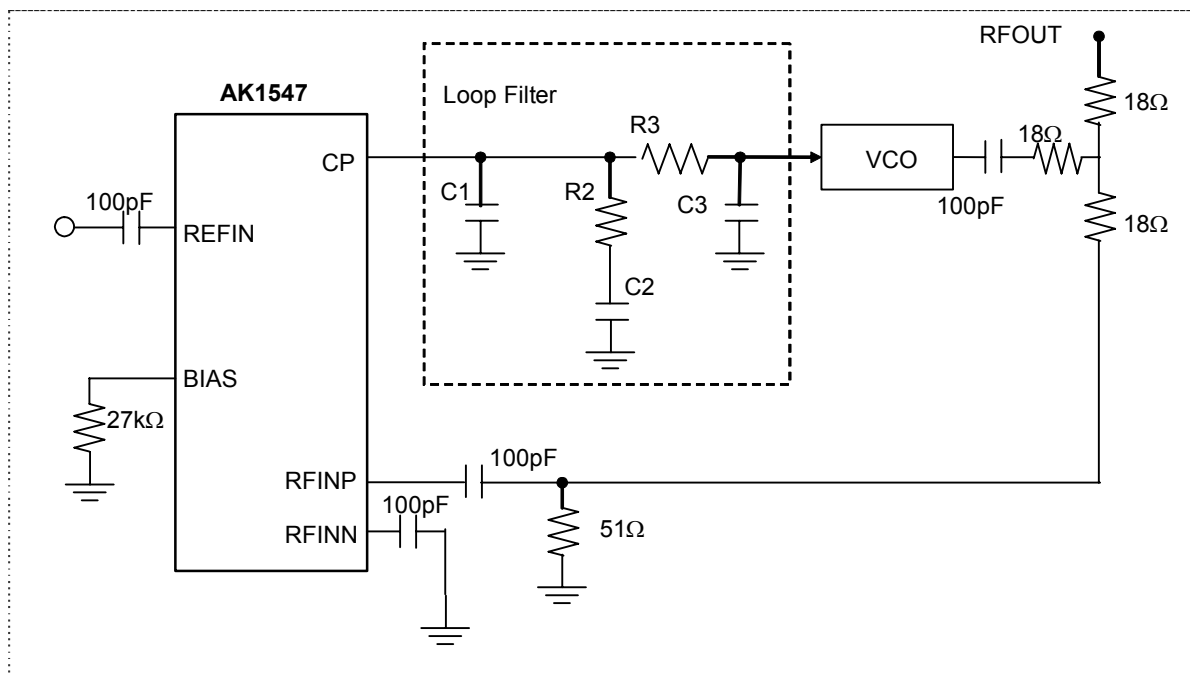


Fig. 124 Typical Evaluation Board Schematic

- Note1) Although it is no problem that both of [TEST1] and [TEST2] are open, it is recommended that they should be connected to ground.
- Note2) Although it is no problem that exposed pad at the center of the backside is open, it is recommended that it should be connected to ground.



16. Outer Dimensions

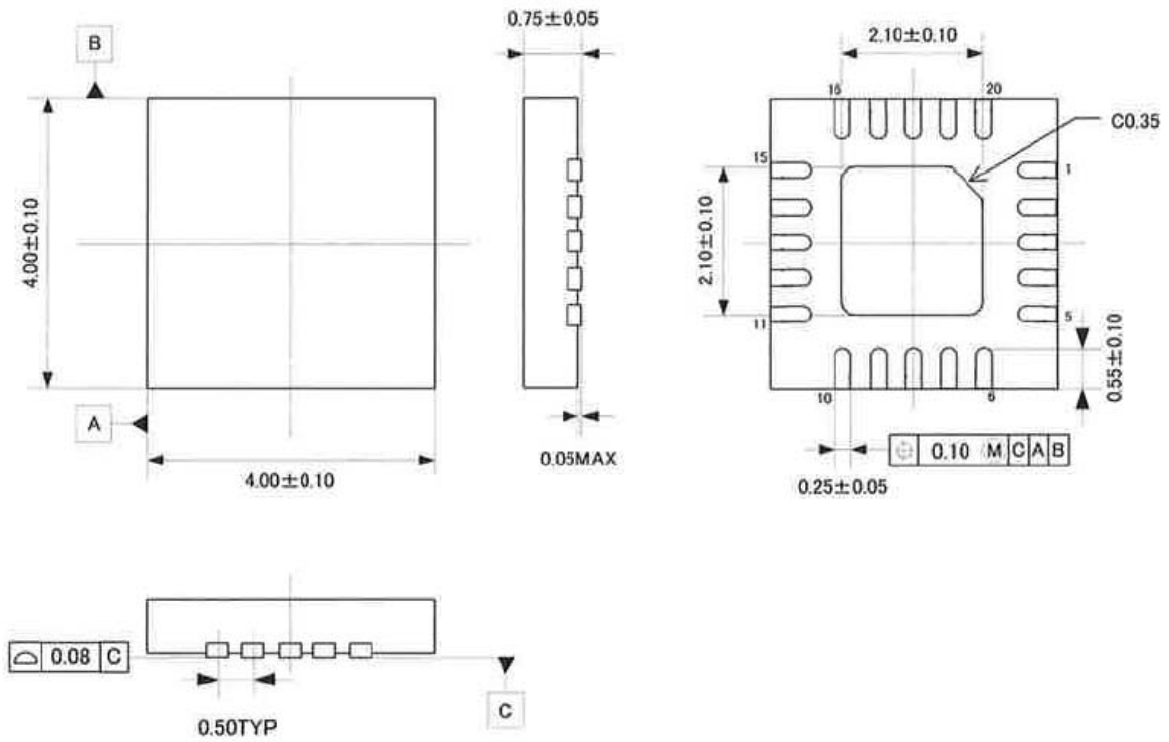
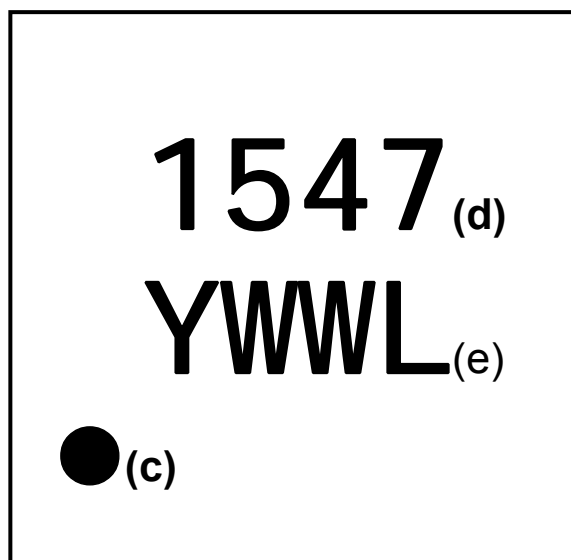


Fig. 135 Outer Dimensions



17. Marking

- a. Style : QFN
- b. Number of pins : 20
- c. A1 pin marking : ●
- d. Product number : 154 7
- e. Date code : YWWL (4 digits)
- Y : Lower 1 digit of calendar year
(Year 2012-> 2, 2013-> 3 ...)
- WW : Week
- L : Lot identification, given to each product lot which is made in a week
(A, B, C...)
→ LOT ID is given in alphabetical order





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