AK1573/AK1573B/AK1573C

Frequency Synthesizer with Integrated VCO

1. General Description

AK1573 is the Integer-N frequency synthesizer with integrated VCO (Voltage Controlled Oscillator). It is composed of programmable charge pump, reference divider, programmable divider, dual modulus prescaler (P / P + 1). With the feature of high-performance, low noise and small size, it can be used as a local signal source of a variety of frequency conversion.
By combining with an external loop filter, AK1573 form a complete Phase Locked Loop.
Access to the register is controlled by the serial interface of the 3-wire and Power supply voltage is 2.7V to 3.3V.

2. Features

- □ Normalized Phase Noise: -223dBc/Hz
- □ Low Noise Integrated VCO: -86dBc/Hz@10kHz, -112dBc/Hz@100kHz
- □ Operating Supply Voltage: 2.7 to 3.3V
- □ Low Current Comsumption@0dBm Output
  - AK1573 43mA
  - AK1573B 44mA
  - AK1573C 46mA
- □ Programmable to Divide by: 1, 2, 4, 8, 16, 32, 64
- □ Programmable Output Power: -12dBm to +6dBm
- □ Fast Lock-up Function
- □ Analog or Digital Lock Detect Function
- □ Output Mute Function
- □ Package: 24pin QFN (0.5mm pitch 4x4mm)
- □ Operating Temperature Range: -40 ºC to 85 ºC
- □ Frequency Coverage Options

	AK1573	AK1573B	AK1573C
VCO Frequency [MHz]	1480 to 2240	1728 to 2600	2100 to 3000
Divide by 1	1480 to 2240	1728 to 2600	2100 to 3000
Divide by 2	740 to 1120	864 to 1300	1050 to 1500
Divide by 4	370 to 560	432 to 650	525 to 750
Divide by 8	185 to 280	216 to 325	262.5 to 375
Divide by 16	92.5 to 140	108 to 162.5	131.25 to 187.5
Divide by 32	46.25 to 70	54 to 81.25	65.625 to 93.75
Divide by 64	30 to 35	30 to 40.625	32.8125 to 46.875

3. Ordering Guide

- AK1573	24-pin QFN (4.0mm x 4.0mm, 0.5mm pitch)
- AK1573B	24-pin QFN (4.0mm x 4.0mm, 0.5mm pitch)
- AK1573C	24-pin QFN (4.0mm x 4.0mm, 0.5mm pitch)
- AKD1573	AK1573 Evaluation Board
- AKD1573B	AK1573B Evaluation Board
- AKD1573C	AK1573C Evaluation Board

4. Applications

- □ Public safety and Community/Emergency Wireless System
- □ Wireless applications
- □ Cellular BTS

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6. Block Diagram and Functions

6.1. Block Diagram

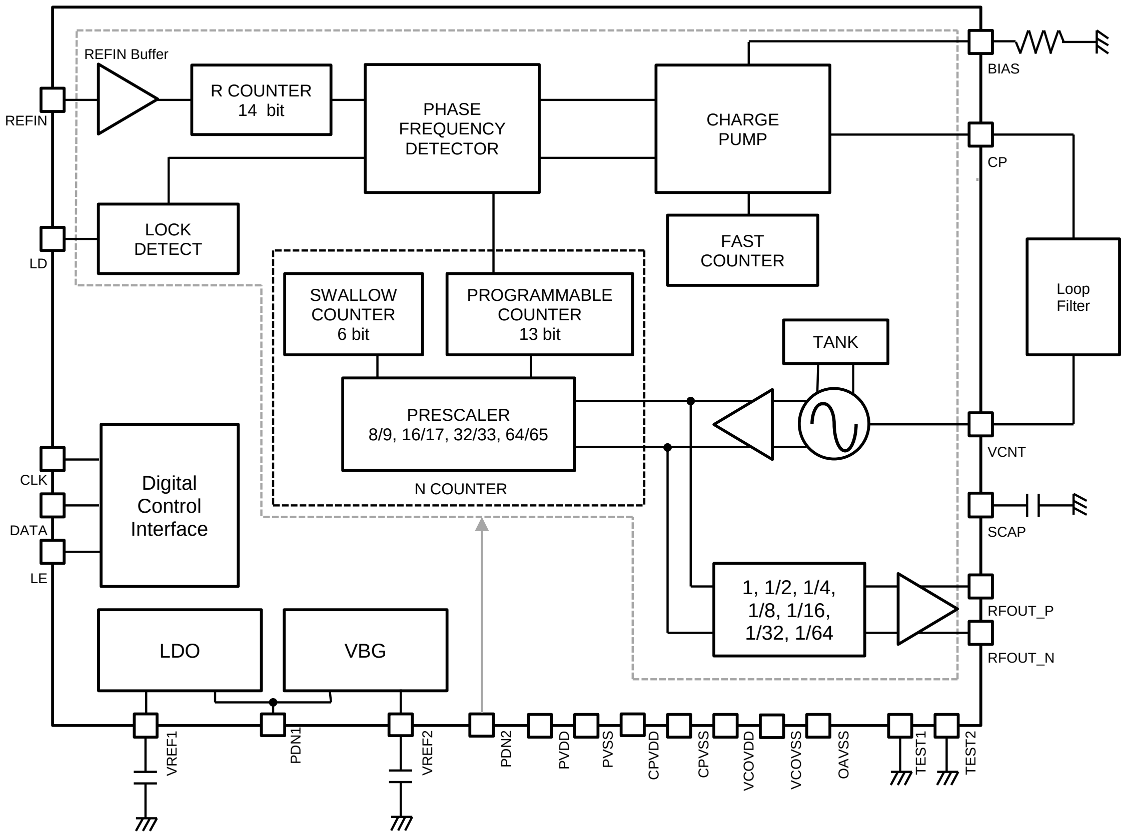


Figure.1 Block Diagram

6.2. Functions

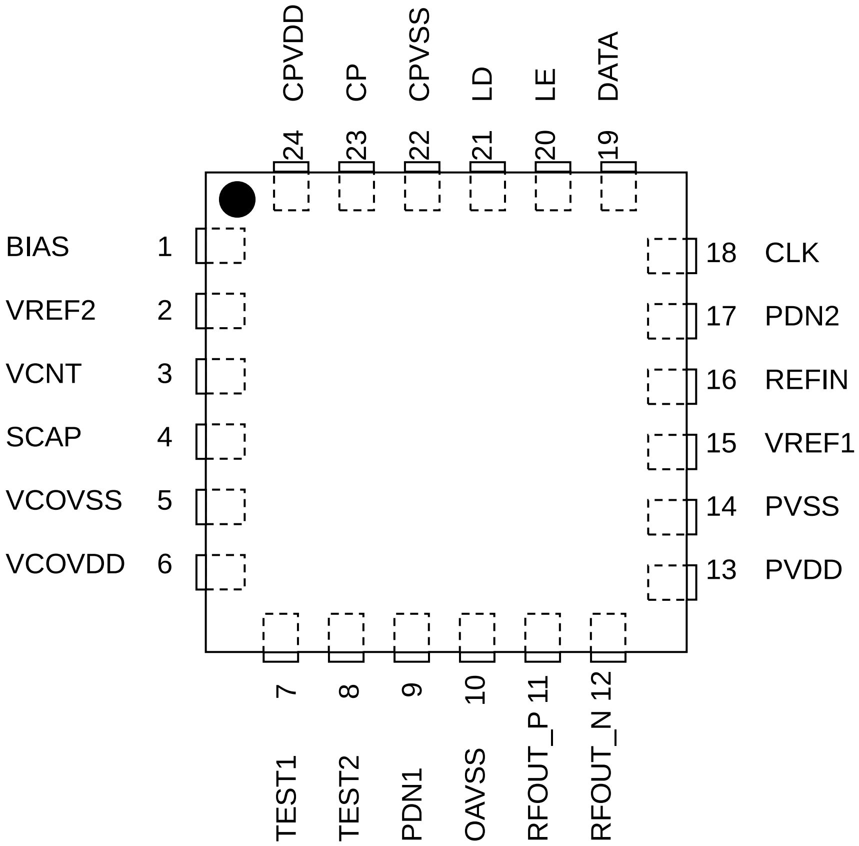
Block	Function
N counter	It is composed of prescaler, Swallow Counter and Programmable Counter. VCO output signal is divided by N and passed to phase frequency detector (PFD).
VCO Divider	It divides VCO output signal and passes it to output buffer. Dividing ratio of 1, 2, 4, 8, 16, 32 and 64 can be selected.
R counter	It divides a reference signal by R and passes it to phase frequency detector (PFD).
VCO (Voltage Controlled Oscillator)	It generates a signal of the frequency corresponding to a voltage inputted to VCNT pin.
PFD(Phase Frequency Detector)	It outputs a signal corresponding to phase difference between N counter and R counter.
Charge Pump	Sweep or pull-in a current corresponding to a signal from PFD.

7. Pin Configurations and Functions

No.	Pin Name	I/O	Pin function	Power Down	Description
1	BIAS	AI	Charge pump current setting pin		Connect a 27kΩ resistor to the ground
2	VREF2	AO	Internal reference voltage output pin	"L"	Connect a 470nF capacitor to the ground
3	VCNT	AI	VCO control voltage input pin		
4	SCAP	AO	VCO Bias stabilizing connection pin	"L"	Connect a 100pF capacitor to the ground
5	VCOVSS	G	Ground of VCO block		
6	VCOVDD	P	Power supply of VCO block		
7	TEST1	DI	TEST1 pin Connect to the ground		Pull Down Schmitt trigger input
8	TEST2	DI	TEST2 pin Connect to the ground		Pull Down Schmitt trigger input
9	PDN1	DI	Power down 1 pin. When PDN1 = "L", device is powered down and the registers are not retained.		Schmitt trigger input
10	OAVSS	G	Ground of Local buffer		
11	RFOUT_P	AO	Local signal output pin		Open collector Connect a inductor and a register to VDD
12	RFOUT_N	AO	Local signal complementary output pin		
13	PVDD	P	Power supply of Prescaler and LDO		
14	PVSS	G	Ground of Prescaler and LDO		
15	VREF1	AO	Output pin of LDO	"L"	Connect a 220nF capacitor to the ground
16	REFIN	DI	Reference signal input pin		
17	PDN2	DI	Power down 2 pin. When PDN2 = "L", all blocks except LDO and VBG are powered down but the registers are retained		Schmitt trigger input
18	CLK	DI	Serial clock input pin.		Schmitt trigger input
19	DATA	DI	Serial data input pin.		Schmitt trigger input
20	LE	DI	Load enable input pin.		
21	LD	DO	Lock detect output pin	"L"	
22	CVPSS	G	Ground of Charge Pump		
23	CP	AO	CP signal output pin	Tri-State	
24	CPVDD	P	Power supply of Charge Pump		

AI: Analog input pin AO: Analog output pin AIO: Analog I/O pin
DI: Digital input pin DO: Digital output pin P: Power supply pin G: Ground pin

* "Power Down" means the state in which power supply is applied and PDN1 / PDN2 pins = "L".
* The exposed pad at the center of the backside should be connected to the ground



24-pin QFN (0.5mm pitch, 4mm × 4mm)

Figure.2 Package pin layout (Top view)

8. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Description
Supply Voltage	VDD	-0.3	3.6	V	* 1, 2
Ground Level	VSS	0	0	V	* 3
Analog input voltage	VAIN	VSS-0.3	VDD+0.3	V	* 1, 4, 6
Digital input voltage	VDIN	VSS-0.3	VDD+0.3	V	* 1, 5, 6
Input current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	125	°C	

Note
* 1. All voltage reference ground level: 0V
* 2. Applied to the VCOVDD / PVDD / CPVDD pins
* 3. Applied to the CPVSS / PVSS / VCOVSS / OAVSS pins
* 4. Applied to the VCNT / REFIN pins
* 5. Applied to the CLK / DATA / LE / PDN1 / PDN2 / TEST1 / TEST2 pins
* 6. The maximum value must not exceed the absolute maximum rating of 3.6V.

Exceeding these maximum ratings may result in damage to the AK1573. Normal operation is not guaranteed at these extremes.

9. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD	2.7	3.0	3.3	V	Applied to the VCOVDD / PVDD / CPVDD pins

10. Electrical Characteristics

10.1. Digital DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Description
High level input voltage	Vih		0.8×VDD			V	* 1.
Low level input voltage	Vil				0.2×VDD	V	* 1.
High level input current 1	Iih1	Vih = VDD=3.3V	-1		1	μA	* 2
High level input current 2	Iih2	Vih = VDD=3.3V	16.5	33	66	μA	* 3
Low level input current	Iil	Vil = 0V, VDD=3.3V	-1		1	μA	* 1
High level output voltage	Voh	Ioh = -500μA	VDD-0.4			V	* 4
Low level output voltage	Vol	Iol = 500μA			0.4	V	* 4

Note
* 1. Applied to the CLK / DATA / LE / PDN1 / PDN2 pins
* 2. Applied to the CLK / DATA / LE / PDN1 / PDN2 pins
* 3. Applied to the TEST1 / TEST2 pins
* 4. Applied to the LD pin

10.2. Serial Interface Timing

<Write-In Timing>

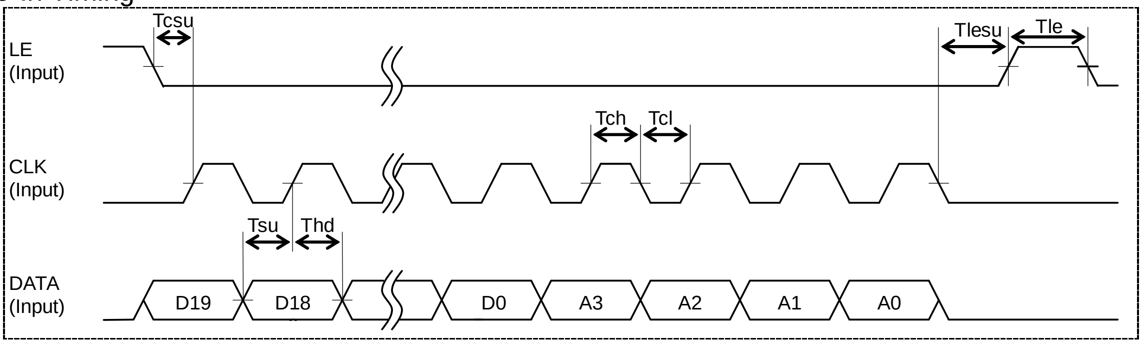


Figure.3 Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Clock L level hold time	Tcl	25			ns	
Clock H level hold time	Tch	25			ns	
Clock setup time	Tcsu	10			ns	
Data setup time	Tsu	10			ns	
Data hold time	Thd	10			ns	
LE setup time	Tlesu	10			ns	
LE pulse width	Tle	25			ns	

10.3. Analog Circuit Characteristics

VDD=2.7 to 3.3V, -40°C<Ta<85°C, BIAS resistance =27kΩ unless otherwise specified.
The exposed pad at the center of the backside should be connected to the ground

Parameter		Min.	Typ.	Max.	Unit	Description
REFIN						
Input sensitivity		0.4		VDD	Vpp	REFIN frequency < 200MHz
		0.4		2	Vpp	REFIN frequency ≥ 200MHz
Input Frequency Range		10		300	MHz	
Maximum available prescaler output Frequency				300	MHz	Design guarantee value
Phase Frequency Detector(PFD)						
PFD Frequency				104	MHz	Design guarantee value
Charge Pump						
Maximum Charge Pump current			2800		μA	
Minimum Charge pump current			350		μA	
Icp TRI-STATE leak current			1		nA	Ta = 25°C, Vcpo = VDD / 2 Vcpo : CP pin voltage
Sink / Source current mismatch * 1			1	10	%	Vcpo = VDD / 2, Ta = 25°C Vcpo : CP pin voltage
Icp vs. Vcpo * 2			3	15	%	0.5 ≤ Vcpo ≤ VDD - 0.5 Ta = 25°C
VCO						
Operating Frequency Range		1480		2240	MHz	AK1573
		1728		2600	MHz	AK1573B
		2100		3000	MHz	AK1573C
VCO tuning Sensitivity			fvco×0.02		MHz/V	fvco : Oscillation Frequency
Phase Noise @ 1.6GHz (AK1573) @ 1.8GHz (AK1573B) @ 2.1GHz (AK1573C) OUTLV[2:0] bits ≥ "011"	10kHz offset		-86		dBc/Hz	VCOI bit = "1"
	100kHz offset		-112		dBc/Hz	VCOI bit = "1"
	1MHz offset		-133		dBc/Hz	VCOI bit = "1"
	10MHz offset		-151		dBc/Hz	VCOI bit = "1"
Normalized Phase Noise			-223		dBc/Hz	Note 3
Output Buffer						
OUTPUT Power @1GHz			6		dBm	OUTLV[2:0] bits = "111"
			3		dBm	OUTLV[2:0] bits = "101"
			1		dBm	OUTLV[2:0] bits = "011"
			-5		dBm	OUTLV[2:0] bits = "001"
Output Frequency		30			MHz	Design guarantee value
Regulator						
VREF1 start-up time				10	ms	

Note
* 1. Sink/Source current mismatch : [(|Isink|-|Isource|)/{(|Isink|+|Isource|)/2}] * 100 [%]
* 2. Icp v.s.Vcpo : [{1/2*(|I1|-|I2|)}/{1/2*(|I1|+|I2|)}]*100 [%]
* 3. Measured in-band phase noise with the loop locked. Normalized Phase Noise is calculated from following equation. REFIN frequency = 120MHz, F_{PFD} = 10MHz.

$(PN_{total} = PN_{synth} - 10 \log F_{PFD} - 20 \log N)$

PN_{total} : Normalized Phase Noise
PN_{synth} : In-band Phase Noise
F_{PFD} : PFD Frequency

Parameter	Min.	Typ.	Max.	Unit	Description
Current Consumption					
IDD1			10	μA	PDN1 pin = PDN2 pin = "L" (Full power down)
IDD2 @1.6GHz (AK1573)					PDN1 pin = PDN2 pin = "H" DIV[2:0] bits = “000” PRE[1:0] bits = “00”
@ OUTLV[2:0] bits = “001” VCOI bits = “0”		33		mA	
@ OUTLV[2:0] bits = “011” VCOI bits = “0”		43		mA	
@ OUTLV[2:0] bits = “111” VCOI bits = “0”		62		mA	
@ OUTLV[2:0] bits = “111” VCOI bits = “1”		66	93	mA	
IDD2 @1.8GHz (AK1573B)					
@ OUTLV[2:0] bits = “001” VCOI bits = “0”		34		mA	
@ OUTLV[2:0] bits = “011” VCOI bits = “0”		44		mA	
@ OUTLV[2:0] bits = “111” VCOI bits = “0”		62		mA	
@ OUTLV[2:0] bits = “111” VCOI bits = “1”		66	93	mA	
IDD2 @2.1GHz (AK1573C)					
@ OUTLV[2:0] bits = “001” VCOI bits = “0”		37		mA	
@ OUTLV[2:0] bits = “011” VCOI bits = “0”		46		mA	
@ OUTLV[2:0] bits = “111” VCOI bits = “0”		64		mA	
@ OUTLV[2:0] bits = “111” VCOI bits = “1”		68	93	mA	
IDD3 @1.6GHz (AK1573) @1.8GHz (AK1573B) @2.1GHz (AK1573C) DIV[2:0} bits ≥ “100”		75	105	mA	PDN1 pin = PDN2 pin = "H" DIV[2:0] bits ≠ “000” PRE[1:0] bits = “00”
IDD4		0.5	1	mA	PDN1 pin = "H", PDN2 pin = "L" (power down except VBG / LDO)
CP current adjusting resistance					
BIAS resistance	22	27	33	kΩ	Connect to BIAS pin

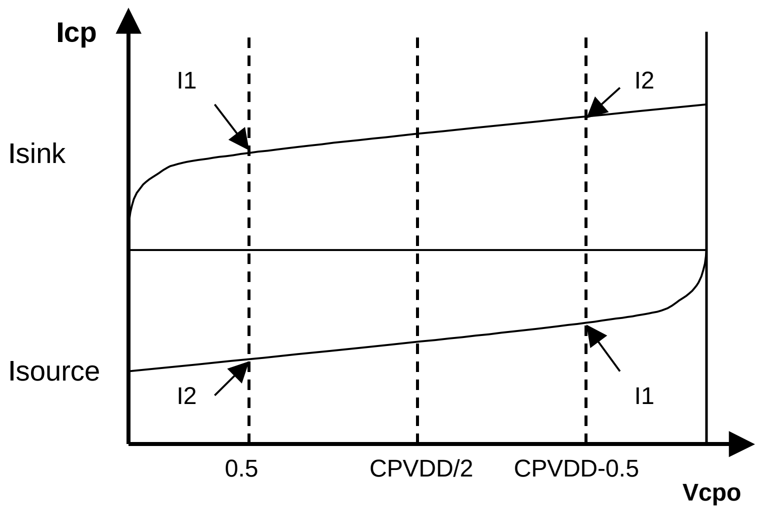


Figure.4 Charge Pump Characteristics – Voltage vs Current

10.4. Loop filter

Figure.5 shows loop filter topology used to evaluate AK1573, AK1573B and AK1573C.

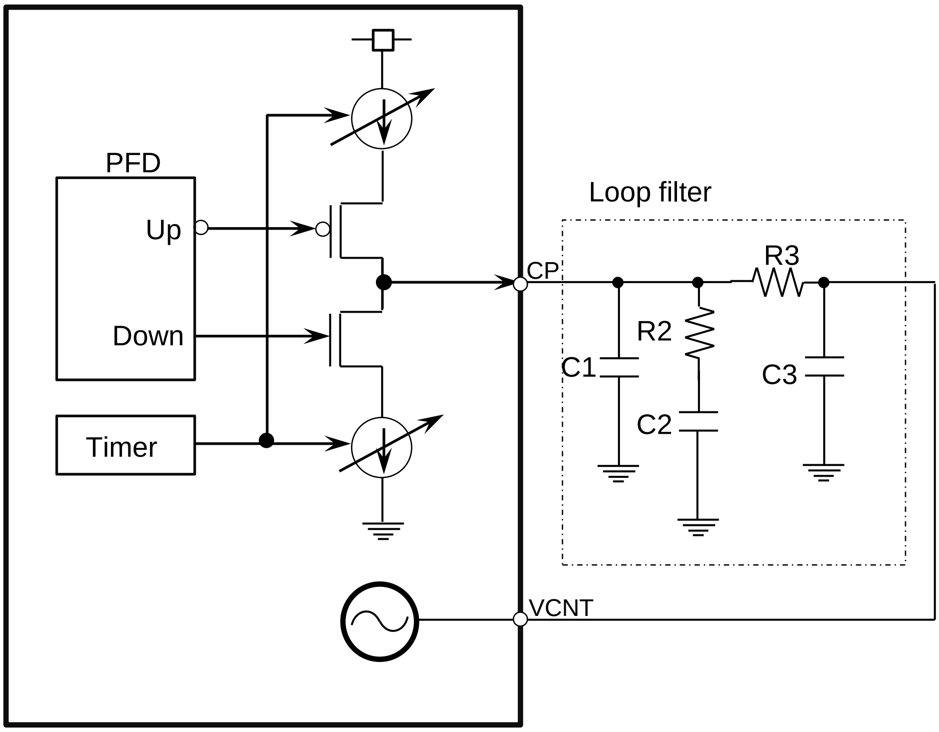


Figure.5 Loop Filter Schematic

11. Typical Characteristics

VDD=3.0V, Ta=25°C, BIAS resistance =27kΩ.

1. Analog Characteristics

AK1573

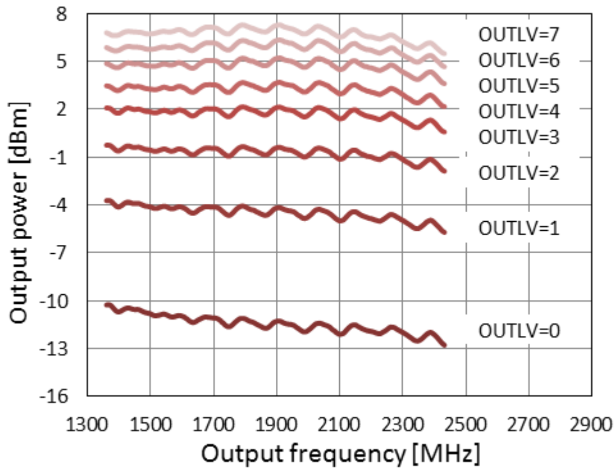
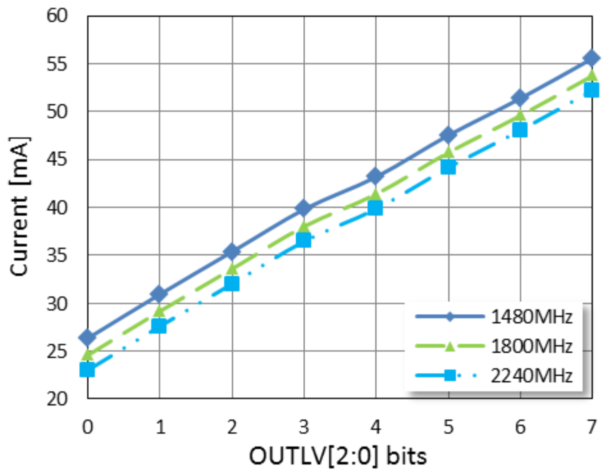
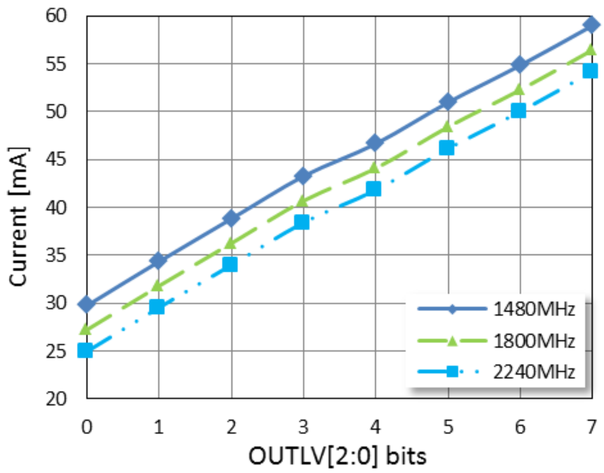


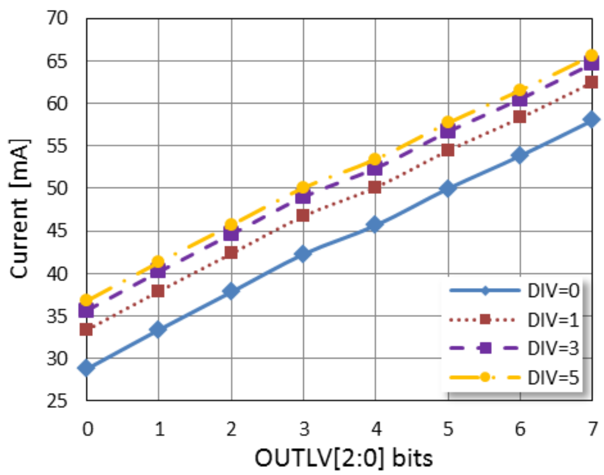
Figure.6 Output power vs. Output frequency



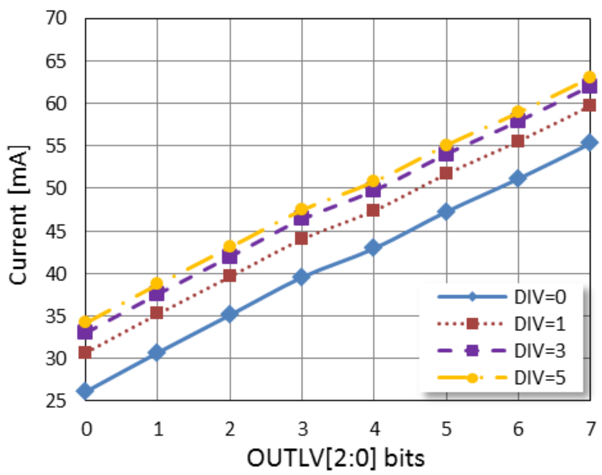
(a) VCOI bit = “0”, DIV[2:0] bits = “000”



(b) VCOI bit = “1”, DIV[2:0] bits = “000”



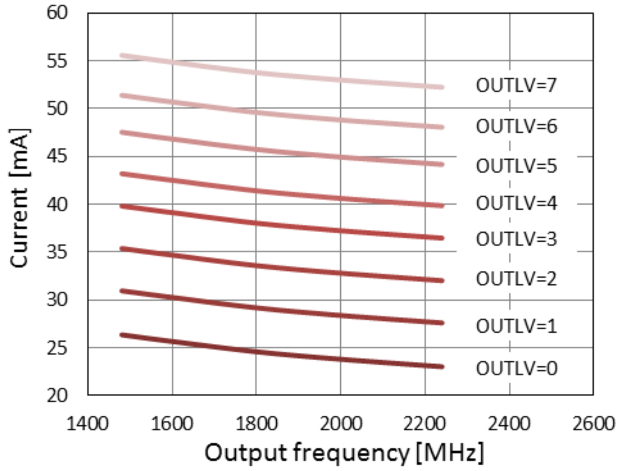
(c) Output frequency=1600MHz, VCOI bit=“1”



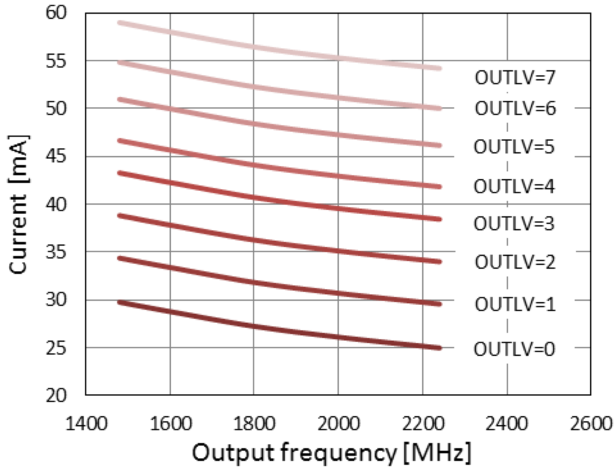
(d) Output frequency=2000MHz, VCOI bit=“1”

Figure.7 Current vs. OUTLV[2:0] bits

REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = “111”



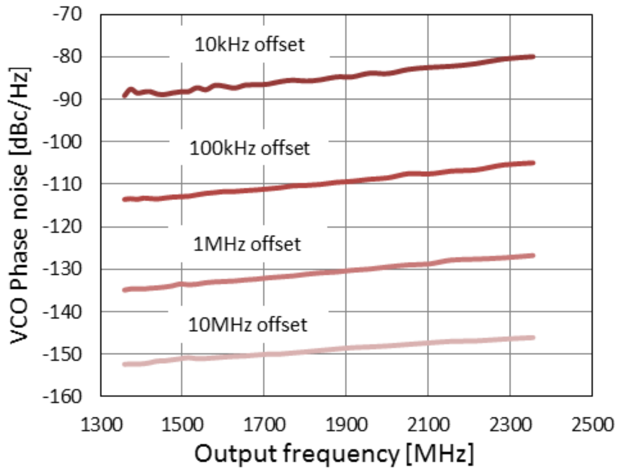
(a) VCOI bit = “0”



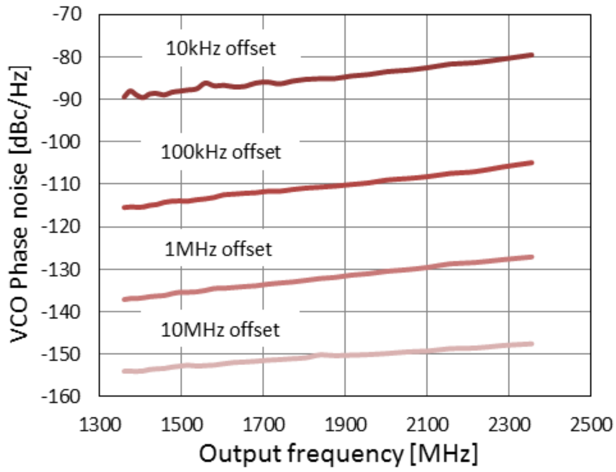
(b) VCOI bit = “1”

Figure.8 Current vs. Output frequency

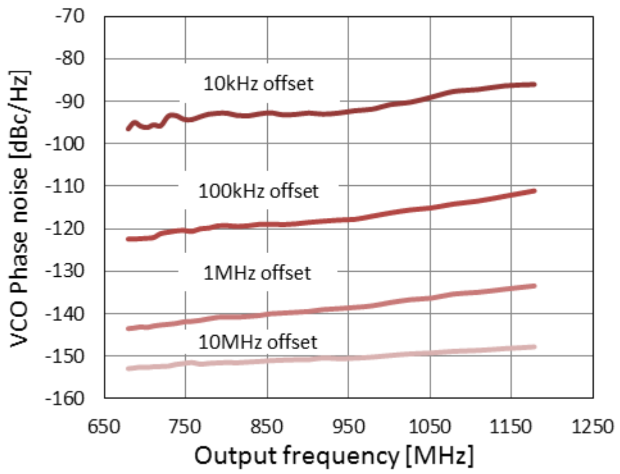
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = “111”, DIV[2:0] bits = “000”



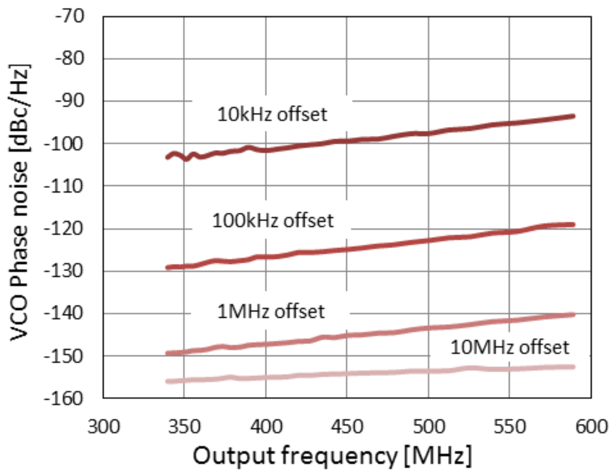
(a) VCOI bit = “0”, DIV[2:0] bits = “000”



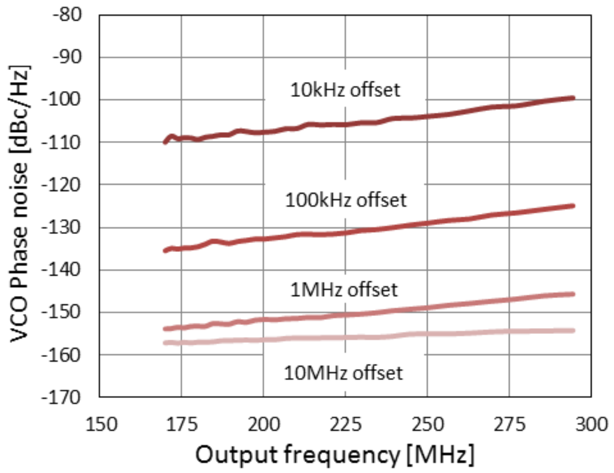
(b) VCOI bit = “1”, DIV[2:0] bits = “000”



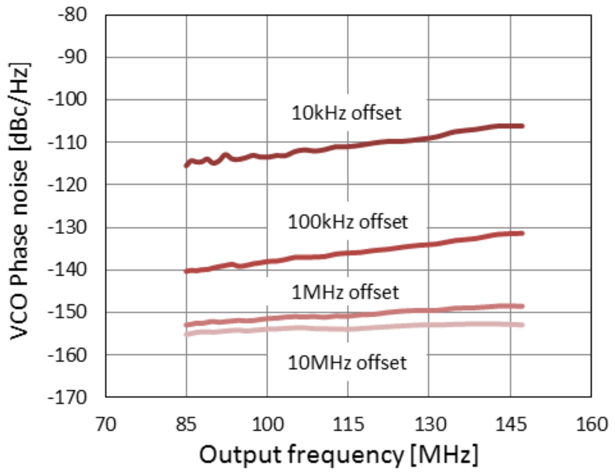
(c) VCOI bit = “1”, DIV[2:0] bits = “001”



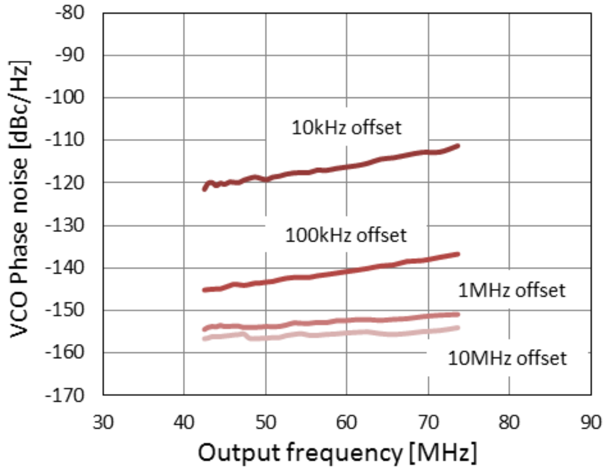
(d) VCOI bit = “1”, DIV[2:0] bits = “010”



(e) VCOI bit = “1”, DIV[2:0] bits = “011”



(f) VCOI bit = “1”, DIV[2:0] bits = “100”



(g) VCOI bit = “1”, DIV[2:0] bits = “101”

Figure.9 VCO Phase Noise vs. Output frequency
OUTLV[2:0] bits = “111”

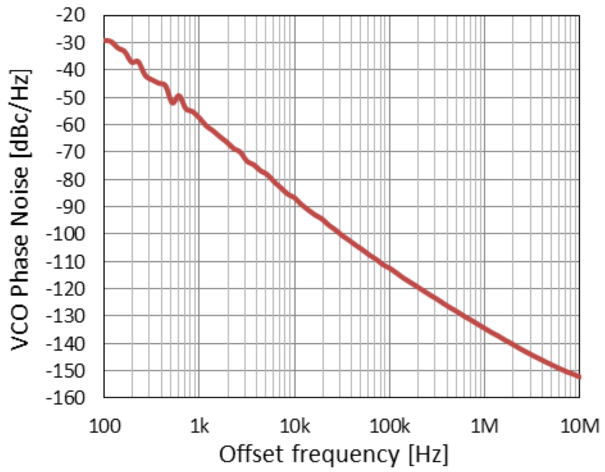


Figure.10 VCO Phase Noise vs. Offset frequency
Output frequency = 1602.8MHz, VCOI bit = “1”, OUTLV[2:0] bits = “111”

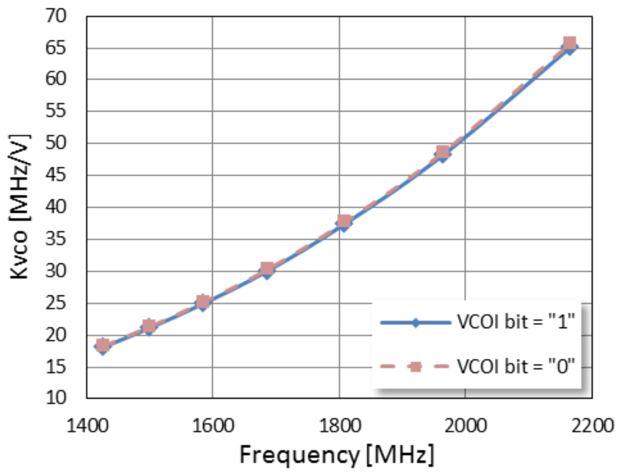


Figure.11 VCO Tuning Sensitivity

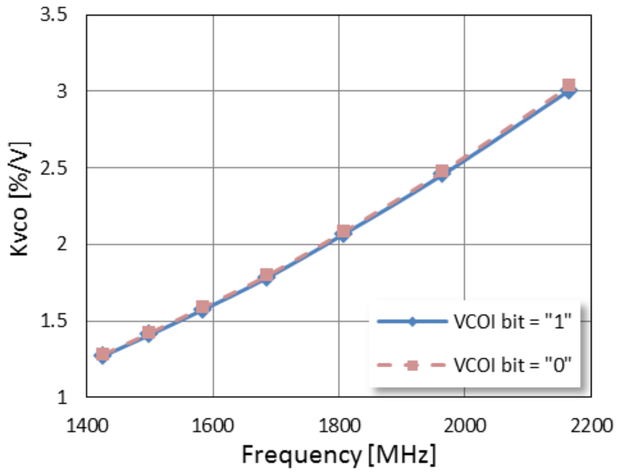
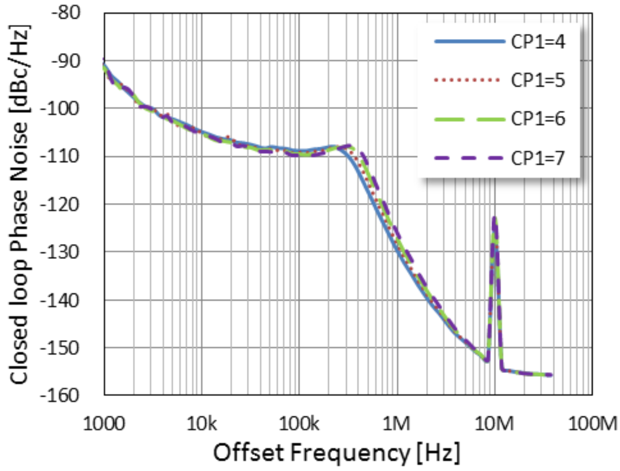
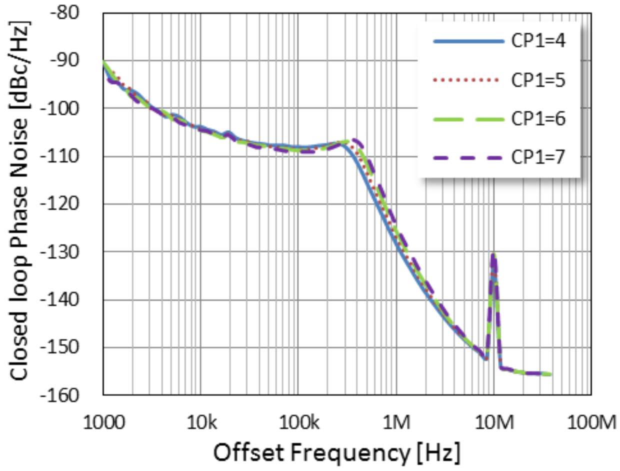


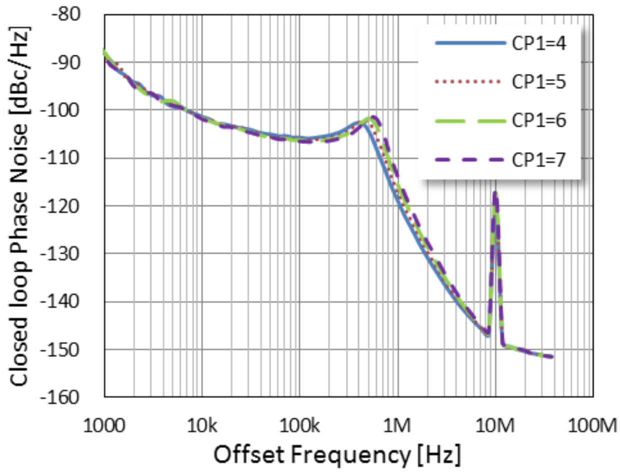
Figure.12 VCO Tuning Sensitivity



(a) Output frequency = 1500MHz



(b) Output frequency = 1600MHz



(c) Output frequency = 2100MHz

Figure.13 Closed loop Phase Noise
REFIN frequency = 120MHz, R counter = 12, Prescaler = 8/9
Loop Filter : C1 = 33pF, C2 = 1500pF, C3 = N/A, R2 = 10kΩ, R3 = 0Ω

AK1573B

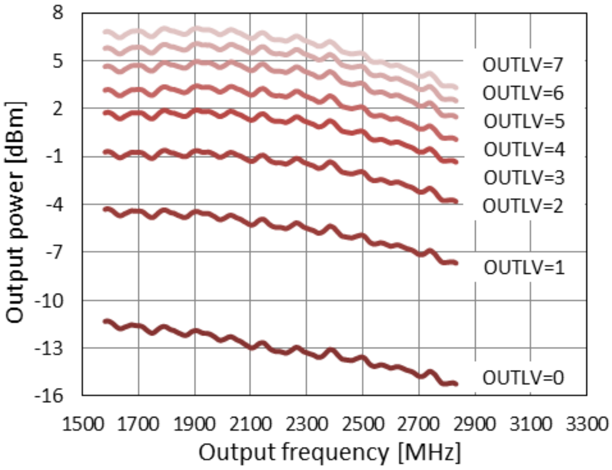
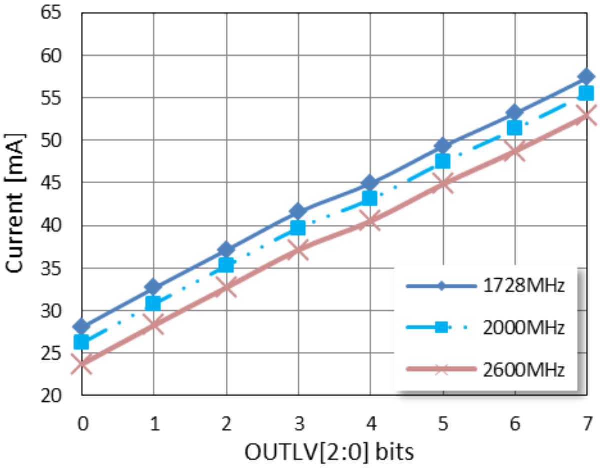
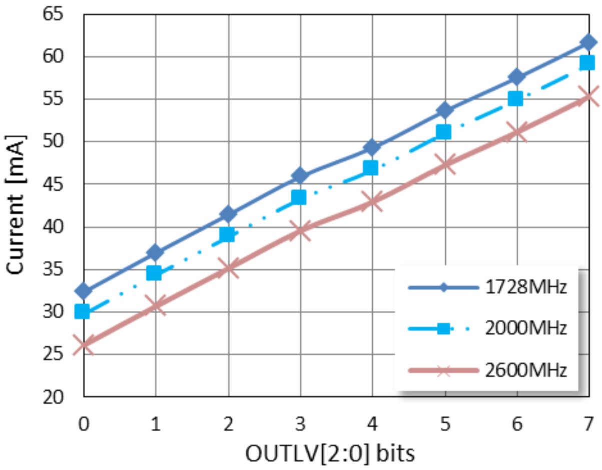


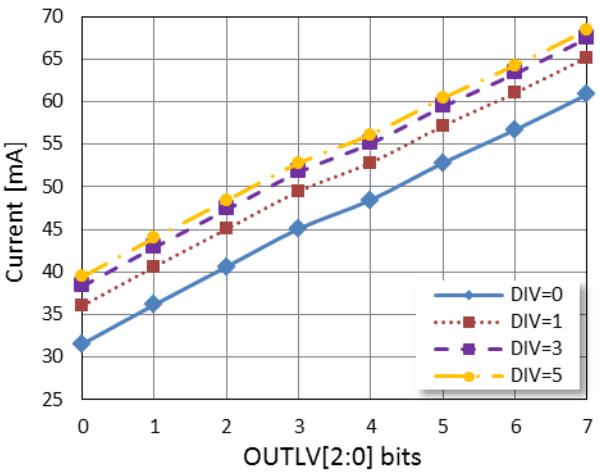
Figure.14 Output power vs. Output frequency



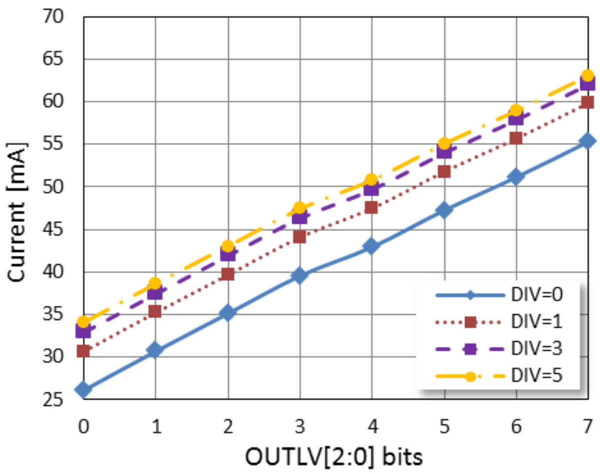
(a) VCOI bit = “0”, DIV[2:0] bits = “000”



(b) VCOI bit = “1” , DIV[2:0] bits = “000”

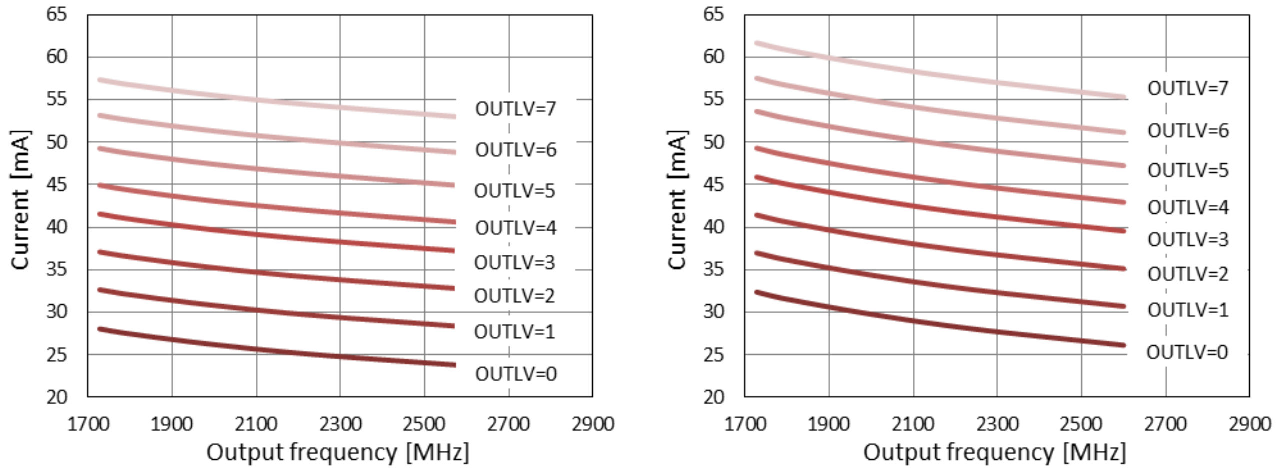


(c) Output frequency=1800MHz, VCOI bit=“1”



(d) Output frequency=2600MHz, VCOI bit=“1”

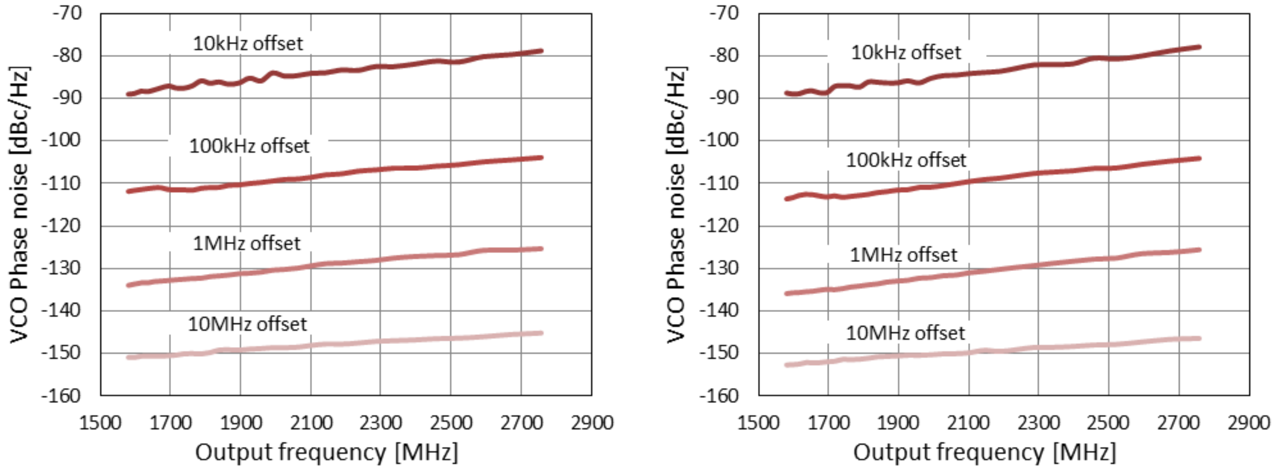
Figure.15 Current vs. OUTLV[2:0] bits
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = “111”



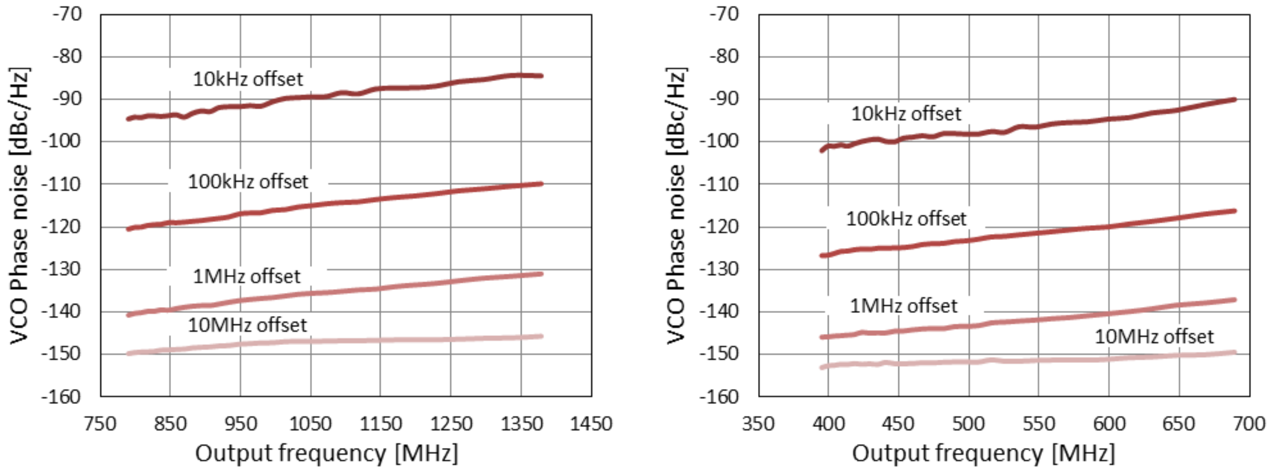
(a) VCOI bit = “0” (b) VCOI bit = “1”

Figure.16 Current vs. Output frequency

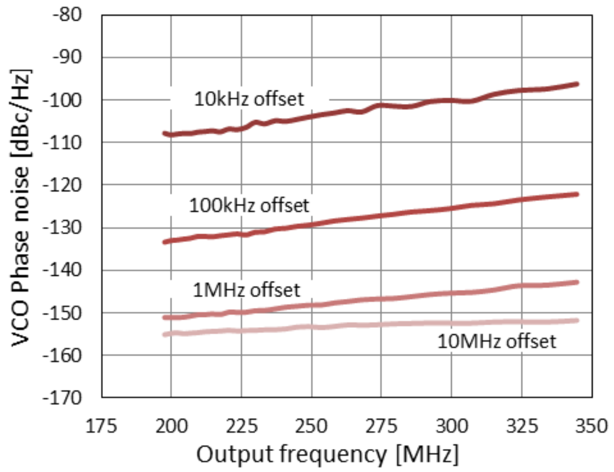
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = “111”, DIV[2:0] bits = “000”



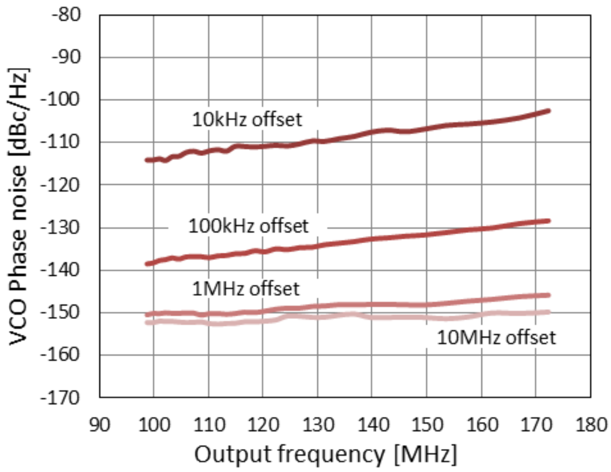
(a) VCOI bit = “0”, DIV[2:0] bits = “000” (b) VCOI bit = “1”, DIV[2:0] bits = “000”



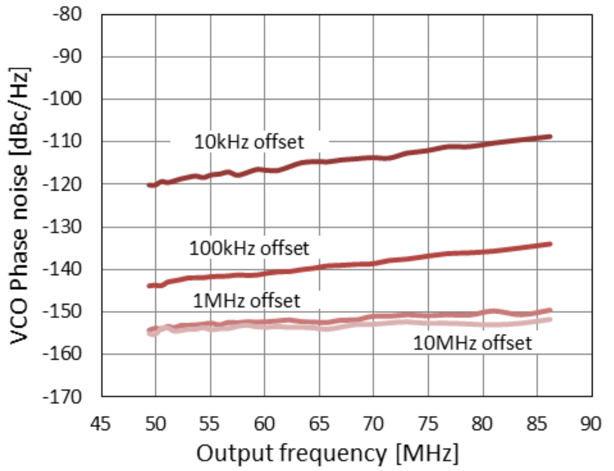
(c) VCOI bit = “1”, DIV[2:0] bits = “001” (d) VCOI bit = “1”, DIV[2:0] bits = “010”



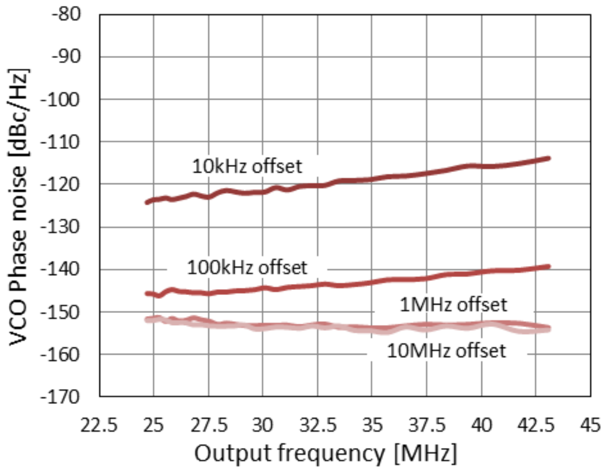
(e) VCOI bit = “1”, DIV[2:0] bits = “011”



(f) VCOI bit = “1”, DIV[2:0] bits = “100”



(g) VCOI bit = “1”, DIV[2:0] bits = “101”



(h) VCOI bit = “1”, DIV[2:0] bits = “110”

Figure.17 VCO Phase Noise vs. Output frequency
OUTLV[2:0] bits = “111”

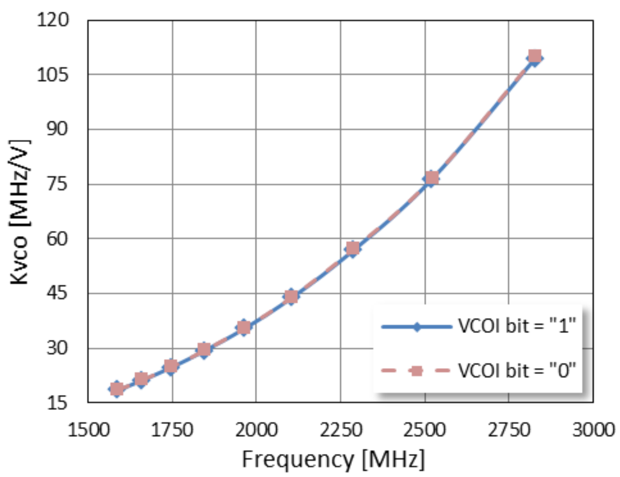


Figure.18 VCO Tuning Sensitivity

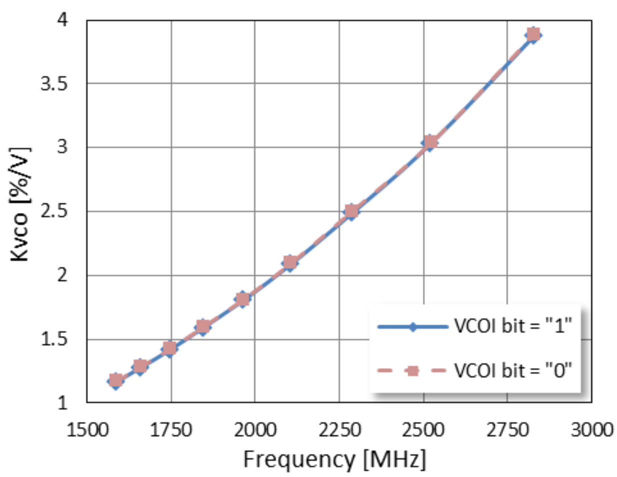


Figure.19 VCO Tuning Sensitivity

AK1573C

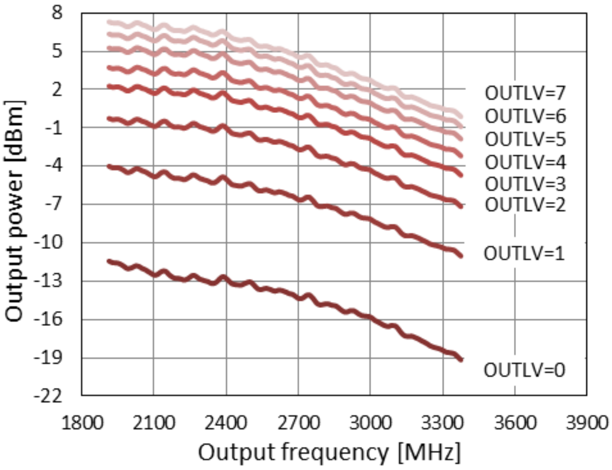
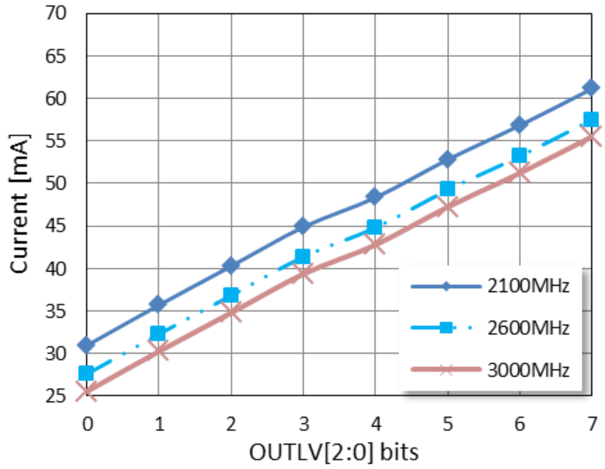
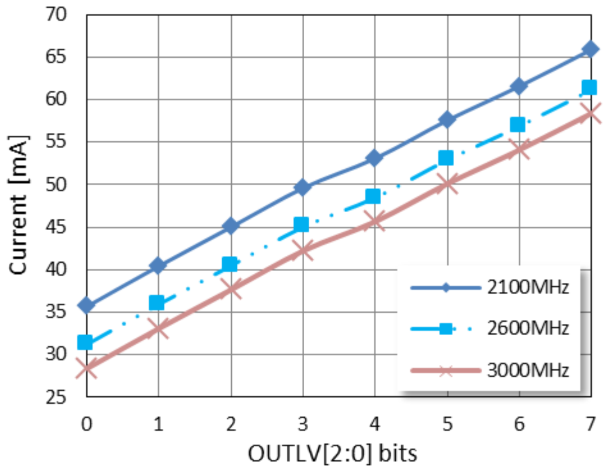


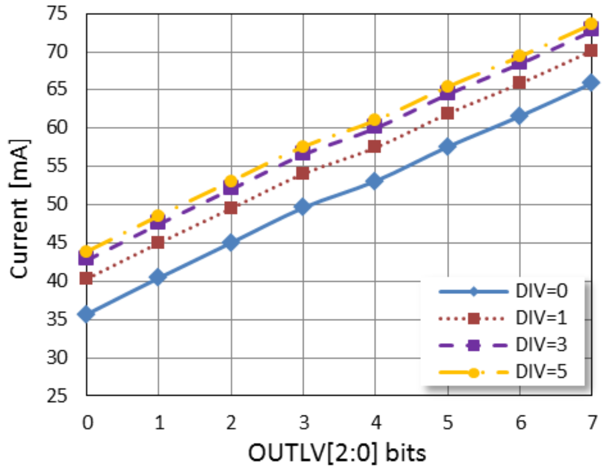
Figure.20 Output power vs. Output frequency



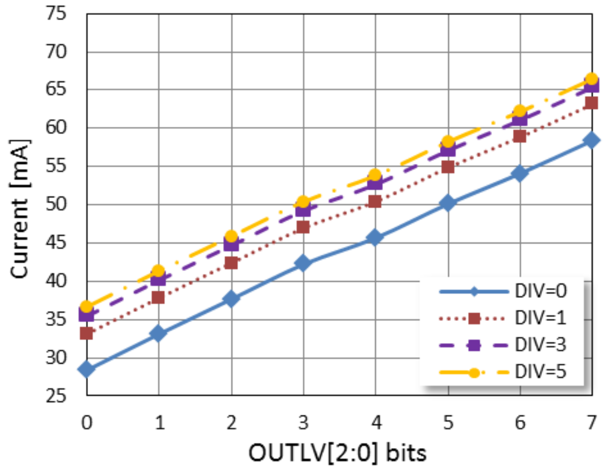
(a) VCOI bit = “0”, DIV[2:0] bits = “000”



(b) VCOI bit = “1” , DIV[2:0] bits = “000”

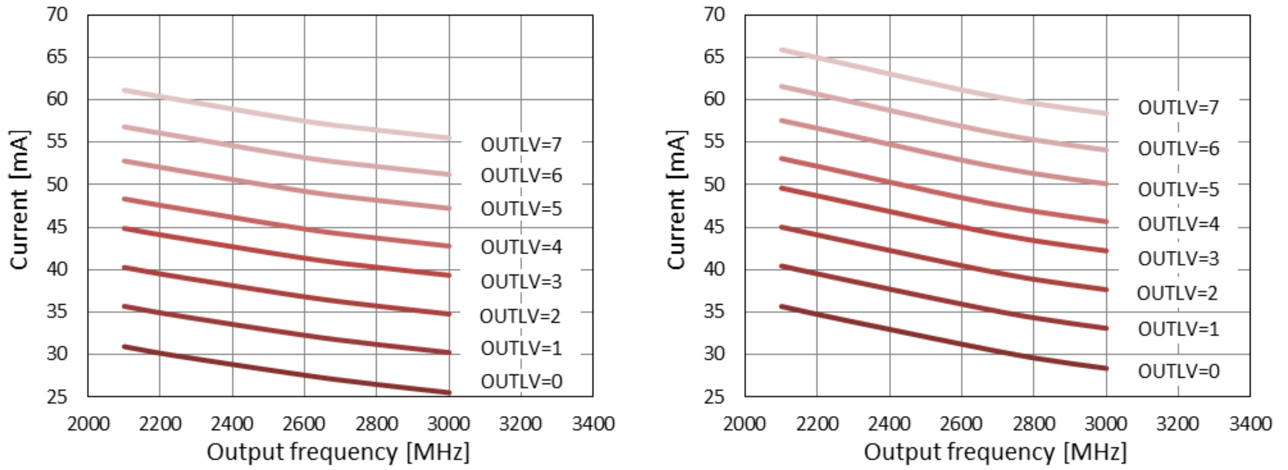


(c) Output frequency=2100MHz, VCOI bit=“1”



(d) Output frequency=3000MHz, VCOI bit=“1”

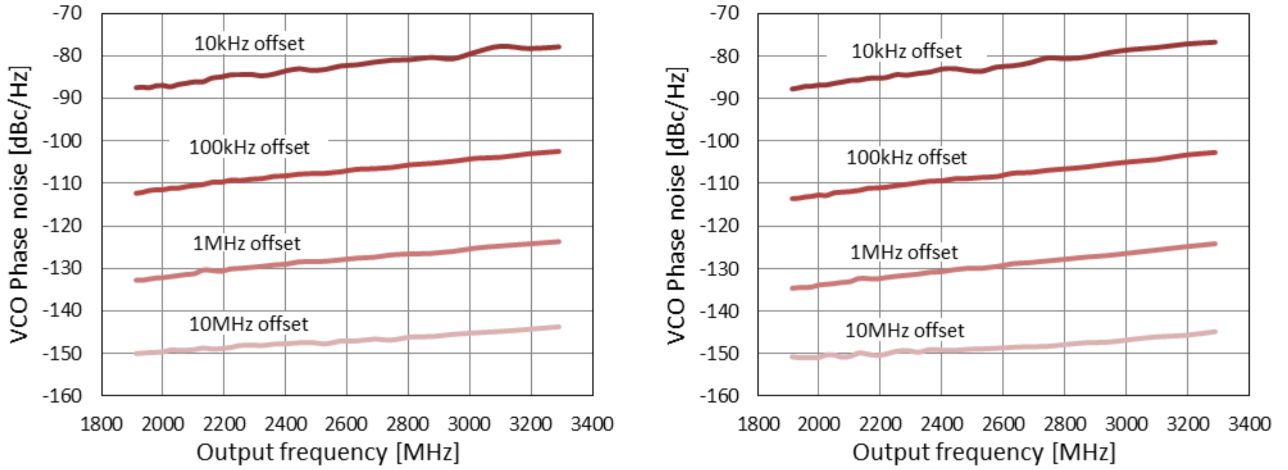
Figure.21 Current vs. OUTLV[2:0] bits
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = “111”



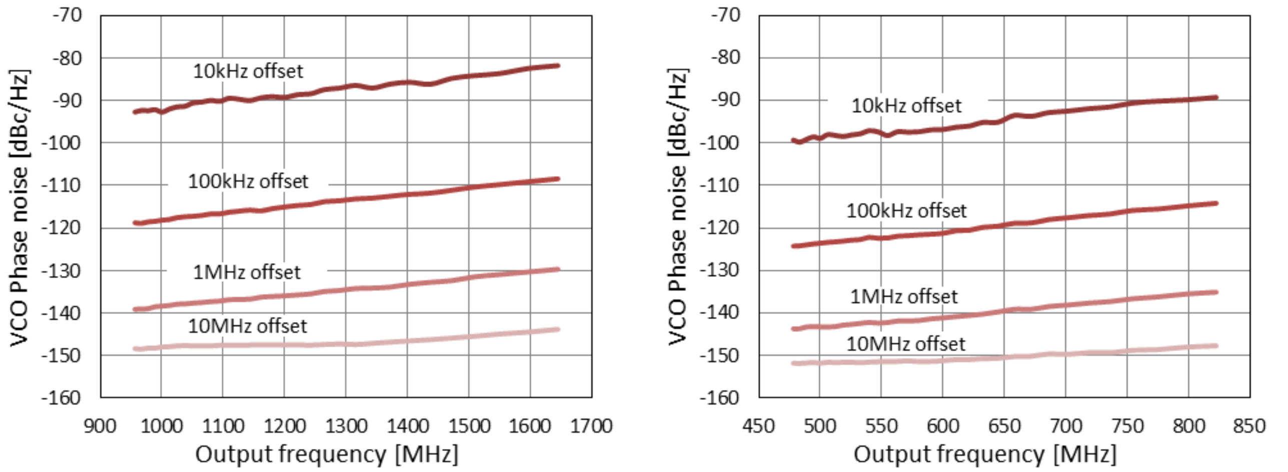
(a) VCOI bit = “0” (b) VCOI bit = “1”

Figure.22 Current vs. Output frequency

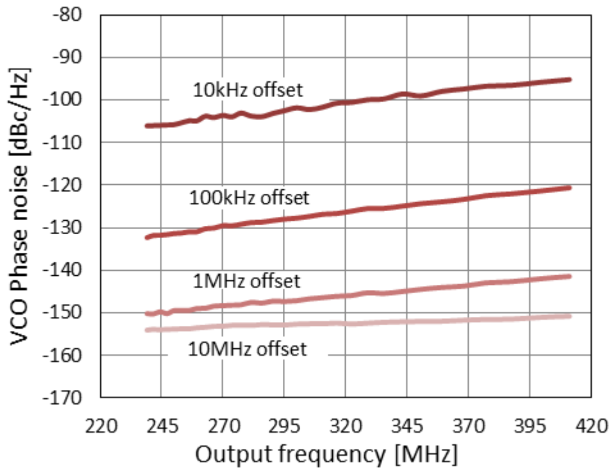
REFIN frequency = 100MHz, R counter = 100, CP1[2:0] bits = “111”, DIV[2:0] bits = “000”



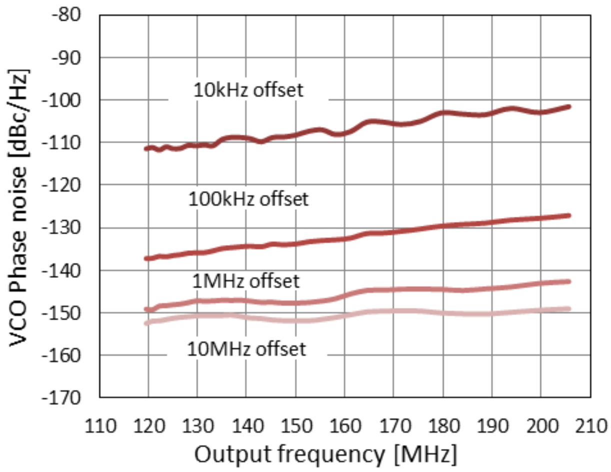
(a) VCOI bit = “0”, DIV[2:0] bits = “000” (b) VCOI bit = “1”, DIV[2:0] bits = “000”



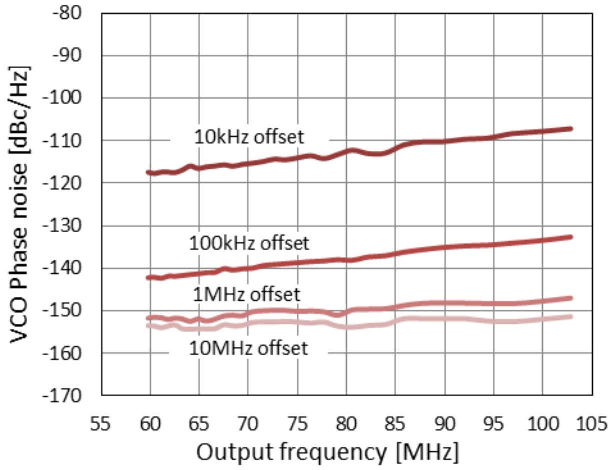
(c) VCOI bit = “1”, DIV[2:0] bits = “001” (d) VCOI bit = “1”, DIV[2:0] bits = “010”



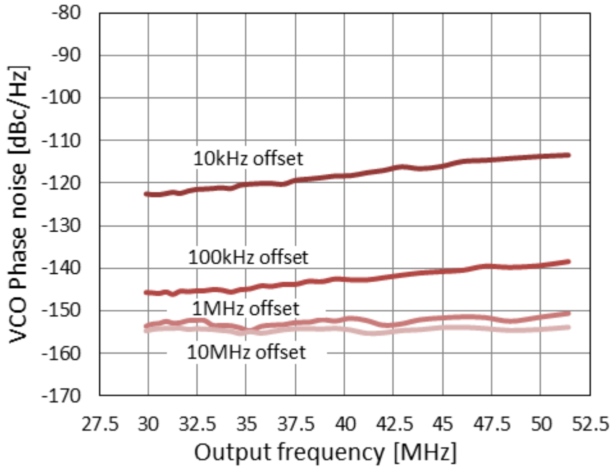
(e) VCOI bit = “1”, DIV[2:0] bits = “011”



(f) VCOI bit = “1”, DIV[2:0] bits = “100”



(g) VCOI bit = “1”, DIV[2:0] bits = “101”



(h) VCOI bit = “1”, DIV[2:0] bits = “110”

Figure.23 VCO Phase Noise vs. Output frequency
OUTLV[2:0] bits = “111”

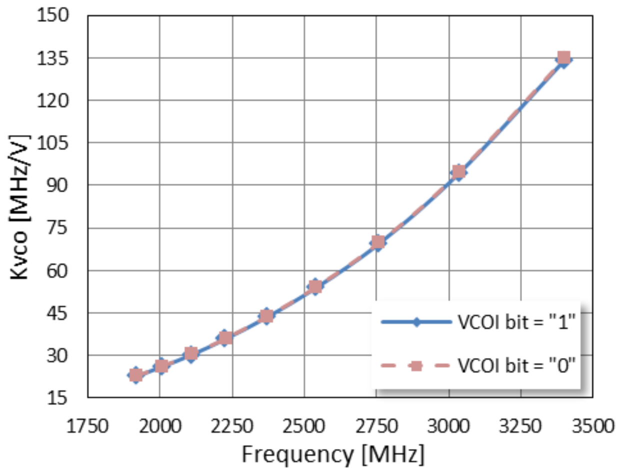


Figure.24 VCO Tuning Sensitivity

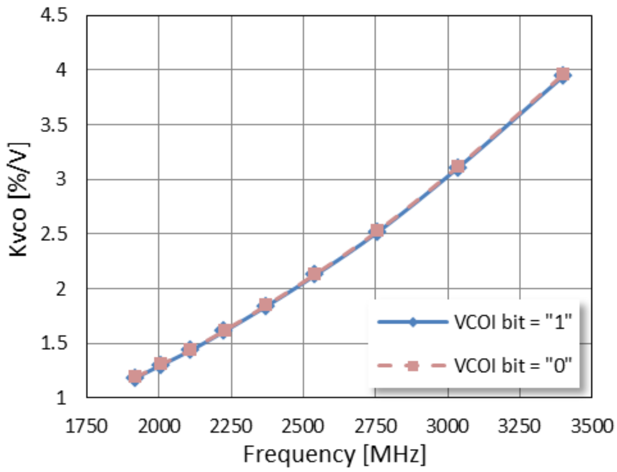


Figure.25 VCO Tuning Sensitivity

12. Register Map

Name	Data	Address			
A/B	D19 to D0	0	0	0	1
C/P		0	0	1	0
Ref/Pres		0	0	1	1
Function		0	1	0	0

	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
A/B	Don't care	B [12]	B [11]	B [10]	B [9]	B [8]	B [7]	B [6]	B [5]	B [4]	B [3]	B [2]	B [1]	B [0]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	0x01
C/P	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	CP2 [2]	CP2 [1]	CP2 [0]	Don't care	Don't care	Don't care	CP1 [2]	CP1 [1]	CP1 [0]	0x02
Ref/Pres	CALTM [3]	CALTM [2]	CALTM [1]	CALTM [1]	PRE [1]	PRE [0]	R [13]	R [12]	R [11]	R [10]	R [9]	R [8]	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	0x03
Function	Don't care	Don't care	LDCNT SEL	FAST EN	CPHiZ	LD	DIV[2]	DIV[1]	DIV[0]	MTLD	OUTLV [2]	OUTLV [1]	OUTLV [0]	Don't care	Don't care	VCOI	FAST [3]	FAST [2]	FAST [1]	FAST [0]	0x04
Software Reset	Don't care																				0x05

■ Notes on writing registers

1. When PDN1 pin = ”H” and LDO (VREF1 pin) is active, access to the register is available
2. The setting of <Address0x02> and <Address0x03> will be reflected to the behavior of AK1573 when the register <Address0x01> is written
3. <Address0x04> can be written independently.
4. After PDN1 pin turns to “H”, all of the register values are indefinite. It is needed to write the data to all the registers to confirm.

Examples of the register setting

Ex.1 Power on setting

1. Set PDN1 pin = ”L” and PDN2 pin = ”L”
2. Power on VCOVDD, PVDD and CPVDD
   Note) All VDD should be powered on simultaneously
3. Set PDN1 pin = ”H” and PDN2 pin = ”L” (VBG / LDO are powered on)
4. Write the data to the register <Address0x04>
5. Set PDN1 pin = ”H” and PDN2 pin = ”H” (All blocks are powered on)
6. Write the data to the register <Address0x01> and <Address0x02>
7. Write the data to the register <Address0x01>

Ex.2 Change frequency settings

1. Write the data to the register <Address0x01>

Ex.3 Change Charge Pump settings

1. Write the data to the register <Address0x02>
2. Write the data to the register <Address0x01>

Ex.4 Change Reference dividing ratio

1. Write the data to the register <Address0x03>
2. Write the data to the register <Address0x01>

< Address0x01 : N counter >

D[18:6]

B[12:0] : B (Programmable) counter setting
Set the dividing ratio of B (Programmable) counter.
The setting range is shown in the following table.

B[12:0]	Programmable counter dividing ratio	Remark
0	-	Prohibited
1	-	Prohibited
2	-	Prohibited
3	3	
:	:	
8191	8191	

D[5:0]

A[5:0] : A (Swallow) counter setting
Set the dividing ratio of A (Swallow) counter.
The setting range is shown in the following table.

A[5:0]	Swallow counter dividing ratio	Remark
0	0	
1	1	
2	2	
:	:	
63	63	

The data at A[5:0] bits and B[12:0] bits must meet the following requirements:
B[12:0] bits ≥ 3, B[12:0] bits ≥ A[5:0] bits
See “13. Frequency Setting” for details of the relationship between a frequency dividing ratio N and the data at A[5:0] bits and B[12:0] bits.

It is prohibited to set frequency once again until VCO calibration and Fast lock-up mode is completed.

< Address0x02 : C/P >

D[8: 6]

CP2[2:0] : Charge pump current setting for Fast Lockup operation

D[2:0]

CP1[2:0] : Charge pump current setting for normal operation
AK1573 provides two settings for charge pump current. CP1[2:0] bits are for normal operation and CP2[2:0] bits are for Fast Lockup mode.
The following formula shows the relationship among the resistance value, the register setting and the electric current.

Charge pump current (Icp) [A] = Icp_min [A] × [(CP1[2:0] bits or CP2[2:0] bits setting) + 1]
Charge pump minimum current (Icp_min) [A] = 9.45 / BIAS Resistance [Ω]

The following table shows the typical Icp for each status.

Icp (typ.) unit : μA

CP1[2:0], CP2[2:0]	BIAS		
	33kΩ	27kΩ	22kΩ
0	286	350	430
1	573	700	859
2	859	1050	1289
3	1146	1400	1718
4	1432	1750	2148
5	1718	2100	2577
6	2005	2450	3007
7	2291	2800	3436

< Address0x03 : Ref/Pres >

D[19:16]

CALTM[3:0] Set the calibration precision of VCO

The register CALTM[3:0] bits set the calibration precision and time. The larger CALTM[3:0] bits are set, the higher calibration precision becomes, but the longer calibration time is required as trade-off. Set the value calculated by the following formula to get enough calibration precision. However, CALTM[3:0] bits should be set from 0 to 10. Over 11 are prohibited. See “15. VCO” for details of the VCO calibration.

$$\text{CALTM[3:0] bits} \geq 10 - \log(\text{B[12:0] bits}) / \log(2)$$

The calibration time can be estimated as following formula;

$$\text{Calibration time} = 1 / F_{PFD} \times 11 \times 2 \,\hat{}\, \text{CALTM[3:0] bits}$$

D[15:14]

PRE[1:0] : Selects a dividing ratio for the prescaler

00: P=8
01: P=16
10: P=32
11: P=64

The prescaler value should be selected so that the prescaler output frequency is less than or equal to 300MHz.

D[13:0]

R[13:0] : 14bit Reference Counter

The following settings can be selected for the reference clock division.
The allowed range is 1 (1/1 division) to 16383 (1/16383 division). 0 cannot be set.
The maximum PFD frequency is 104MHz.

R[13:0]	Dividing Ratio
0	Prohibited
1	1
2	2
3	3
4	4
:	:
:	:
:	:
16381	16381
16382	16382
16383	16383

< Address0x04 : Function >

D[17]

LDCNTSEL : Lock Detect Precision
Set the counter value for digital lock detect.

LDCNTSEL	Function	
0	15 times Count	unlocked to locked
	3 times Count	locked to unlocked
1	31 times Count	unlocked to locked
	7 times Count	locked to unlocked

D[16]

FASTEN : Enables the Fast Lock mode
See “14. Fast Lock-up mode” for details of the Fast Lock-up function.

0: Fast Lockup disable
1: Fast Lockup enable

D[15]

CPHIZ : TRI-STATE output setting for charge pump

0: Charge pumps are activated
1: Tri-State

D[14]

LD : Selects output from LD pin
See “12. Lock detect” for details of the Lock detect function.

0: Digital lock detect
1: Analog lock detect

D[13:11]

DIV[2:0] : Selects Divide of Output

Select the dividing ratio in accordance with the used frequency.

0: Divide by 1
1: Divide by 2
2: Divide by 4
3: Divide by 8
4: Divide by 16
5: Divide by 32
6: Divide by 64
7: Prohibited

D[10]

MTLD : Local signal mute

0: Disable to mute local signal in unlock state.
1: Enable to Mute local signal in unlock state.

Set MTLD bit = “0” when LD bit = “1”.

D[9:7]

OUTLV[2:0] : Select output power level

Adjust bias current of output buffer

OUTLV[2:0]	Bias current (mA)
0	4
1	8
2	12
3	16
4	20
5	24
6	28
7	32

D[4]

VCOI : VCO core current setting

0: Low current mode
1: Normal

D[3:0]

FAST[3:0] : FAST counter timer
Set the effective time of fast lock-up mode.
Counter value = 3 + FAST[3:0] bits × 4

FAST[3:0]	Counter value
0	3
1	7
2	11
3	15
4	19
5	23
6	27
7	31
8	35
9	39
10	43
11	47
12	51
13	55
14	59
15	63

< Address0x05 : Software Reset >

When writing a <Address0x05>, all of the internal flip-flops, except for the register and calibration results, are initialized. Internal flip-flops except for the register and the calibration results is initialized in the state of PDN1 pin = PDN2 pin = "H". When standing up PDN1 pin and PDN2 pin at the same time or PDN1 pin and PDN2 pin are fixed to "H", internal flip-flops are not initialized. In this case, it is needed to initialize internal flip-flops using the Software Reset.

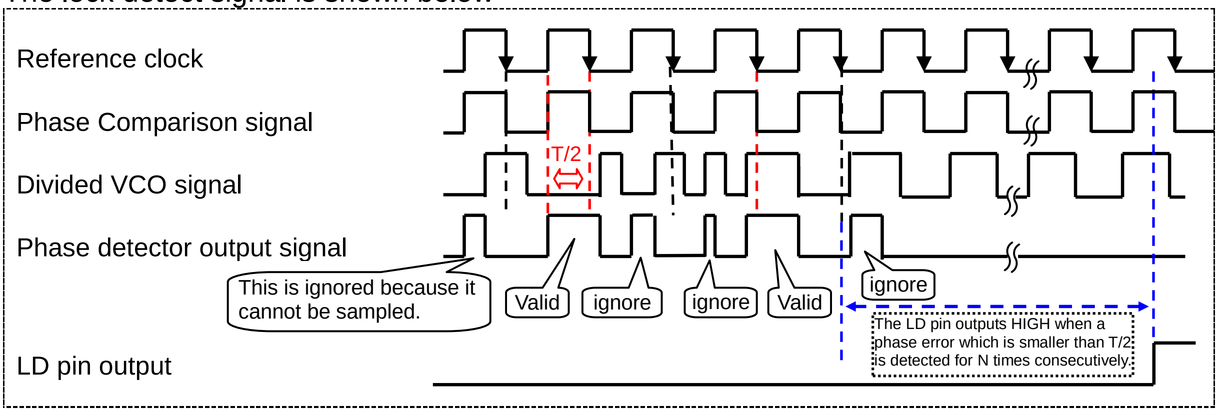
13. Function Descriptions

13.1. Lock detect

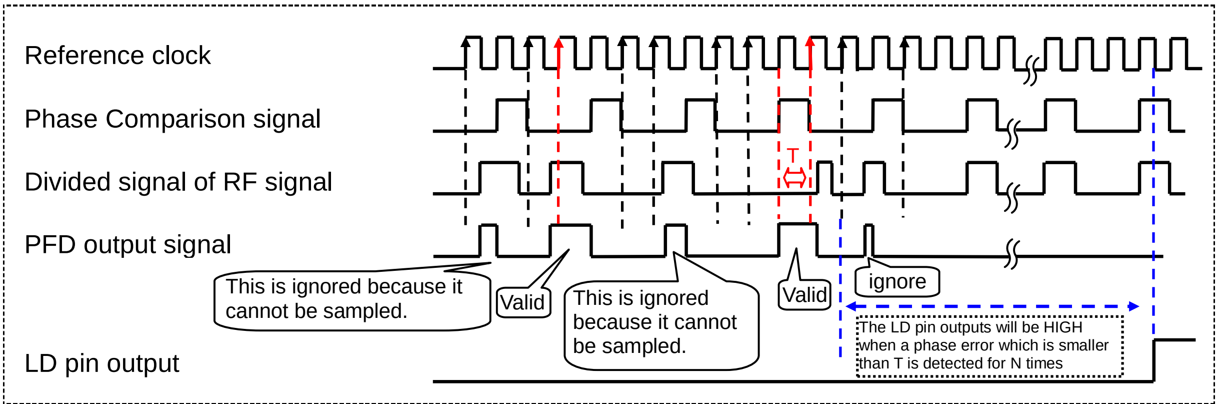
Lock detect output can be selected by LD bit in <Address0x04>. When LD bit = "1", LD pin outputs a phase comparison result which is from phase detector directly (This is called "analog lock detect"). When LD bit = "0", the output is the lock detect signal according to the on-chip logic (This is called "digital lock detect").
The digital lock detect can be done as following :
The LD pin is in unlocked state (which outputs "L") when a frequency setup is made.
In the digital lock detect, the LD pin outputs "H" (which means the locked state) when a phase error smaller than a cycle of [REFIN] clock (T) is detected for N times consecutively. When a phase error larger than T is detected for N times consecutively while the LD pin outputs "H", then the LD pin outputs "L" (which means the unlocked state). The counter value N can be set by LDCNTSEL bit in <Address0x04>. The N is different between "unlocked to locked" and "locked to unlocked".

LDCNTSEL bit	unlocked to locked	locked to unlocked
0	N=15	N=3
1	N=31	N=7

The lock detect signal is shown below



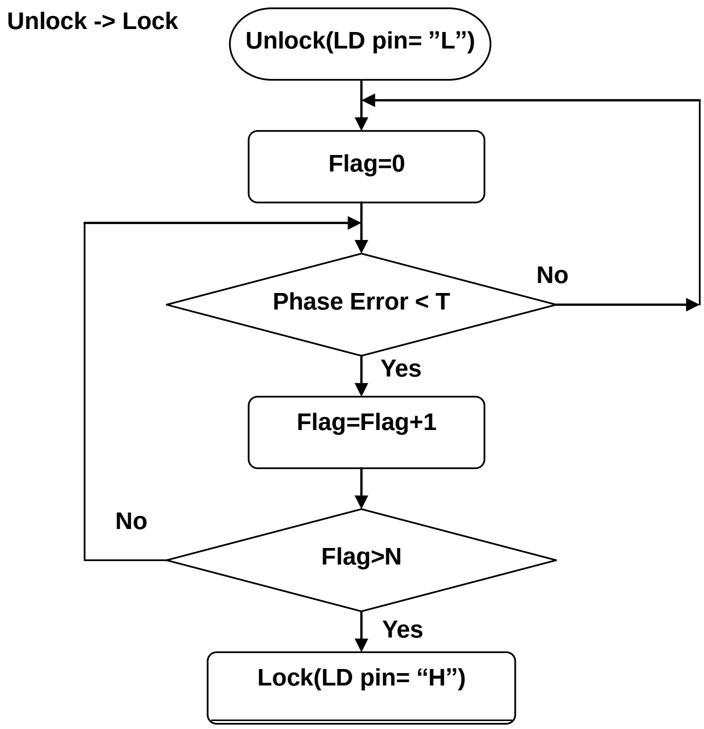
Case of R counter = 1 (Note)

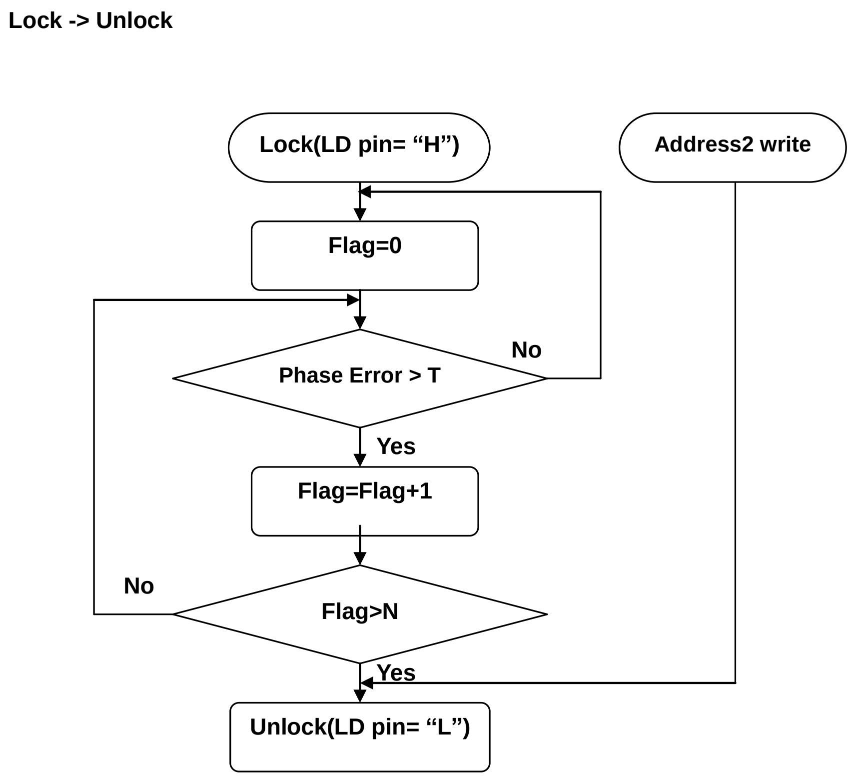


Case of R counter > 1 (Note)

* R counter can be set by R[13:0] bits in Address0x03

Figure.26 Digital Lock Detect Operations


Unlock -> Lock
Unlock(LD pin= ”L”)
Flag=0
Phase Error < T
No
Yes
Flag=Flag+1
No
Flag>N
Yes
Lock(LD pin= “H”)


Lock -> Unlock
Lock(LD pin= “H”)
Address2 write
Flag=0
Phase Error > T
No
Yes
Flag=Flag+1
No
Flag>N
Yes
Unlock(LD pin= “L”)

13.2. Frequency Setting

The following formula is used to calculate the frequency setting for the AK1573.

Frequency Setting	= F_{PFD} × (P × B + A)	
F_{PFD}	: PFD frequency	
P	: Prescalor value (refer to Address0x02 : Pre[1:0])	
B	: B (Programmable) counter (refer to Address0x01 : B[12:0])	
A	: A (Swallow)counter (refer to Address0x01 : A[5:0])	

○ Example

Set the AK1573 as follows to obtain Frequency setting =2100MHz with F_{PFD} = 200kHz

P = 8 (Address0x02 : Pre[1:0] bits = 0)
B = 1312 (Address0x01 : B[12:0] bits = 1312)
A = 4 (Address0x01 : A[5:0] bits = 4)

Frequency setting = 200k × (8 × 1312 + 4) = 2100MHz

Note) Lower limit for setting consecutive dividing numbers

For the AK1573, it is not possible to set consecutive dividing ratio below the lower limit (The lower limit is determined by a dividing ratio set for the prescaler).
The following table shows an example where consecutive dividing numbers below the lower limit cannot be set. The consecutive dividing ratio can be set when B ≥ P-1.

***P=8 (Dual modulus prescaler 8/9)**

P	B[12:0]	A[5:0]	Dividing ratio	
8	6	6	54	55 cannot be set as an N divider.
8	7	0	56	This is the lower limit. 56 or over can consecutively be set as an N divider.
8	7	1	57	
:	:	:	:	
8	7	7	63	
8	8	0	64	
:	:	:	:	

***P=16 (Dual modulus prescaler 16/17)**

P	B	A	N	
16	14	14	238	239 cannot be set as an N divider.
16	15	0	240	This is the lower limit. 240 or over can consecutively be set as an N divider.
16	15	1	241	
:	:	:	:	
16	15	15	255	
16	16	0	256	
:	:	:	:	

***P=32 (Dual modulus prescaler 32/33)**

P	B	A	N	
32	30	30	990	991 cannot be set as an N divider.
32	31	0	992	This is the lower limit. 992 or over can consecutively be set as an N divider.
32	31	1	993	
:	:	:	:	
32	31	31	1023	
32	32	0	1024	
:	:	:	:	

***P=64 (Dual modulus prescaler 64/65)**

P	B	A	N	
64	62	62	4030	4031 cannot be set as an N divider.
64	63	0	4032	This is the lower limit. 4032 or over can consecutively be set as an N divider.
64	63	1	4033	
:	:	:	:	
64	63	63	4095	
64	64	0	4096	
:	:	:	:	

13.3. Fast Lock-up mode

The AK1573 goes into Fast Lock Up mode by setting FASTEN bit in <Address0x04> to “1”. When A and B counter setting is finished (writing in <Address0x01>), Fast Lock Up mode starts after calibration.
The Fast Lock Up mode is enabled only during the time period set by the timer according to the counter value in FAST[3:0] bits in <Address0x04>. The charge pump current is set to the value specified by CP2[2:0] bits. When the specified time period elapses, the Fast Lock Up mode operation is switched to the normal operation, and the charge pump current returns to CP1[2:0] bits setting.

FAST[3:0] bits in <Address0x04> is used to set the time period for this mode. The following formula is used to calculate the time period :

Switchover time = 1 / F_{PFD} × Counter Value
Counter Value = 3 + 4 × (FAST[3:0] bits setting)

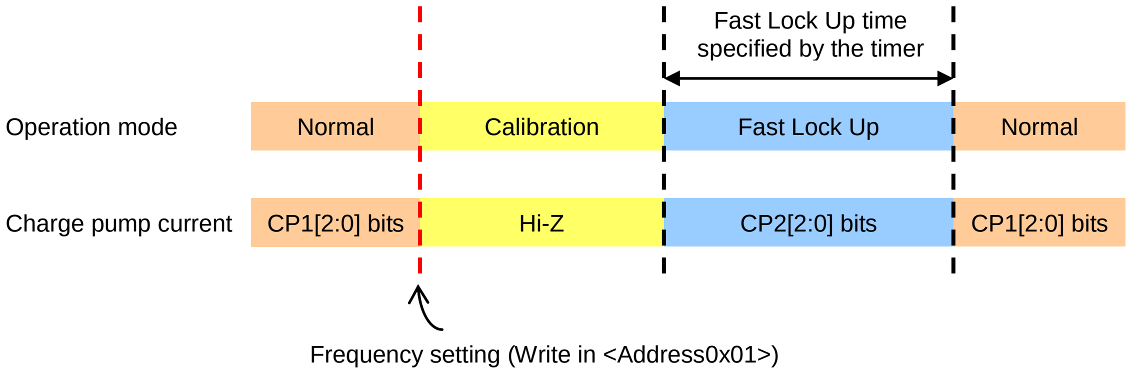


Figure.27 Fast Lock-up Mode Timing Chart

13.4. VCO

Calibration

The VCO core in AK1573 uses several overlapping bands to achieve low Phase Noise, low VCO sensitivity (K_{VCO}) and wide frequency range. The correct band is chosen automatically at frequency setting by VCO calibration. The calibration starts when A counter and B counter in <Address0x01> are set. During the calibration, VCO V_{CNT} is disconnected from the external loop filter and connected to an internal reference voltage. The charge pump output is Tri-State.

The internal reference voltage must be stable so that the calibration is done correctly. Therefore, it is necessary to wait 10µsec at least until <Address0x01> is set after PDN2 pin rises up to “1” (when 100pF is connected to SCAP pin).

The register CALTM[3:0] bits set the calibration precision and time. The larger CALTM[3:0] bits are set, the higher calibration precision becomes, but the longer calibration time is required as trade-off. Set the value calculated by the following formula to get enough calibration precision. However, CALTM[3:0] bits should be set from 0 to 10. Over 11 are prohibited.

$$\text{CALTM[3:0] bits} \geq 10 - \log(\text{B[12:0]}) / \log(2)$$

The calibration time can be estimated as following formula;

$$\text{Calibration time} = 1 / F_{PFD} \times 11 \times 2 \text{ \^{} CALTM[3:0] bits}$$

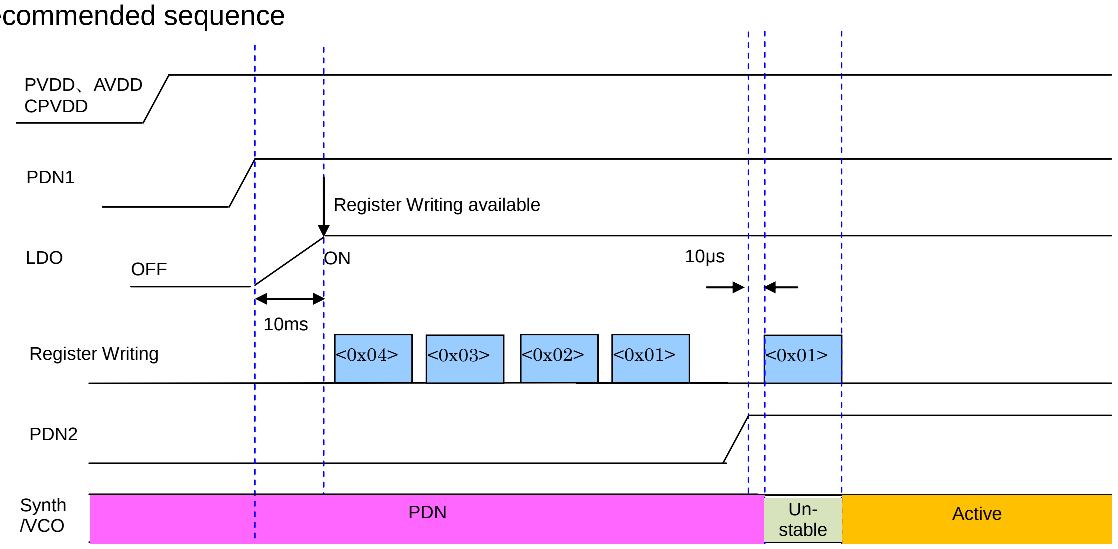
It is prohibited to set frequency once again until VCO calibration and Fast lock-up mode is completed.

Low Current Mode

The AK1573 goes into low current mode by setting VCOI bit in <Address0x04> to “0”. This mode decreases VCO core current but Phase Noise gets worse compared to normal mode.

14. Power on sequence

1. Recommended sequence



2. The sequence when PDN1 pin and PDN2 pin are powered on simultaneously

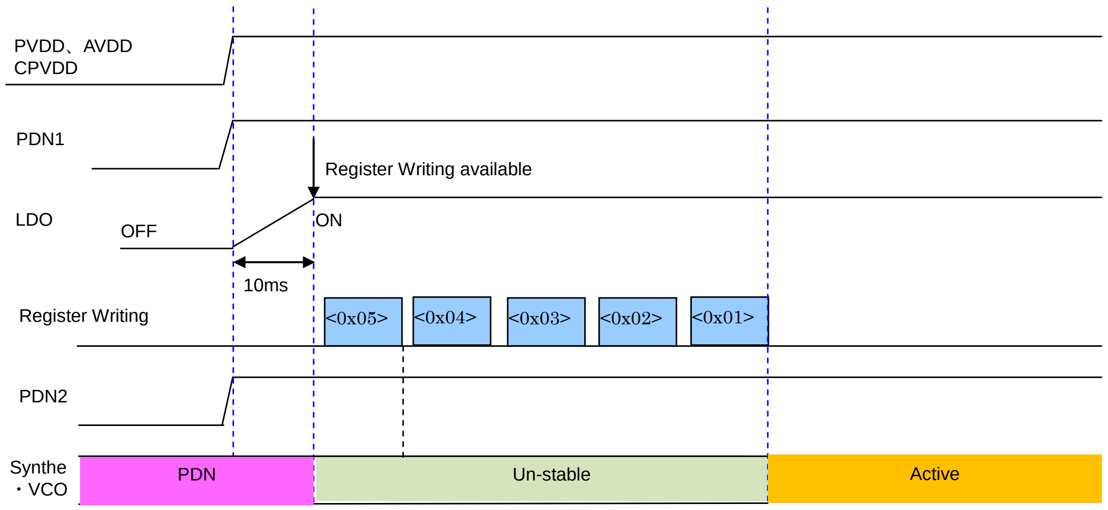


Figure.28 Power on sequence

* After powering on AK1573, the initial register's values are not defined. It is required to write the data to all the registers.
* It takes about 10msec from PDN1 pin rise-up to LDO rise-up.
* If PDN1 pin and PDN2 pin are powered on simultaneously, the operation of AK1573 is not defined until the registers are set.

15. Recommended External Circuits

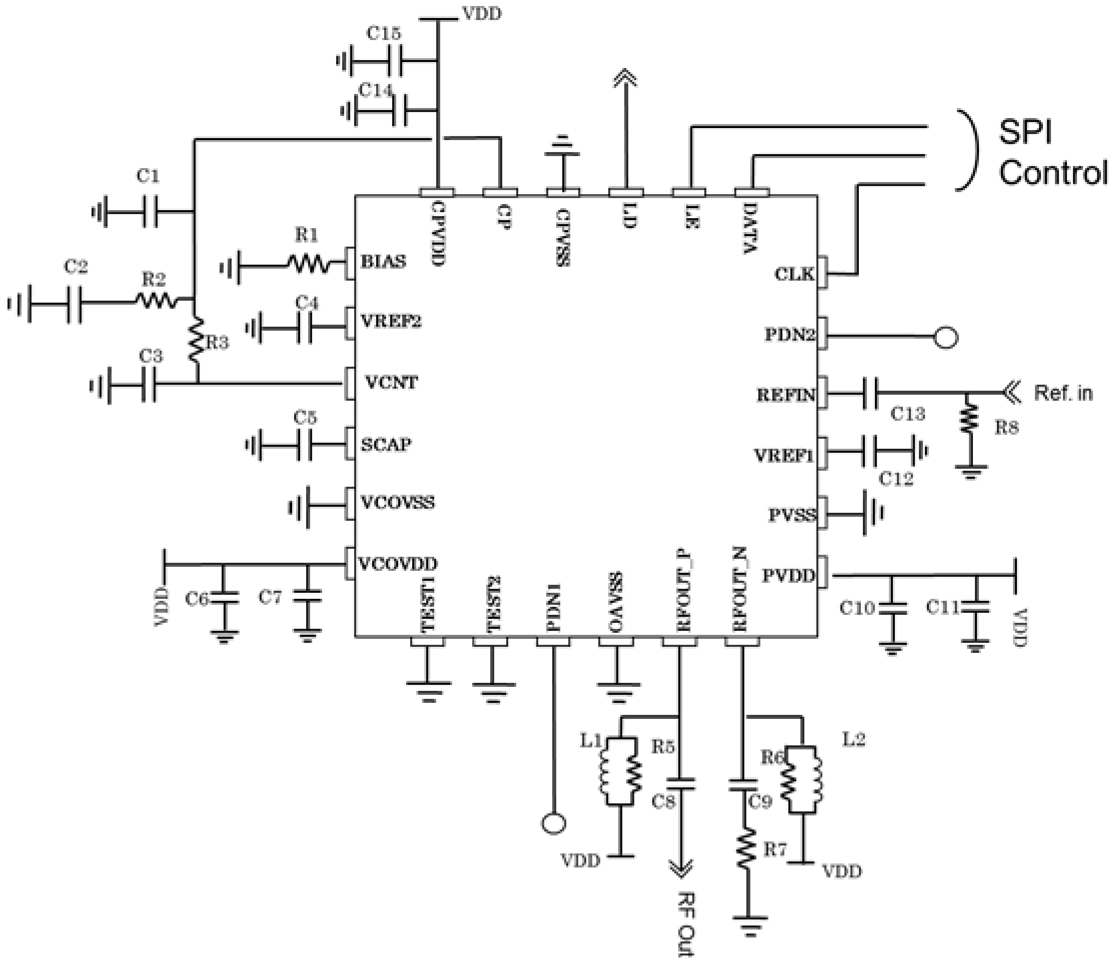


Figure.29. Evaluation Board Schematic

Table.1

Ref.	Value	Ref.	Value	Ref.	Value	Ref.	Value
C1	Loop Filter	C7	100pF	C13	100pF	R3	Loop Filter
C2	Loop Filter	C8	100pF	C14	100pF	R1	27kΩ
C3	Loop Filter	C9	100pF	C15	10nF	R5	100Ω
C4	470nF	C10	100pF	L1	2.2μH	R6	100Ω
C5	100pF	C11	10nF	L2	2.2μH	R7	51Ω
C6	10nF	C12	220nF	R2	Loop Filter	R8	51Ω

* The exposed pad at the center of the backside should be connected to the ground.
* TEST1 / TEST2 pins should be connected to the ground.
* RFOUT_P / RFOUT_N pins must be connected an inductor and a register to VDD.
* In the case of single-ended output operation, unused output pin is terminated through 50Ω after 100pF capacitance.

16. Application Note

Differential to single-ended circuit

AK1573 has differential output ports. "15 Recommended External Circuits" shows single-ended output but users can convert differential output to single output using lumped element balun. By doing this, AK1573 outputs higher signal level compared to single-ended output with the same current consumption. Lumped element balun shows frequency dependence, so users need to populate optimized elements in order to obtain good matching characteristics. Table.2 shows the reference values of lumped element balun.

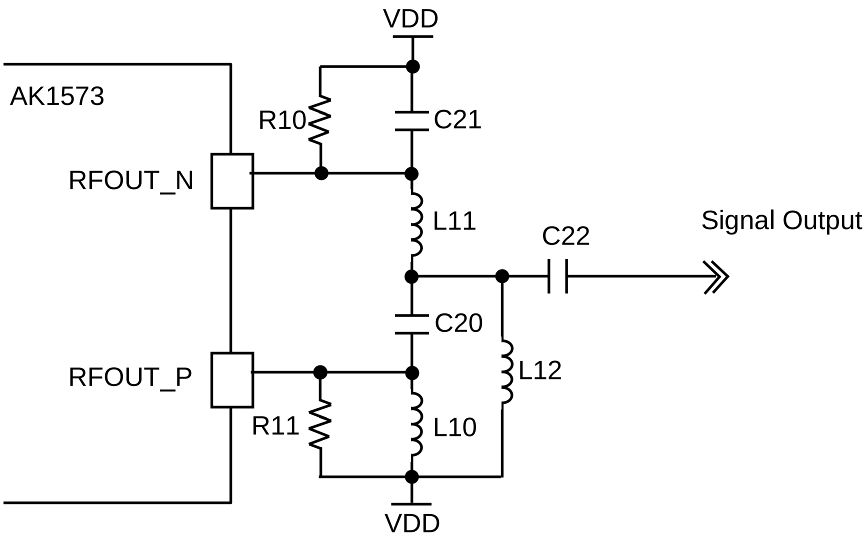
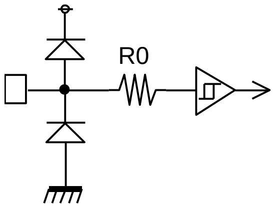
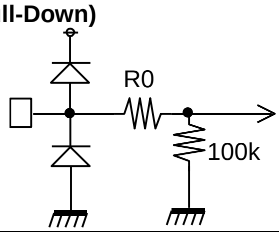
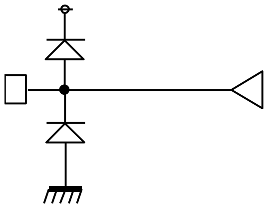
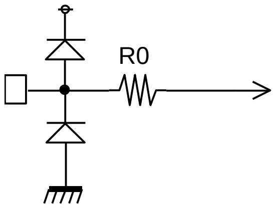


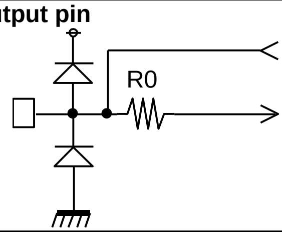
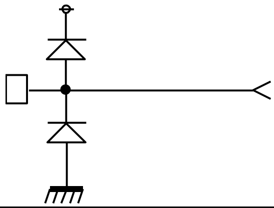
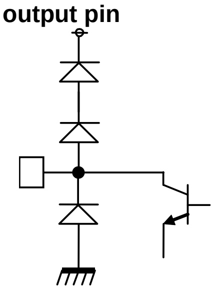
Figure 30 Lumped Element Balun Circuit

Table.2 Reference values of lumped element balun

Frequency Range [MHz]	C20 [pF]	C21 [pF]	C22 [pF]	L10 [nH]	L11 [nH]	L12 [nH]	R10 [Ω]	R11 [Ω]
2150 to 2250	1	1	1000	1	1	330	100	100
2000 to 2150	1	1	1000	1.5	1.5	330	100	100
1900 to 2000	1	1	1000	2	2	330	100	100
1770 to 1900	1	1	1000	2.4	2.4	330	100	100
1600 to 1770	1	1	1000	3.3	3.3	330	100	100
1450 to 1600	1	1	1000	4.3	4.3	330	100	100
1280 to 1450	1	1	1000	5.1	5.1	330	100	100
1050 to 1280	1	1	1000	7.5	7.5	330	100	100
800 to 1050	1	1	1000	10	10	330	100	100
550 to 800	1	1	1000	15	15	330	100	100
350 to 550	1.6	1.6	1000	22	22	330	100	100
200 to 350	4.7	4.7	1000	47	47	330	100	100
100 to 200	8	8	1000	82	82	330	100	100
60 to 100	15	15	1000	150	150	330	100	100
40 to 60	27	27	1000	270	270	330	100	100
30 to 40	39	39	1000	390	390	330	100	100

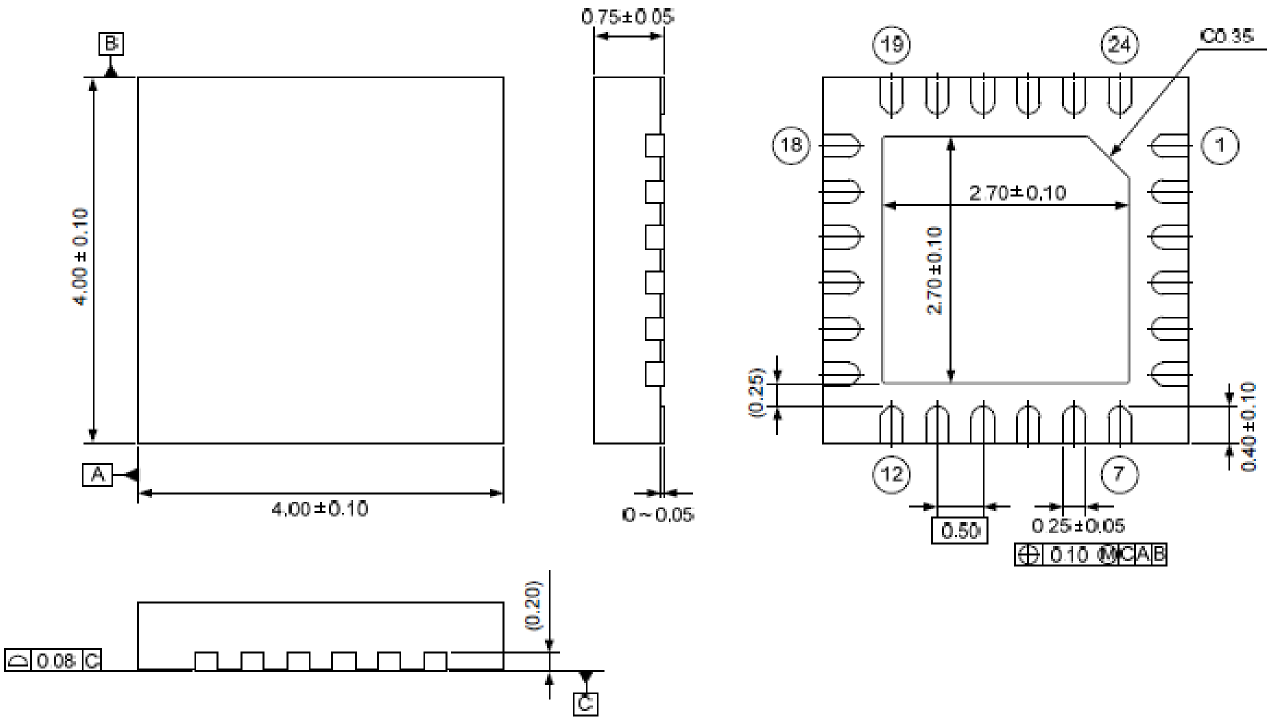
17. Interface circuit

Pin No.	Pin name	I/O	R0 (Ω)	Current (μA)	Function
9	PDN1	I	300		**Digital input pin** 
17	PDN2	I	300		
18	CLK	I	300		
19	DATA	I	300		
20	LE	I	300		
7	TEST1	I	300		**Digital input (Pull-Down)** 
8	TEST2	I	300		
21	LD	O			**Digital output pin** 
3	VCNT	I	100		**Analog input pin** 
16	REFIN	I	300		

Pin No.	Pin Name	I/O	R0 (Ω)	Current (μA)	Function
1	BIAS	IO	300		**Analog input/output pin** 
2	VREF2	IO	300		
4	SCAP	IO	100		
15	VREF1	IO	300		
23	CP	O			**Analog output pin** 
11	RFOUT_P	O			**Open-collector output pin** 
12	RFOUT_N	O			

18. Package

18.1. Outline Dimensions

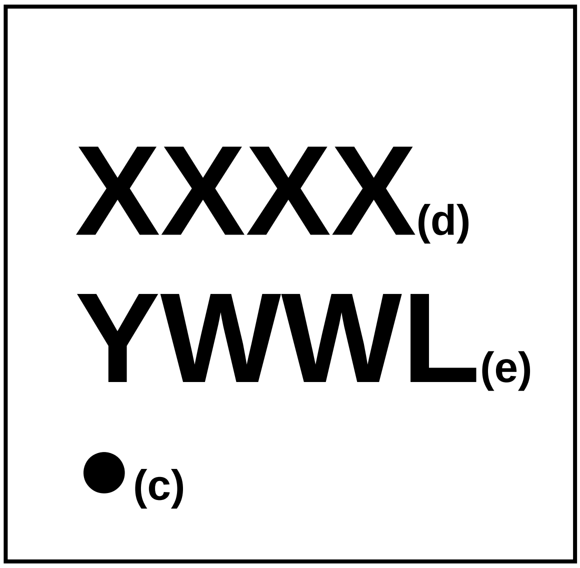


* The exposed pad at the center of the backside should be connected to ground.

18.2. Marking

(a) Style : QFN
(b) Number of pins : 24-pin
(c) 1 pin marking : ○
(d) Product number : XXXX (4 or 5 digits)
AK1573 : AK1573
AK1573B : AK1573B
AK1573C : AK1573C

(e) Date code : YWWL (4 digits)
Y: Lower 1 digit of calendar year (Year 2015 → 5, 2016 → 6 ...)
WW: Week
L: Lot identification, given to each product lot which is made in a week
→ LOT ID is given in alphabetical order (A, B, C…)



19. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/08/03	00	First Edition		

IMPORTANT NOTICE