AK2027

Product Datasheet

Latest Version: 1.0

2009-06-03

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Revision History

Date	Revision	Description
2009-06-03	1.0	Initial Release

1. Introduction

1.1 Overview

AK2027 is a single-chip highly-integrated digital music system solution for devices such as dedicated audio players. It includes an audio decoder with a high performance DSP with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. AK2027 also provides an interface to flash memory and memory card, LED/LCD, button and switch inputs, headphones, and microphone, and FM radio input and control. Its programmable architecture supports WMA and other digital audio standards. For devices like USB-Disk, it can act as a USB mass storage slave device to personal computer system. The Chip has low power consumption to allow long battery life and efficient flexible on-chip DC-DC converters that allows Li-ion battery. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphones. The A/D includes inputs for both Microphone and Analog Audio in to support voice recording and FM radio integration features. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio players.

1.2 Features

- MPEG1/2/2.5 Audio Layer 1,2,3 decoder， bit rate 8-448Kbps,8-48KHz,CBR/VBR
- Support WMA Decoder, bit rate 32-384Kbps,8-48KHz
- Digital Voice Recording at ultra low 4.4 or 8Kbps w/ Artek Speech Algorithm
- 24 bits DSP Core
- On-chip DSP PM with SRAM(16K*24) ,can be switched to be MCU memory space
- On-chip DSP DM with SRAM(16K*24), can be switched to be MCU memory space
- Integrated MCU, the instruction set is compatible with Z80
- Internal ZRAM1((16K-64)*8),ZRAM2((12K+256)*8),ZRAM3(16K*8) accessed by MCU
- Internal 14Kx8 BROM build in Boot up and USB Upgrade firmware
- Internal (21K+12K)x8 TROM
- Internal SRAM access time<7ns
- External up to 4 (pcs) x 32M~4G bytes Nand type Flash accessed by MCU or DMA
- External Smart Media Card, support following memory card interface
  Multi Media Card Specification Version 4.2 (1/4 bit mode)
  Secure Digital Card Specification Version 2.0 (1/4 bit mode)

Memory Stick Version 1.43 (1/4-bit mode)
Memory Stick Pro Version 1.02 (1/4-bit mode)

- Support 24MHz OSC with on-chip PLL for DSP and about 32KHz RC oscillator
- 2-channel DMA,1-channel CTC and interrupt controller for MCU
- Energy saving with dynamic power management, supporting Li-ion
- Support USB2.0 Compliance PHY+SIE,RD/WR:6MB/5MB (NAND Flash Base)
- Build in Stereo 20-bit Sigma-Delta D/A
- Build in Key Scan Circuit and GPIO
- Support external 8080 Series LCM driver interface
- Support FM Radio input and 32 levels volume control
- Support Stereo 21-bit Sigma-Delta A/D for Microphone/FM Input, sample rate at 8/12/16/22/24/32/48KHz
- MCU run at 48MHz(typ),F/W can program from DC up to 48MHz transparently
- DSP+PM/DM Speed up to 90MIPS,while 48mips@1.6v
- D/A+PA SNR :without A weight>91dB
- A/D SNR >86dB
- Headphone driver output 2x20mW @16ohm
- Standby Leakage Current: VCC: 50uA@3.0V (MAX), VDD: 350uA@1.6V(MAX)
- Low Power Consumption: <80mW@1.6V at typical WMA decoder solution
- Package at LQFP-64 (7X7mm)

2. Pin Description

2.1 Pin Assignment

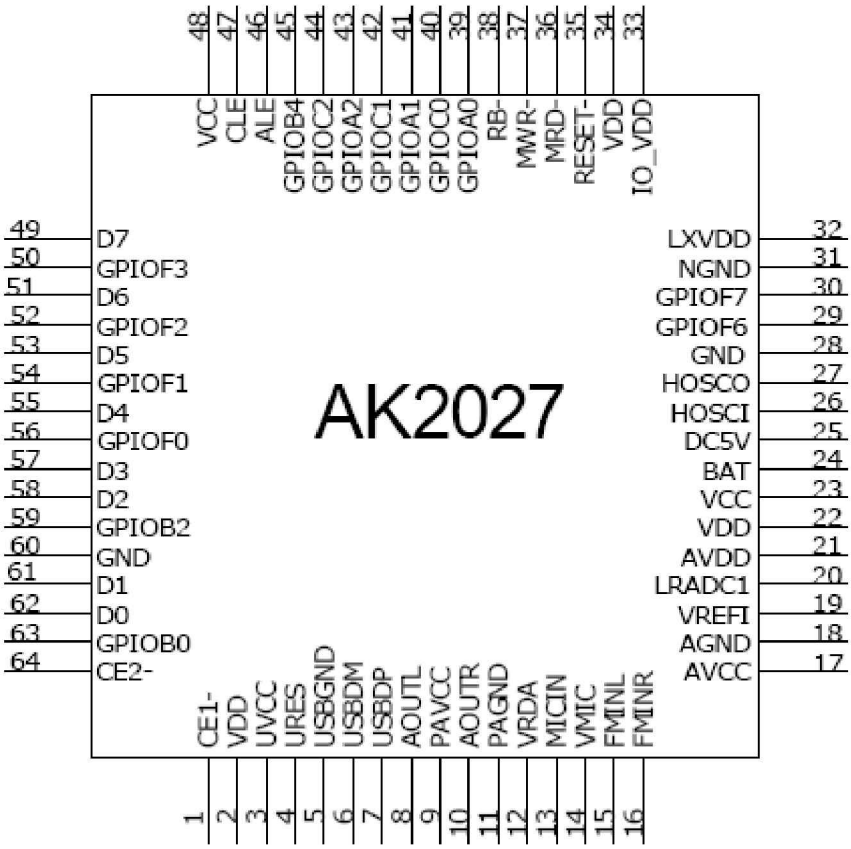


Figure 1: AK2027 Pin Out Figure

2.2 Pin Definition

Table 1: AK2027 Pin Definition

Pin No.	Pin Name	I/O Type	Driver	Reset Default	Short Description
1	CE1-	O	/	H	Ext. memory chip enable 1

2	VDD	PWR	/	/	Digital Core power
3	UVCC	PWR	/	/	Power supply for USB
4	URES	AO	/	/	USB precision Resistor
5	USBGND	PWR	/	/	USB ground
6	USBDM	A	/	H	USB data minus
7	USBDP	A	/	H	USB data plus
8	AOUTL	AO	/	/	Int. PA left channel analog output
9	PAVCC	PWR	/	/	Power supply for power amplifier
10	AOUTR	AO	/	/	Int. PA right channel analog output
11	PAGND	PWR	/	/	Power amplifier ground
12	VRDA	AO	/	/	Bypass capacitor connect pin for Int. D/A Reference voltage
13	MICIN	AI	/	/	Microphone pre-amplifier input
14	VMIC	PWR	/	/	Power supply for Microphone
15	FMINL	AI	/	/	Left channel of FM line input
16	FMINR	AI	/	/	Right channel of FM line input
17	AVCC	PWR	/	/	power supply of Analog
18	AGND	PWR	/	/	Analog ground
19	VREFI	AI	/	/	Voltage reference input
20	LRADC1 (REM_CON)	AI	/	/	Low resolution A/D input 1
21	AVDD	PWR	/	/	Analog Core power pin
22	VDD	PWR	/	/	Digital Core power
23	VCC	PWR	/	/	Digital power pin
24	BAT	I	/	/	Battery Voltage input.
25	DC5V	AI	/	/	5.0V Voltage
26	HOSCI	AI	/	/	High frequency crystal OSC input
27	HOSCO	AO	/	/	High frequency crystal OSC output
28	GND	PWR	/	/	Ground

29	GPIO_F6	BI	10mA	Z	Bit6 of General purpose I/O port F
30	GPIO_F7	BI	10mA	Z	Bit7 of General purpose I/O port F
31	NGND	PWR	/	/	NMOS Ground
32	LXVDD	PWR	/	/	VDD DC-DC pin
33	IO_VDD	PWR	/	Z	IO for VDD DC-DC
34	VDD	PWR	/	/	Digital Core power
35	RESET-	I	/	H	System reset input (active low)
36	MRD-	O	/	H	Ext. memory read strobe
37	MWR-	O	/	H	Ext. memory write strobe
38	RB-	I	/	H	Nand Type flash Ready/Busy status input.
39	GPIO_A0	O	5mA	Z	Bit0 of General purpose I/O port A
	ICEDI	I		/	Data input of DSU
40	GPIO_C0	BI		OD	Bit0 of General purpose I/O port C
	I2C_SCL	O	5mA	/	I2C serial clock (Open drain)
41	GPIO_A1	O	5mA	Z	Bit1 of General purpose I/O port A
	ICECK	I		/	Clock input of DSU
42	GPIO_C1	BI		OD	Bit1 of General purpose I/O port C
	I2C_SDA	O	5mA	/	I2C Serial data (Open drain)
43	GPIO_A2	O	5mA	Z	Bit2 of General purpose I/O port A
	ICEDO	O		/	Data output of DSU
44	GPIO_C2	BI	10mA	Z	Bit2 of General purpose I/O port C
	MMC_CLK1	O		/	Clock1 for MMC/SD Card
	MS_CLK	O		/	Clock for MS Card
45	GPIO_B4	BI	/	Z	Bit4 of General purpose I/O port B
	MMC_CMD	BI		/	CMD of SD/MMC card interface
	MS_BS	O		/	BS of MS card interface
46	ALE	O	/	L	Address latch enable for NAND flash
47	CLE	O	/	L	Command latch enable for NAND flash
48	VCC	PWR	/	/	Digital power pin

49	D7	BI	/	L	Bit7 of ext. memory data bus
50	GPIO_F3	BI	10mA	Z	Bit3 of General purpose I/O port F
	MMC_D3	BI		/	Bit3 of MMC/SD Card data bus
	MS_D3	BI		/	Bit3 of MS Card data bus
51	D6	BI	/	L	Bit6 of ext. memory data bus
52	GPIO_F2	BI	10mA	Z	Bit2 of General purpose I/O port F
	MMC_D2	BI		/	Bit2 of MMC/SD Card data bus
	MS_D2	BI		/	Bit2 of MS Card data bus
53	D5	BI	/	L	Bit5 of ext. memory data bus
54	GPIO_F1	BI	10mA	Z	Bit1 of General purpose I/O port F
	MMC_D1	BI		/	Bit1 of MMC/SD Card data bus
	MS_D1	BI		/	Bit1 of MS Card data bus
55	D4	BI	/	L	Bit4 of ext. memory data bus
56	GPIO_F0	BI	10mA	Z	Bit0 of General purpose I/O port F
	MMC_D0	BI		/	Bit0 of MMC/SD Card data bus
	MS_D0	BI		/	Bit0 of MS Card data bus
57	D3	BI	/	L	Bit3 of ext. memory data bus
58	D2	BI	/	L	Bit2 of ext. memory data bus
59	GPIO_B2	BI	5mA	Z	Bit2 of General purpose I/O port B
	CE4-	O		H	External MROM Chip enable 4
	KEYO0	O		/	Bit0 of key scan circuit output
60	GND	PWR	/	/	Ground
61	D1	BI	/	L	Bit1 of ext. memory data bus
62	D0	BI	/	L	Bit0 of ext. memory data bus
63	GPIO_B0	BI	5mA	Z	Bit0 of General purpose I/O port B
	CE3-	O		H	CE3- of NAND Flash
	KEYI0	I		H	Bit0 of key scan circuit input
64	CE2-	O	5mA	H	Ext. memory chip enable 2
	GPIO_A4	BI		/	Bit4 of General purpose I/O port A.

NOTE:

1: PWR—Power Supply
2: AI——Analog Input
3: AO——Analog Output
4: O——Output
5: I———Input
6: BI——Bi-direction

3. Function Description

3.1 Functional Block Diagram

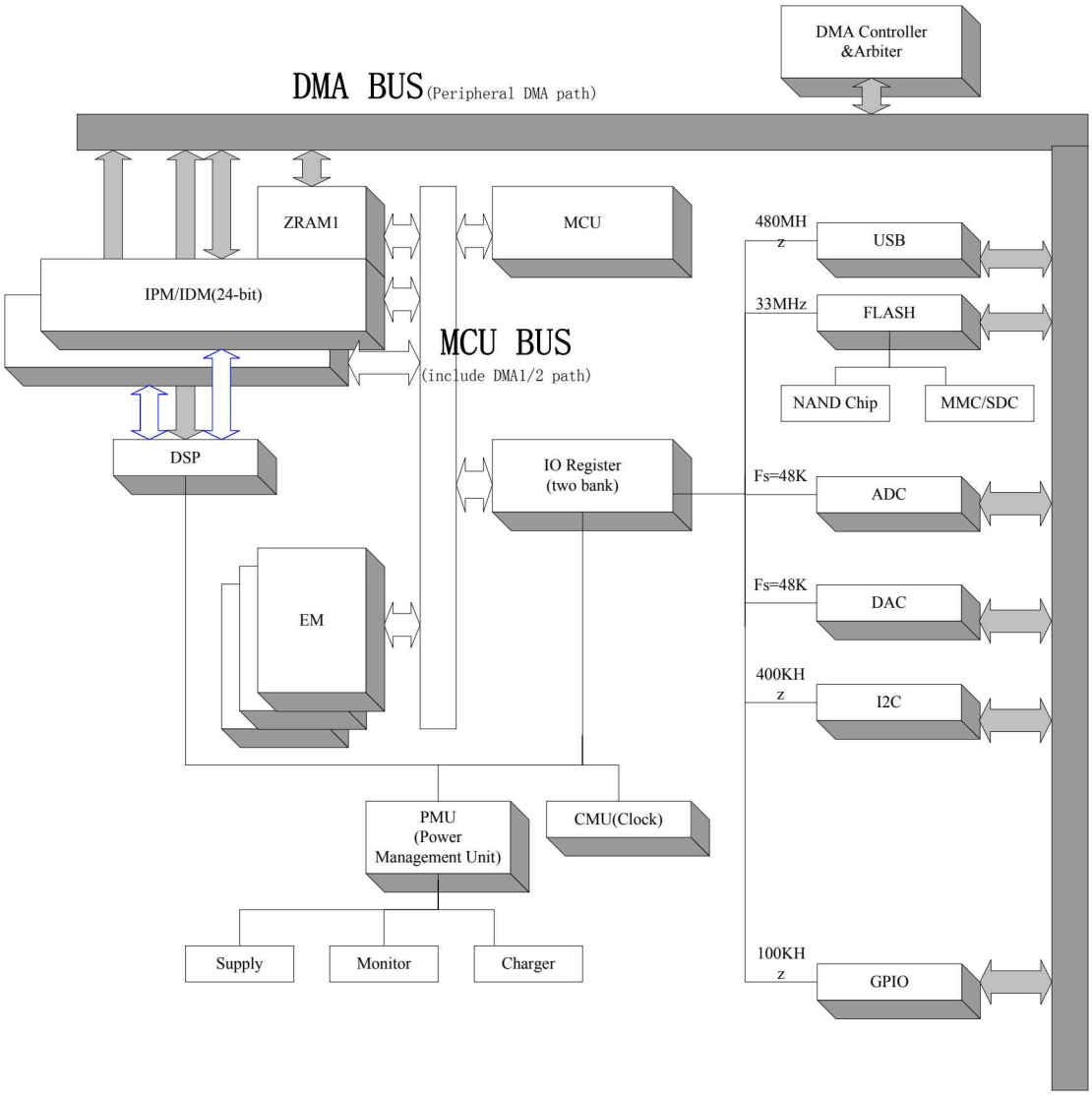


Figure 2: AK2027 Functional Block Diagram

3.2 MCU Core

3.2.1 MCU System Memory Mapping

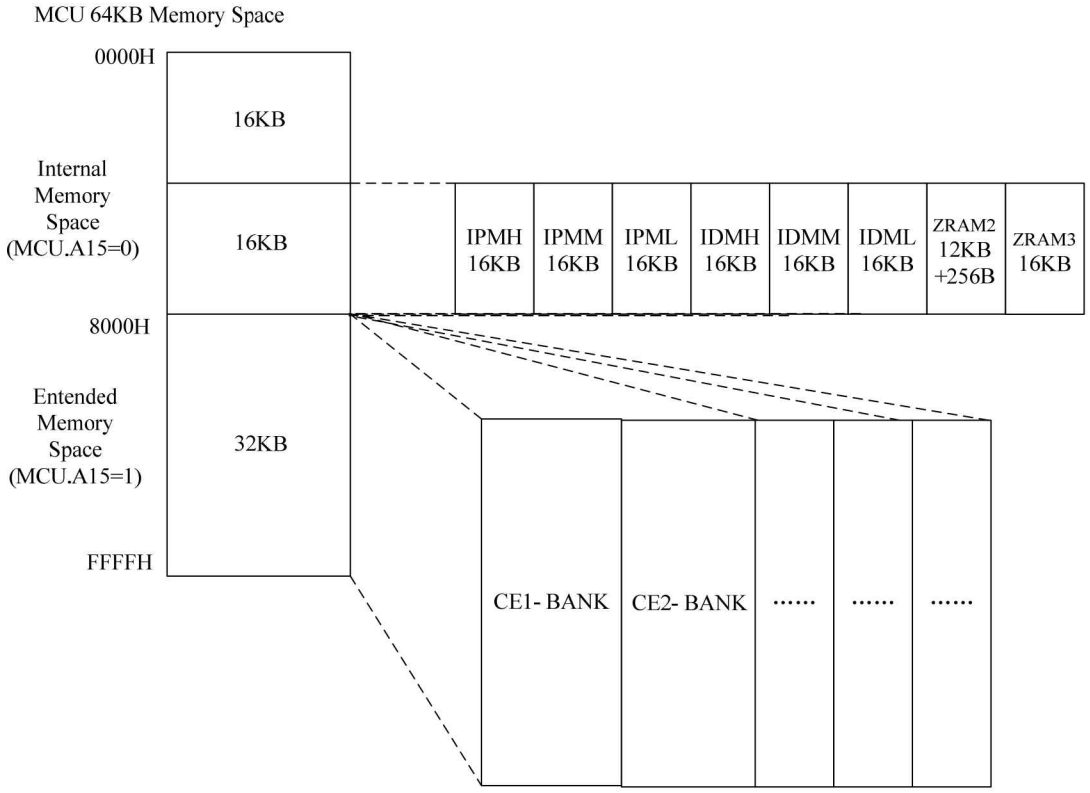


Figure 3: MCU System Memory Mapping

Internal MCU MROM/SRAM memory mapping:

1) (16K-64)byte ZRAM1(IA15=0,IA14=0) : 0000H-3FBFH
2) 8Kbyte B1+B2(IA15=0,IA14=1,IOReg05.[2:0]=111): 4000H-5FFFH
3) (4K+256) byte URAM: 6000H-70FFH, it has synchronization and asynchronism accessing modes.
4) 16Kbyte ZRAM3(IA15=0,IA14=1,IOReg05.[2:0]=011): 4000H-7FFFH
5) 14Kbyte BROM(IA15=1,Reg02=00h, Reg01=00h) : 8000h-B7FFh
6) 21Kbyte TROM1(IA15=1,Reg02=00h,Reg01=02h) : 8000h-D3FFh
7) 12Kbyte TROM2(IA15=1,Reg02=00h,Reg01=03h) : 8000h-AFFFh

Internal DSP IPM/IDM memory mapping:

1) 16K x24bit IPM SRAM : 0000H-3FFFH

2) 16K x24bit IDM SRAM : 0000H-3FFFH

Internal DSP IPM/IDM memory mapping accessed by MCU:

1) 16K x3 byte IPM SRAM : 4000H-7FFFH
2) 16K x3 byte IDM SRAM : 4000H-7FFFH

(Hi/Mid/Low Byte Select and Mapping Mode controlled by IOReg05)

DMA MODE NOTE:

1: When DMA1 and DMA2 are active, MCU will halt, while DMA1 and DMA2 have priority.

2: FLASHDMA or USB DMA is active, MCU will not halt.

3.3 DSP24 Core

This Core is a high performance, programmable Digital Signal Processor (DSP) suitable for a variety of digital audio compounding functions, such as Dolby AC-3 Surround which require large memory provided and the higher accuracy. RDSP24 is a general purpose DSP which can be appended various peripherals circuitry to implement some advanced signal processing algorithms for audio application.

3.4 ZRAM1, ZRAM2 and ZRAM3

Speed: max read time 30 ns from ZRAMRD- going low

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

ZRAM2 is composed of B1,B2 and URAM: 4K+4K+(4K+256). All of them can be operated independently. It has the following modes:

1) MCU running at ZRAM1, while DMA[M] read B1 and DMA[N] write B2. Vise versa.
   M=4,5,6; N=4,5,6 ; M!=N.
2) MCU is running at ZRAM1, while DMA[M] read B2 and DMA[N] write ZRAM3. Vise versa.
   M=4,5; N=4,5 ; M!=N.
3) MCU is running at ZRAM1, while DMA[M] read B1 and DMA[N] write ZRAM3. Vise versa.
   M=4,5; N=4,5 ; M!=N.
4) MCU running at ZRAM1 or ZRAM2 or ZRAM3.

IPM and IDM

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

PM/DM can be accessed by MCU, DSP, DMA1, DMA2, DMA4 and DMA5.

When DSP is accessing the high (low) 8Kbytes, MCU/DMA1,2,4,5 can access low (high) 8K

bytes at the same time.

3.5 USB2.0 SIE

The Artek USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. In high-speed mode this device is capable of transmitting or receiving data up to 480Mbps.This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU, RAM, ROM and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

3.6 NAND Flash /SMC Controller

The NAND Flash/SMC controller is a configurable interface to external NAND Flash/SMC. The highly configurable and flexible interface can attach to using most of readily available NAND Flash device. The flash data bus can be configured to be 8-bit access.

The controller automatically generates the Reading, Programming and Other commands timing by proper CLE, ALE and CE controls. So reliable data transferring between the Int. RAM and ext. Flash by MCU or DMA is available.

3.7 MMC/SD Interface

Multimedia Card/SD need serial input/output interface to send command and receive data. The timing is indicated by the following figure:

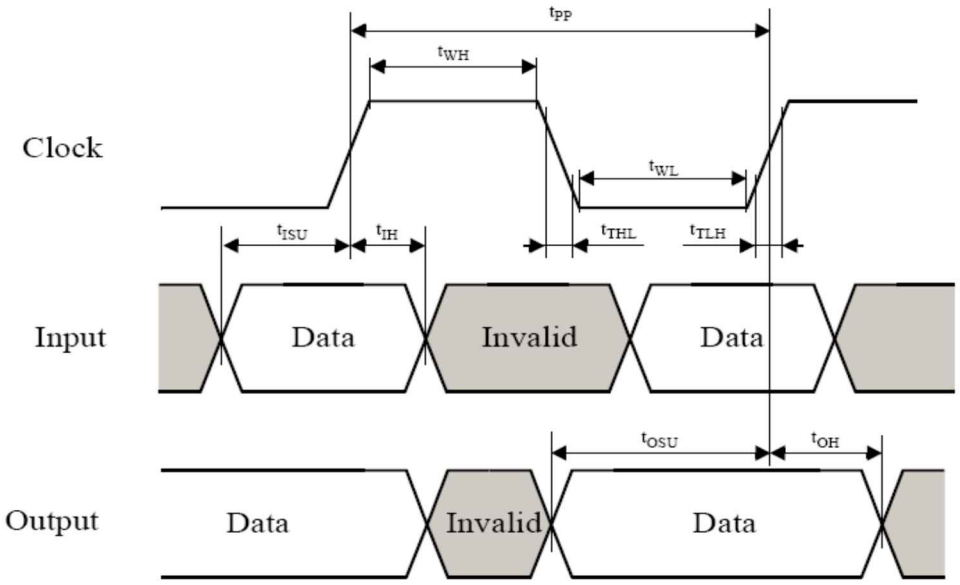


Figure 4: MMC/SD Interface Timing

Table 2: Card interface timings

Parameter	symbol	Min	Max	unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	26/52	MHz	CL<=30pF(tolerance +100KHz)
Clock frequency identification Mode(Open Drain)	fOD	0	400	KHz	Tolerance:+20KHz
Clock low time	tWL	6.5		ns	CL<=30pF
Clock rise time	tTLH		3	ns	CL<=30pF
Clock fall time			3	ns	CL<=30pF
Inputs CMD DAT(reference to CLK)					
Input setup time	tISU	3		ns	CL<=30pF
Input hold time	tIH	3		ns	CL<=30pF
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	5		ns	CL<=30pF
Output hold time	tOH	5		ns	CL<=30pF
Signal rise time	trise		3	ns	CL<=30pF
Signal fall time	tfall		3	ns	CL<=30pF

Table 3: Bus signal Line Load

Parameter	Symbol	Min	Recommend	Max	Unit	Remark
Pull up resistance for CMD	Rcmd	4.7	10	100	KOhm	To prevent

						bus floating
Pull up resistance for dat0-7	Rdat	50	50	100	KOhm	To prevent bus floating
Bus signal line capacitance	CL			30	pF	Single card
Signal card capacitance	Ccard			7	pF	
Maximum signal line inductance				16	nH	Fpp<=52MHz

CL=CHost+Cbus+Ccard

3.9 General Purpose IO Ports

AK2027 has GPIOA, GPIOB, GPIOC and GPIOF. Most of them are multiplexed function pins as the following table shows:

Table 4: GPIO Modes

GPIO	F1 (CE0S=H default)
GPIO_A0	GPIO_A0/ICEDI
GPIO_A1	GPIO_A1/ICECK
GPIO_A2	GPIO_A2/ ICEDO
GPIO_A4	CE2-/GPIO_A4
GPIO_B0	GPIO_B0/CE3-/ KEYI0
GPIO_B2	GPIO_B2/CE4-/ KEYO0
GPIO_B4	GPIOB4/MMC_CMD/MS_BS
GPIO_C0	GPIO_C0/I2C_SCL/ICEEN-
GPIO_C1	GPIO_C1/I2C_SDA /ICERST-
GPIO_C2	GPIO_C2/MMC_CLK1/MS_CLK
GPIO_F0	GPIO_F0/MMC_D0/MS_D0
GPIO_F1	GPIO_F1/MMC_D1/MS_D1
GPIO_F2	GPIO_F2/MMC_D2/MS_D2
GPIO_F3	GPIO_F3/MMC_D3/MS_D3
GPIO_F6	GPIO_F6
GPIO_F7	GPIO_F7

3.9 HOSC/PLL

AK2027 supports 24Mhz crystal which is the system clock source.

A low jitter PLL referenced to 24MHz is used to generate clock for DSP and for serial communication protocols such as USB, UART, etc. The clock used in serial communications is 48MHz. Another PLL referenced to 24MHz is used to generate 22.5792MHz for sample rate 44.1K/22.05KHz/11.025KHz and 24.576MHz for audio sequence of 48Khz.

3.10 PMU/DC-DC

3.10.1 DC-DC converters and regulators

There are one on-chip DC-DC converter and two Regulators. DC-DC2 converter can work in Buck mode for different input voltage. DC-DC2 converter works in PFM or PWM modulation for different load current.

Table 5: Power mode configuration

PWRM	DC5V>4.3V	DC-DC1	Regulator1	DC-DC2	IO_VDD	Regulator2	Description
1	0	N	Y	Buck	BAT	N	Li+, 1 Inductor
X	1	N	Y	N	-	From VCC	USB

3.10.2 Battery monitor

There is a low speed 6-bit A/D for Battery monitor and wire control.

The relationship between battery type and the A/D input range is:

Table 6: Relationship between Battery Type and A/D Input Range

Battery type	Internal Voltage divider for battery	Battery Voltage Range
1 Li+	1/2	1.4-4.2

3.11 A/D, D/A, IIS Port and Headphone Driver

3.11.1 D/A Interface

AK2027's internal D/A is an on-chip Sigma-Delta Modulator, a high performance D/A is composed of it. The D/A interface support 8-level play back FIFO (16 X 24-bit PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256XFS clock for over-sampling, while 24.576MHz supports 48K/32K/24K/16K/12K/8K Hz with 256XFS for over-sampling.

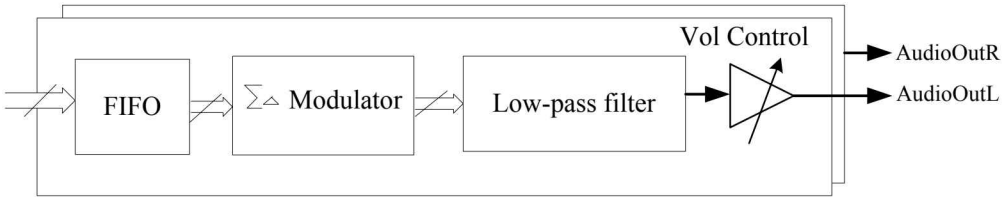


Figure 5: D/A Block Diagram

Internal D/A can drive earphone directly and the pin PAVCC need a bypass capacitor about 22uF to eliminate the "PENG" when D/A is powered on or off. D/A includes an analog mixer, reference to the ADDA block diagram.

3.11.2 A/D

The internal microphone amplifier has gain for recording. The VMIC pin is the power supply (2.2V) for microphone.

The audio A/D is a 21 bits sigma delta Analog-to-Digital Converter. Its input source can be selected from MIC amplifier or external FM, and it has two FIFOs.

The FS Supports 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 7: Absolute Max Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	1.6	-0.3~2.0	V
	VCC	3.0	-0.3~3.6	V
Input voltage	V_I		-0.3~3.6	V
Storage temperature	T_{stg}	25	-65~150	℃

Note:

1. T_O = 25℃（Operating Temperature）
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

4.2 Capacitance

Table 8: Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T_O = 25℃, VCC = 0 V.

4.3 DC Characteristics

Table 9: DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -6 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 6 mA			0.4	V
High-level input voltage	V_{IH}		0.6*VCC		VCC+0.6	V
Low-level input voltage	V_{IL}		-0.3		0.4*VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V		±25		uA
Tri-State leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V		±25		uA
GPIO Drive	Idrive1			5		mA
	Idrive2			10		mA
	Idrive3			15		mA

NOTES:

1. T_o = -10 to +70℃, VDD = 1.6 V, VCC = 3.0 V
2. GPIO should not be floating in order to reduce the standby current, refer to the Application Note for the detailed information.
3. There are three types of GPIO drives ranging from 5mA to 15mA, refer to the Section 2.2 Pin Definition for the detailed information.

4.4 AC Characteristics

T_o = -10 to +70℃

4.4.1 AC Test Input Waveform

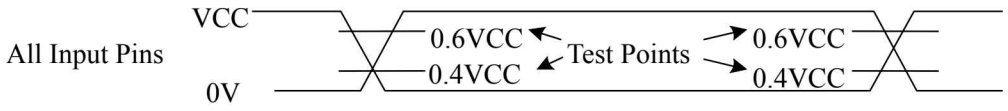


Figure 6: AC Test Waveform

4.4.2 AC Test Output Measuring Points

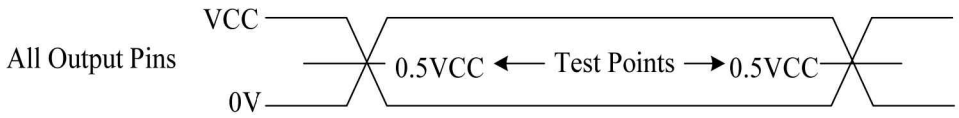


Figure 7: AC Test Output Measuring Points

4.4.3 Reset Parameter

Table 10: Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	50	—	us

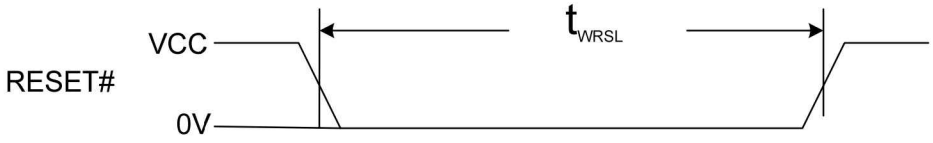


Figure 8: Reset Parameter

4.4.4 Initialization Parameter

Table 11: Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}		—	61.04	us
Output delay time (from RESET#)	t_{OD}		61.04	—	us

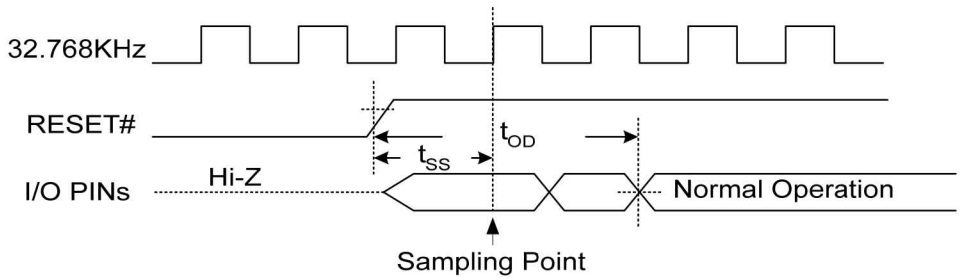


Figure 9: Initialization

4.4.5 GPIO Interface Parameter

Table 12: GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$11/f_{mcuclk}$		s
GPIO output rise time	t_{GPRISE}		5	50	ns
GPIO output fall time	t_{GPFALL}		5	50	ns
Output level width	t_{GPOUT}		$11/f_{mcuclk}$		s

Notes 1. f_{MCUCLK} is the frequency that MCU is running upon.

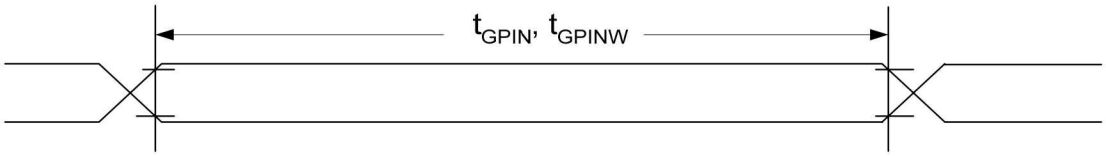


Figure 10: Input Level Width

Figure 11: Output Rise/Fall Time

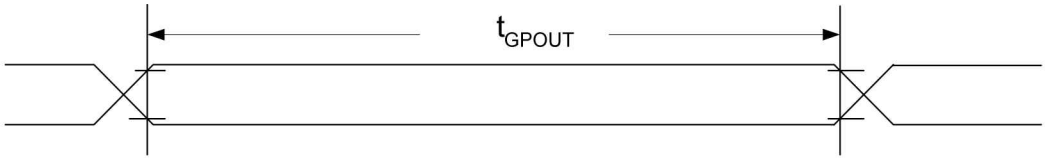


Figure 12: Output Level Width

4.4.6 Ordinary ROM Parameter

Table 13: Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	90		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	90		ns
Data input setup time	t_{DS}	HOSC=24MHz	40		ns
Data input hold time	t_{DH}	HOSC=24MHz	15		ns

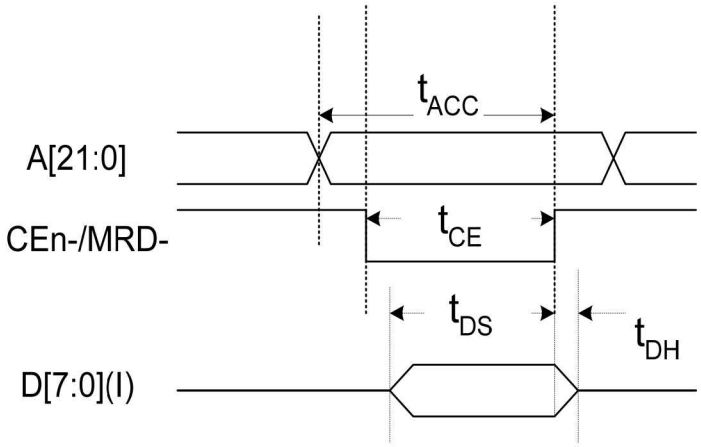


Figure 13: Ordinary ROM

4.4.7 External System Bus Parameter

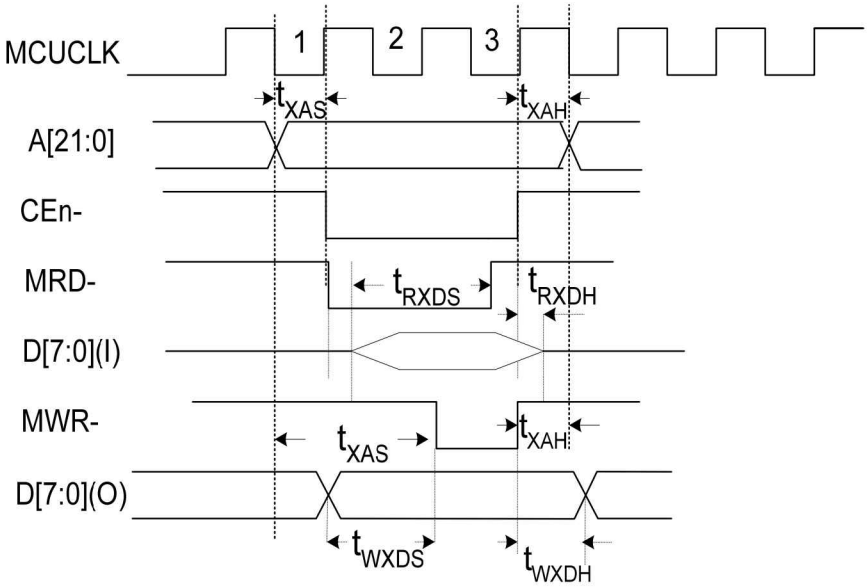


Figure 14: External System Bus Parameter

Table 14: External System Bus Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	10		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

4.4.8 Bus Operation

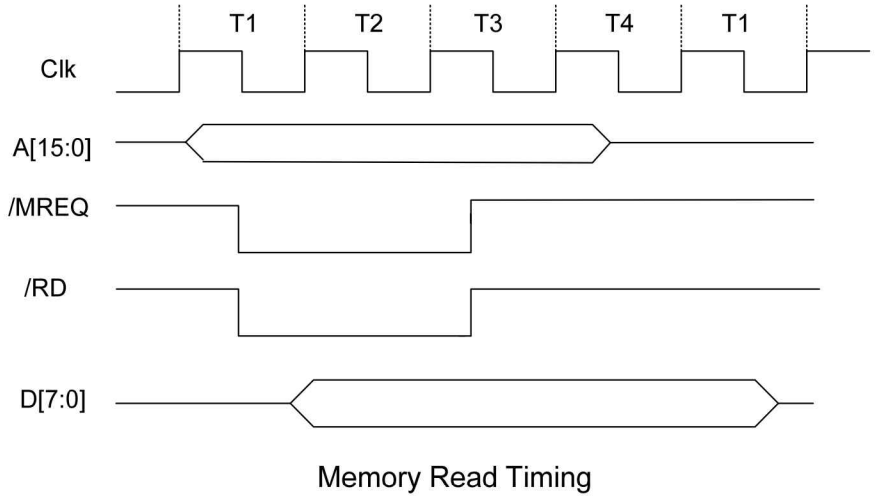


Figure 15: Memory Read Timing

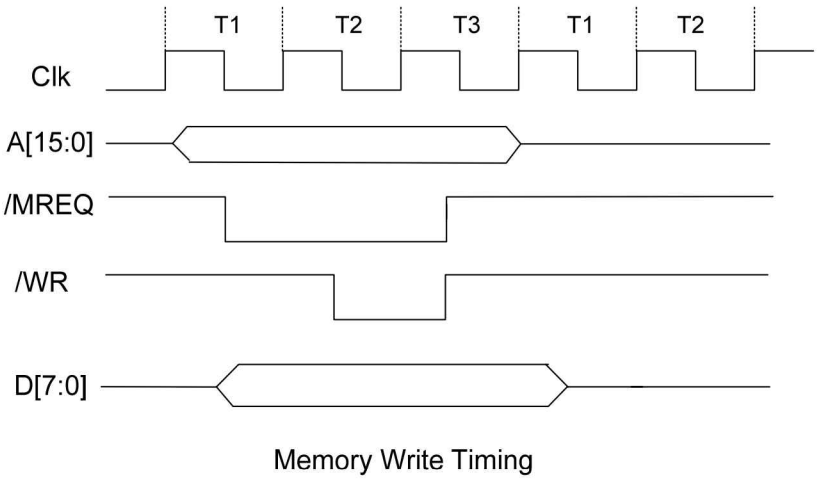


Figure 16: Memory Write Timing

4.4.9 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 2.0 V, VCC = 3.3V, Sample Rate=48KHz)

Table 15: A/D Converter Characteristics

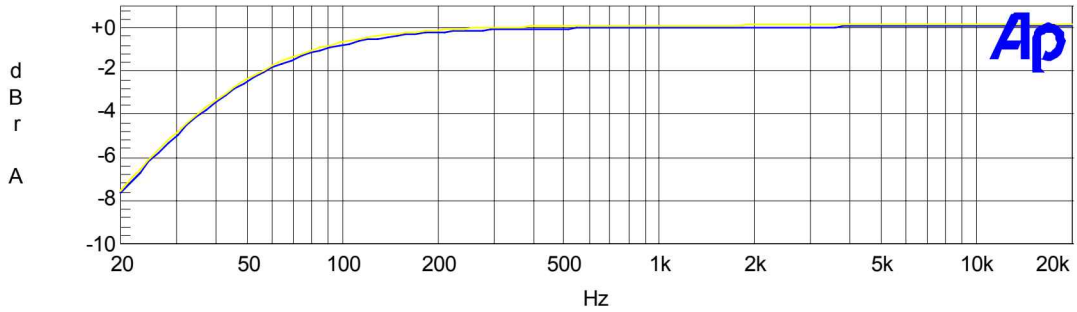
Characteristics	Min	Typ.	Max	Unit
Dynamic range		87.0		dB
Total Harmonic Distortion + Noise		85.0		dB
Frequency Response (20-13KHz)			±0.98	dB
Full Scale Input Voltage(Gain=0dB)		2.7		Vpp

4.4.10 Headphone Driver Characteristics Table

Table 16: Headphone Driver Characteristics

(T_o =-10 - +70℃, VDD = 1.6 V, VCC = 3.0 V, Sample Rate=32KHz, Volume Level=0x1F)

Characteristics	Min	Typ	Max	Unit
Dynamic Range –60 dBFS Input		-87		dB
Total Harmonic Distortion + Noise		-81		dB
Frequency Response 20-20KHz	-7.6	0		dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.3		Vpp
Inter channel Gain Mismatch(1KHz)		-66		dB



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.Level A	Left	
1	3	Yellow	Solid	1	Anlr.Level B	Left	

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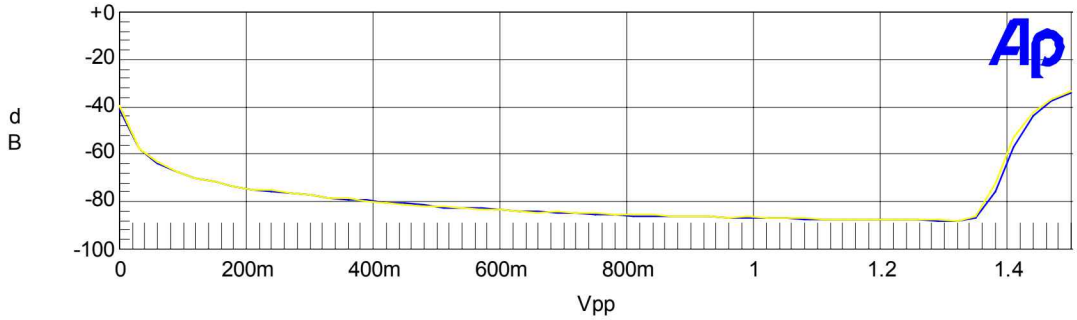
Figure 17: Frequency Response Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	
1	2	Yellow	Solid	1	Anlr.THD+N Ratio	Left	

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Figure 18: THD + N Amplitude Diagram of Headphone Driver

4.4.11 LCM Driver Parameter

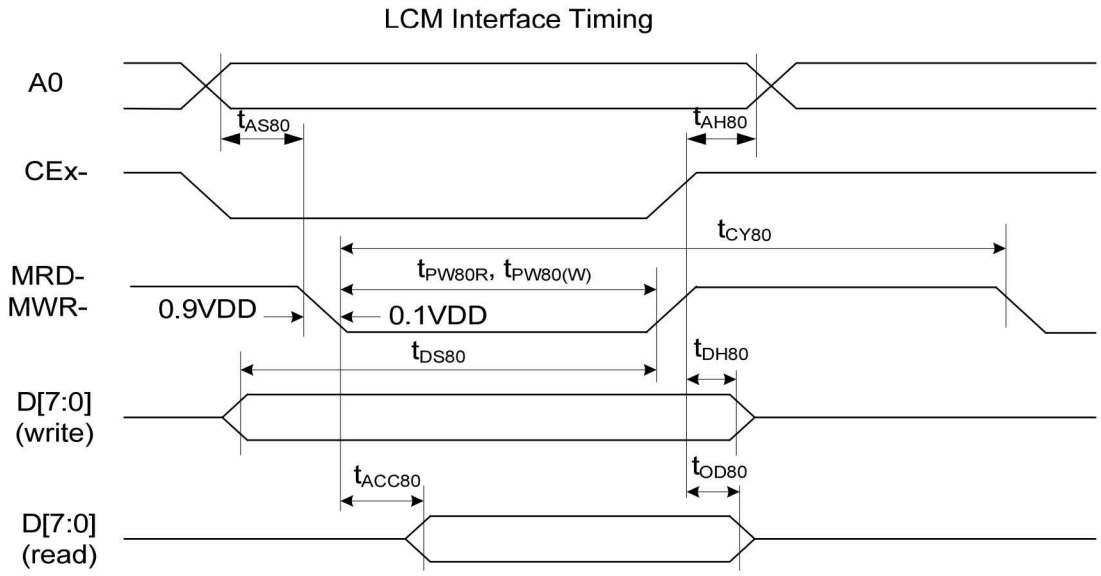


Figure 19: LCM Interface Timing

Table 17: LCM Driver Parameter

Parameter	Symbol	Condition	Typ	Unit
Data access time(write)	$t_{PW80(W)}$	HOSC=24MHZ	29	ns
Data access time (Read)	$t_{PW80(R)}$	HOSC=24MHZ	67	ns
Write cycle time	$t_{CY80(W)}$	HOSC=24MHZ	407	ns
Read cycle time	$t_{CY80(R)}$	HOSC=24MHZ	284	ns
Data setup time	t_{DS80}	HOSC=24MHZ	79	ns
Data hold time	t_{DH80}	HOSC=24MHZ	8	ns
Address setup time	t_{AS80}	HOSC=24MHZ	11	ns
Address hold time	t_{AH80}	HOSC=24MHZ	11	ns
Read access time	t_{ACC80}	HOSC=24MHZ	13	ns
Data input hold time	t_{OD80}	HOSC=24MHZ	8	ns

5. Soldering Conditions

5.1 Recommended Soldering Conditions

Table 18: Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions
Infrared Ray Reflow	Peak package's surface temperature: 235℃ (Lead) or 260℃ (Lead Free)
	Reflow time: 30 seconds or less (210℃or more)—(Lead) or 60 seconds or less (217℃or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note:

The maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution:

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

5.2 Precaution against ESD for Semiconductors

When the strong electric field is exposed to a MOS device, the destruction of the gate oxide may occur and then it can ultimately degrade the device operation. Measures must be taken to stop the generation of static electricity as many as possible, and it is a must to

quickly dissipate the static electricity when it occurs. Environmental control must be adequate enough. Humidifier should be used when it is dry. Recommend to avoid using insulators, which may easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container or a static shielding bag or objects made from conductive material. All test and measurement tools including work bench and floor should be grounded. The operator shall be grounded by using wrist strap. Semiconductor devices shall not be touched with bare hands. Similar precautions shall be taken for PW boards with semiconductor devices on it.

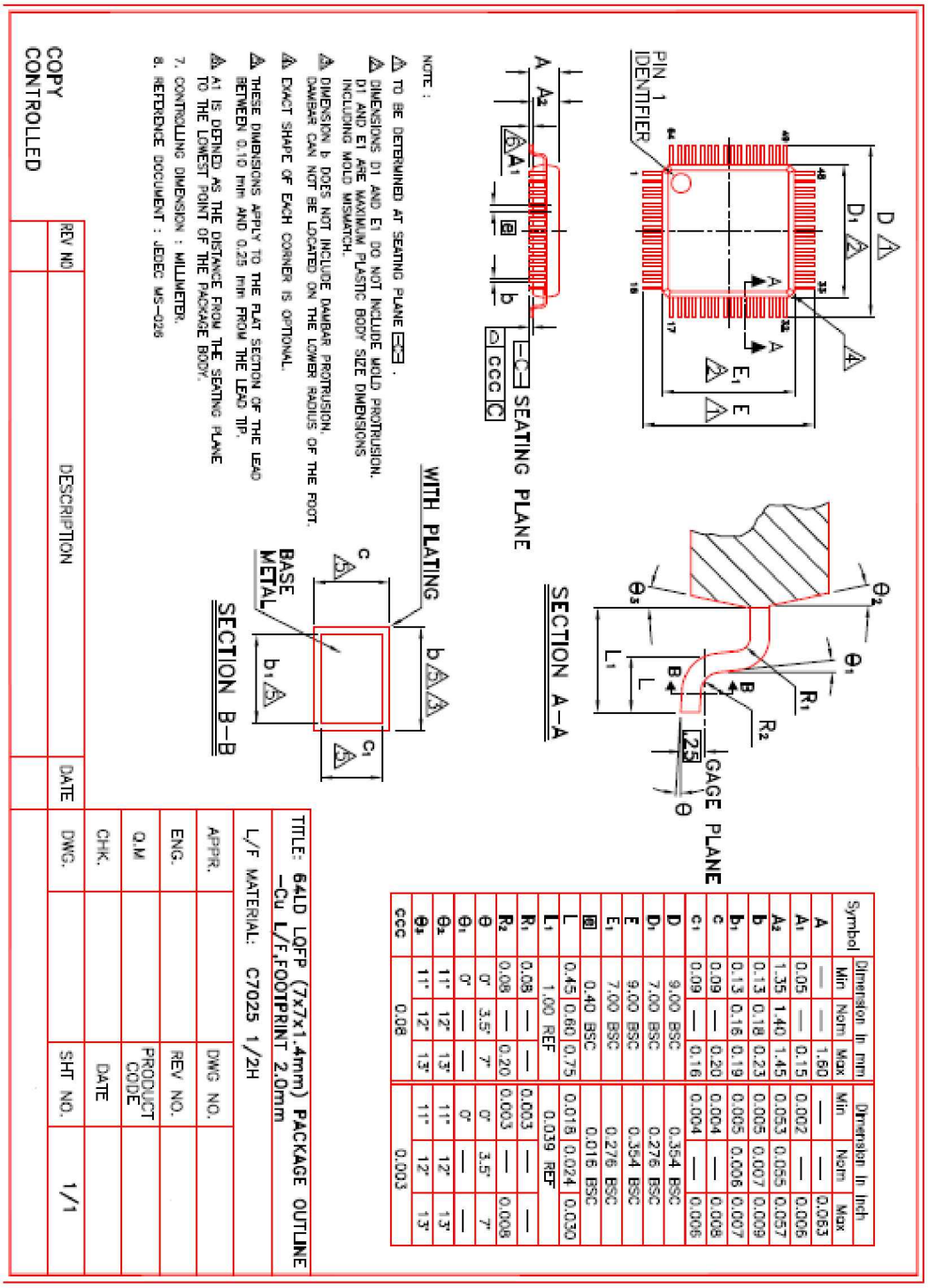
5.3 Handling of Unused Input Pins for CMOS

The cause for no connection to CMOS device inputs can be the malfunction. If no connection is provided for the input pins, the possible cause is that an internal input level may be generated due to noise, etc., which results in malfunction. CMOS devices behave differently from Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin shall be connected to VDD or GND with a resistor, if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device and follows the related specifications governing the devices.

5.4 Status before Initialization of MOS Devices

Power-on does not necessarily define the initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned on, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after the power-on.

6 AK2027 Package Drawing



Symbol	Dimension in mm			Dimension in Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

Figure 20: AK2027 Package Drawing

7 Appendix

7.1 Acronym and Abbreviations

ACK—Acknowledgement

ADC—Analog Digital Converter

ATAIRQ—Advanced Technology Attachment Interrupt Request

CTC—Counter/Timer Channels

DAC—Digital Analog Converter

DMA—Direct Memory Access

DRQ—Data Request

DST—Destination

ECC—Error Correction Code

EM—External/Extended Memory

FIFO—First In First Out

HIP—Host Interface Port

HOSC—High Frequency Oscillator

IDM—Internal Data Memory

IPM—Internal Program Memory

IRQ—Interrupt Request

IR—Infra-red

LOSC—Low Frequency Oscillator

MIC—Microphone

NAK—Negative Acknowledgement

PLL—Phase Locked Loop

RTC—Real Time Clock

RB—Ready/Busy

SIRQ—System external Interrupt Request

SPDIF—Sony/Philips Digital Interface

SPI—Serial Port Interface

SRC—Source

TC—Transmit Complete

UART—Universal Asynchronous Receiver/Transmitter