ASAHI KASEI®

AK2351

Integrated Base Band LSI for Cordless Telephone Sets

Features

- ☐ Integrated voice band filters with MSK MODEM(2400bps) and COMPANDOR for cordless telephone sets
- ☐ Low voltage operation (2.8V～3.3V)
- ☐ Fully integrated COMPANDOR, only two external capacitors are required
- ☐ Buffer amplifier for direct drive of a ceramic receiver is available
- ☐ Switchable expander reception level (0/+6dB)
- ☐ Carrier detection
- ☐ Transmission and reception voice mute
- ☐ Limiter level is externally adjustable
- ☐ Gain setting amplifiers are available both for receiver and transmitter sections
- ☐ Power down mode
- ☐ 3.58MHz oscillator
- ☐ Preemphasis/Deemphasis circuits bypass control
- ☐ Scrambler chip interface
- ☐ Low power CMOS
- ☐ Minimal external components
- ☐ Packaged in 44 pin QFP

General Description

AK2351 is an integrated base band LSI for cordless telephone sets. Not only voice band filters but also a 2400bps MSK MODEM (for data communication) and a COMPANDOR (for noise reduction) are integrated into monolithic CMOS LSI.

The COMPANDOR circuit is fully integrated. Therefore, only an external capacitor is required for each compressor and expander. The fully integrated COMPANDOR is also free from aging problem.

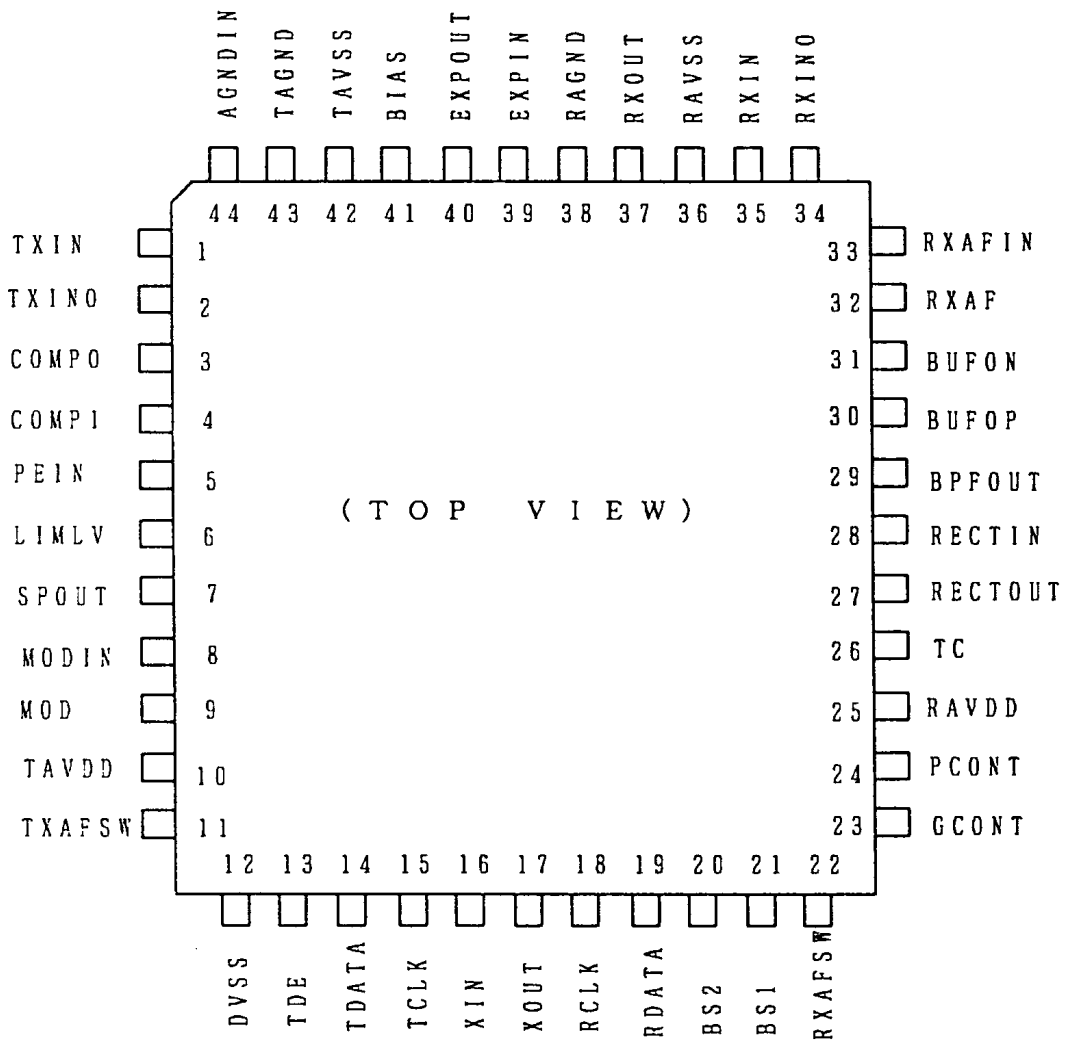
The 2400bps MSK MODEM can assure reliable high speed data communication. A 3.58MHz oscillator circuit is integrated, which may also be used for DTMF tone generator clock. No special clock is required for the MSK MODEM.

Scrambler chip interface and preenpasis/deenphasis circuits bypass mode are available for easy interface with external scrambler device.

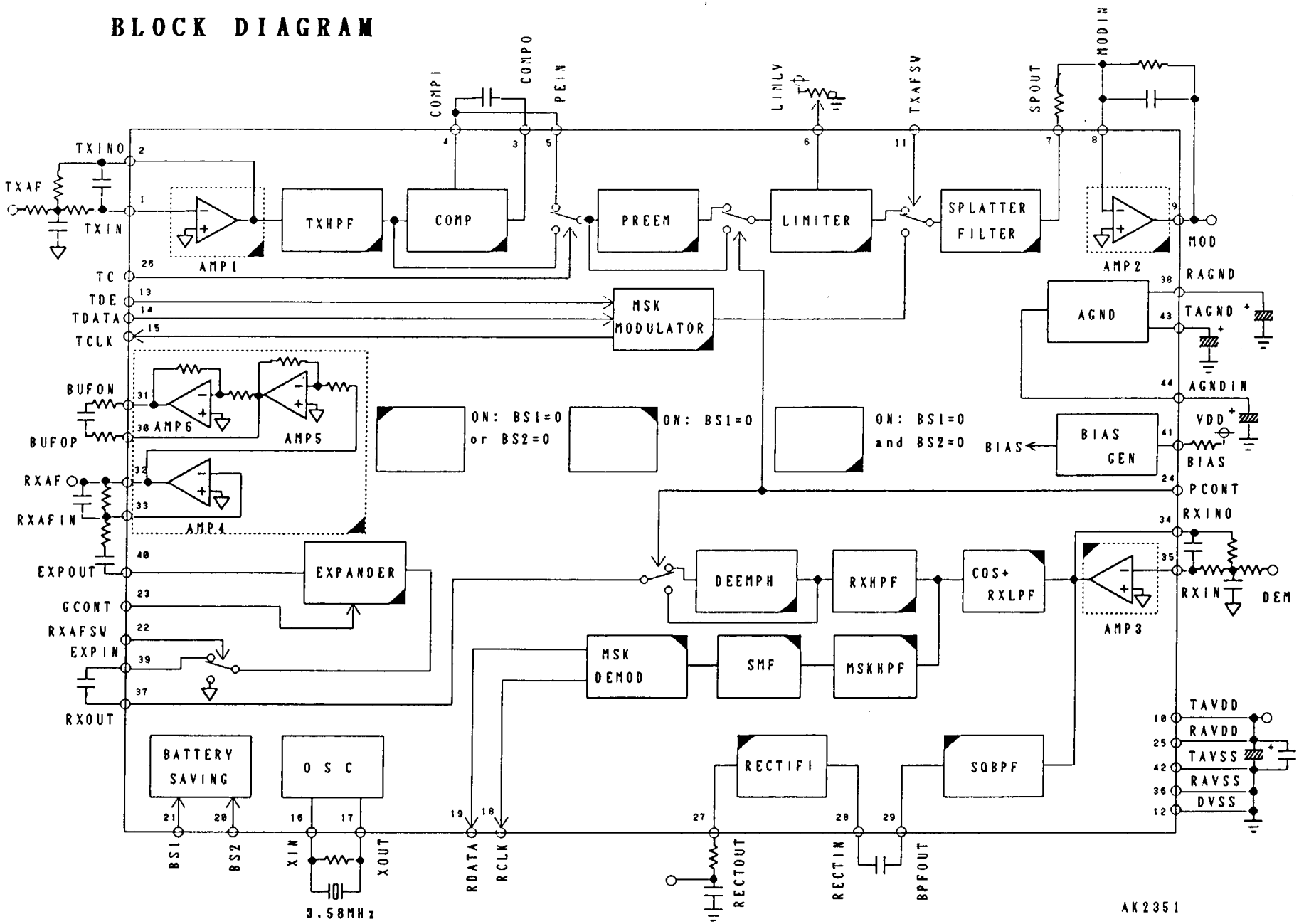
High-pass filter, compressor, pre-emphasis, limiter, MSK modulator, splatter filter, etc. are integrated for transmitter.

Band-pass filter, de-emphasis, expander, buffer, MSK demodulator, etc. for voice/data, and band-pass filter, rectifier, etc. for the squelch are integrated for receiver.

Pin Assignments



BLOCK DIAGRAM



Circuit Configuration

Functional Block	Functions
AMP1	Op Amp for gain adjustment of voice signal to be transmitted and for the anti-aliasing filtering for the succeeding switched capacitor filter (SCF). Adjust the gain to be within 10~30dB and the filter cut-off frequency to be around 10KHz by properly selecting external capacitor and resistor values.
TxHPF	SCF high pass filter to eliminate lower than 300Hz components contained in the transmitted voice signal.
Compress--or	To compress the amplitude of the transmitted voice signal.
Emphasis	To emphasize the high frequency components in the transmited voice signal in order to improve the signal-to-noise performance of the modulated signal.
Limitter	Amplitude limitting circuit to limit the maximum frequency deviation by the modulated signal. Limitter level is adjustable by varying DC level applied on "LIMLV" pin. The limitter level is set to a pre-fixed level if "LIMLV" pin is left open.
Splatter Filter	SC filter to reject higher than 3KHz components contained in the limitter output signal or MSK Modulator signal.
AMP2	Op Amp to form a smoothing filter for the transmitter SCF output. Adjust the gain to be 0dB and set the cut-off frequency to be around 10KHz by properly selecting external capacitor and resistor values.
MSK Modulator	Modulator to generate 2400bps MSK signal in accordance with digital input signal applied on TDATA pin. "H" : 1.2KHz "L" : 2.4KHz
AMP3	Op Amp for gain adjustment of demodulated received signal and for the anti-aliasing filtering for the succeeding SC filter. Adjust the gain to be within 10~20dB and set the cut-off frequency to be around 40KHz by properly selecting external capacitor and resistor values.
COS + RxLPF	SC filter to reject higher-than-3KHz components contained in the demodulated, received signal.
RxHPF	SC filter to reject lower-than-300Hz components contained in the received voice signal.
De-Emphasis	To equalize back the pre-emphasized signal to flat level.
Expander	To expand the signal amplitude compressed by the compressor circuit to flat scale. GCONT pin selects the expander gain of either 0dB or 6dB.

Functional Block	Function
AMP4	Op Amp to form a smoothing filter for the receiver SCF output. Adjust the gain to be 0dB and set the cut-off frequency to be around 20KHz by properly selecting external capacitor and resistor values.
MSK HPF	SC filter to reject lower-than-100Hz components contained in the received MSK signal.
SMF	Active filter to smooth out the output signal from the MSK HPF.
MSK Demodulator	To Recover 2400 Bps receive data and clock from the MSK signal fed on RXIN pin. 1.2KHz : "H" 2.4KHz : "L"
SQ BPF	SC filter to pick up the 20KHz components from the received, demodulated signal for squelch control. The filter has 30dB gai
Rectifying Circuit	Full-wave rectifying circuit to rectify SQ BPF out put signal.
AMP5 AMP6	Inverting, non-inverting buffers to directly drive a ceramic receiver. 220 OHM resistors are recommended to insert between these buffer outputs and the receiver terminals for phase compensation.
BIAS GEN	Bias generator circuit for internal Op Amps.
AGND	Ground Reference voltage generator circuit for internal analog signal processing.
OSC Circuit	A 3.58MHz reference clock generator with an external quartz Crystal resonator and a resistor.
Battery Saving	Battery save mode selection circuit. 1 of 4 modes is selectable by BS1 & BS2 pins.

Pin/Function Descriptions

Pin#	Name	I/O	Function
1	TXIN	I	Transmit voice signal input pin (inverted input pin of AMP1). With external capapcitors and resistors, a microphone AMP is formed.
2	TXINO	O	Output pin of AMP1.
3	COMPO	O	Compressor output pin. Can drive 50k ohm load or more.
4	COMPI	I	Compressor rectifier input pin. This should be connected to COMPO pin through an external capacitor. Input impedance of the pin is 150k ohm or more.
5	PEIN	I	Preenphasis input pin. The output from the scrambler chip is connected to this pin. Should be connected to COPI if the scrambler is not used.
6	LIMLV	I	Limitter level adjust pin. Limitter level is adjustable by varying the DC level applied on this pin. If this pin is left open, a pre-determined level is set.
7	SPOUT	O	Splatter filter output pin.
8	MODIN	I	Transmit signal input pin to be modulated (inverted input pin of AMP2). With external capacitor and resistors, a smoothing filter is formed.
9	MOD	O	Transmit signal output pin to be modulated. Can drive 10k ohm load or more.
10	TAVDD	-	Positive power supply pin for transmit section.
11	TXAFSW	I	Transmit signal select pin (with built-in pull-up) "H" : MSK signal "L" : Voice signal
12	DVSS	-	Negative power supply pin for digital circuit.
13	TDE	I	Transmit MSK signal control (built-in pull-up) "H" : MSK signal off (MUTE) "L" : MSK signal on
14	TDATA	I	Transmit MSK data input pin (with built-in pull-up). Data is synchronously read at the rising edge of TCLK clock.
15	TCLK	O	Clock output pin for transmit MSK data (open-drain output). 2.4KHz clock is output when TDE pin is "LOW". It stays "HIGH" when TDE is "HIGH".
16 17	XIN XOUT	I O	Quatz Crystal resonator pins. By connecting a 3.58MHz resonator and 1 MEG OHM resistor between these pins, a reference clock is generated. For external clock operation, connect XIN pin to DVSS and external clock source to XOUT pin.

Pin#	Name	I/O	Function
18	RCLK	O	Clock output pin for receive MSK data (open-drain output). A 2.4KHz clock is output which is derived from the received MSK signal.
19	RDATA	O	Receive MSK data output pin (open-drain output). Data is synchronously output at the falling edge of RCLK clock.
20 21	BS2 BS1	I I	Battery save control pins (with built-in pull-ups). BS1 BS2 "H" "H" : Mode 0 (Refer to Block Diagram) "H" "L" : Mode 1 "L" "H" : Mode 2 "L" "L" : Mode 3
22	RXAFSW	I	Received voice signal control pin (with built-in pull-up). "H" : Received voice signal off (MUTE) "L" : Received voice signal on
23	GCONT	I	Expander gain control pin (with built-in pull-up) "H" : 0dB "L" : 6dB
24	PCONT	I	Emphasis/deemphasis circuits bypass controle pin. "H" : Normal mode "L" : Bypass mode
25	RAVDD	-	Positive power supply pin for analog receiver section.
26	TC	I	Compressor bypass controle pin (with built-in pull-up) "H" : Normal mode "L" : bypass mode
27	RECTOUT	O	Rectifier output pin for squelch circuit. Can drive 50k ohm load or more.
28	RECTIN	I	Rectifier input pin for squelch circuit.
29	BPFOUT	O	Band pass filter output pin for squelch circuit. Can drive 50k ohm load or more.
30 31	BUFOP BUFON	O O	Ceramic receiver buffer amp output pins. Connect a ceramic receiver to these pins via 220 OHM resistors.
32	RXAF	O	Received voice signal output pin. Can drive 10k ohm load or more.
33	RXAFIN	I	Received voice signal input pin (inverted input of AMP 4). A smoothing filter is formed with external capacitors and resistors.
34	RXIN0	O	AMP3 output pin.
35	RXIN	I	Received de-modulated signal input pin (inverted input of AMP3). A pre-filter is formed with external capacitors and resistors.
36	RAVSS	-	Negative analog power supply for receiver section.

Pin#	Name	I/O	Function
37	RXOUT	O	Received voice filter output pin. Can drive 50k ohm load or more.
38	RAGND	O	Analog ground pin for receiver section. An external capacitor should be connected to this pin to stabilize the analog ground.
39	EXPIN	I	Expander input pin. Input impedance of the pin is 150k ohm or more.
40	EXPOUT	O	Expander output pin.
41	BIAS	I	Bias resistor pin. A specified resistor is connect between VDD and this pin.
42	TAVSS	-	Negative analog power supply pin for transmitter section.
43	TAGND	O	Analog ground pin for transmitter section. An external capacitor is connected to this pin to stabilize the analog ground.
44	AGNDIN	I	Analog ground input pin. An external capacitor is connected to this pin to stabilize the analog ground.

Absolute Maximum Ratings

TAVSS, RAVSS, DVSS=0V ; (Note①)

Parameter	Symbol	Min	Max	Units
Power Supply Voltages (TVAA, RAVDD)	VA+	-0.3	7	V
Input Current (Excluding power supply pins)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	(VA+)+0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VD+)+0.3	V
	V_{INDD} (Note②)	-0.3	7	V
Storage Temperature	Tstg	-55	130	℃

Notes ① : All voltages are referenced to VSS pin
② : TCLK, RCLK, RDATA

Note : Exceeding absolute maximum ratings may cause permanent damage.

Recommended Operating Conditions

TAVSS, RAVSS, DVSS=0V ; (Note①)

Parameter		Symbol	min	typ	max	Units
Ambient Operating Temp.		Ta	-10		70	℃
PowerSupply Voltage : (TAVDD,RAVDD)	R_{BIAS}=150KΩ	VDD	2.8	3.0	3.3	V
	R_{BIAS}=220KΩ				4.0	
Analog Ground Reference Voltage		AGND		1/2VDD		V
Power Supply Current	Mode0	Idd0		0.5	1.0	mA
	Mode1	Idd1		1.1	2.1	
	Mode2	Idd2		1.3	2.8	
	Mode3	Idd		4.2	8.4	

Note① : All voltages are referenced to VSS pin.

Analog Characteristics

0dBm=0.775Vrms

1) TX Section

Parameter		min	typ	max	Units
Reference Input Signal Level	@TXIN0		-10		dBm
Absolute Gain	TXIN0→MOD 1KHz (Note①)	-1.5	0	1.5	dB
Limitter Level	TXIN0→MOD 1KHz (Note①) (VDD=3V without External R)	-9	-8	-7	dBm
	(Adjustable Range with R)			-7	
Noise Level	TXIN→MOD (Note①)			-62	dBm
MSK Output Signal Level	TDATA→MOD (Note①) (VDD=3V, 1.2KHz Output)	-9	-8	-7	dBm
MSK Signal Distortion	TDATA→MOD (Note①) (VDD=3V, 1.2KHz Output)			-32	dB

Note① : Bypassing Compressor and including Preemphasis with external RC smoothing filter (fc=10KHz, 0dB Gain).

2) RX Section

Parameter		min	typ	max	Units
Reference Input Signal Level	@RXIN0		-10		dBm
Absolute Gain	RXIN0→RXOUT 1KHz	-1.5	0	1.5	dB
Noise Level	RXIN0→RXOUT (Note②)			-65	dBm
Absolute Gain(2)	RXIN0→BPFOUT 20KHz	27	30	33	dB
Noise Level(2)	RXIN0→BPFOUT (Note③)			-35	dBm
Rectifier Linearity	RECTIN→RECTOUT(Note④)	-0.5		0.5	dB
MSK Input Signal Level	RXIN0→RDATA (VDD=3V, 1.2KHz Input)	-14	-8	-2	dBm

Note② : After 2nd order low pass filter (fc=10KHz), including Deemphasis.
Note③ : After 2nd order low pass filter (fc=30KHz)
Note④ : Rectifier linearity is defined as follows; 20 LOG (2 A/B) [dB]
Where A [mV] is a DC level referenced to analog ground, measured at point "SQLV" when a 100mVrms sinewave is input on RECTIN pin in the application circuit examples at page 21 (refer to "rectifier output smoothing circuit").
B [mV] is a DC level measured at the same point when a 200mVrms sinewave is input on RECTIN pin.

3) Op-Amp

Parameter			min	typ	max	Units
Gain Error	AMP1	TXIN→TXINO 300Hz～3.4KHz Pre-set Gain 10～30dB	-1	0	1	dB
	AMP3	RXIN→RXINO 300Hz～20KHz Pre-set Gain 10～20dB	-1	0	1	dB
	AMP5 AMP6	BUFIN→BUFON 300Hz～3.4KHz BUFOP (Note⑤)	5	6	7	dB

Note⑤ : Measured at differential outputs between BUFON and BUFOP.

4) Filter Characteristics

Parameter		min	typ	max	Units
Transmitter Over-All Response (Fig.1)					
TXINO→MOD	100Hz			-30	
(Compressor by-passed,	300Hz	-12	-10.5	-9	
Preemphasis included	2.5KHz	6.5	8	9.5	dB
Referenced to 0dB at 1KHz)	3KHz	6.5	8	9.5	
	5KHz			-7	
Receiver Over-All Response (Fig.2)					
RXINO→RXOUT	100Hz			-4	
(Deemphasis included	250Hz		12	13.5	
Referenced to 0dB at 1KHz)	300Hz	9	10.5		dB
	3KHz	-10.5	-9	-7.5	
	5KHz			-15	
S Q B P F (Fig.3) RXINO→BPFOUT	3KHz			-60	
	10KHz			-30	dB
(Referenced to 0dB at 20KHz)	100KHz			-45	

5) Crosstalk

Parameter			min	typ	max	Units
Transmit→Receive	@RXAF TXINO=0dBm	1KHz			-60	dBm
Receive→Transmit	@MOD RXINO=0dBm	1KHz			-60	dBm

Compandor Characteristic

CONDITIONS : VDD=3V f=1KHz Ta=25℃ 0dBm=0.775Vrms GCONT="H"

Parameter		MIN	TYP	MAX	UNIT	CONDITIONS
COMPRESSOR						
	Reference Level	-11.0	-10.0	-9.0	dBm	@COMPO TXIN0=-10dBm
	Maximum Input Level			0	dBm	@TXIN0
	Maximum Output Level			-5.0	dBm	@COMPO Distortion better than -35dB
	Output Level (Note①)	-18.0 -22.0	-17.0 -20.0	-16.0 -18.0	dB	@COMPO TXIN0=-44dBm TXIN0=-50dBm
	Idle Noise		-55	-40	dBm	@COMPO (Note②)
	Distortion		-55	-35	dB	@COMPO TXIN0=-10dBm
	Attack Time	2.0	3.0	5.0	mS	12dB Step Input
	Recovery Time	7.0	13.5	20.0	mS	12dB Step Input
EXPANDER						
	Reference Level	-11.0	-10.0	-9.0	dBm	@EXPOUT EXPIN=-10dBm
	Maximum Input Level			-5.0	dBm	@EXPIN
	Maximum Output Level			0	dBm	@EXPOUT Distortion better than -35dB
	Output Level (Note③)	-32.0 -43.0	-30.0 -40.0	-28.0 -37.0	dB	@EXPOUT EXPIN=-25dBm EXPIN=-30dBm
	Idle Noise		-80	-65	dBm	@EXPOUT (Note②)
	Distortion		-58	-35	dB	@EXPOUT EXPIN=-10dBm
	Attack Time	7.0	13.5	20.0	mS	6dB Step Input
	Recovery Time	7.0	13.5	20.0	mS	6dB Step Input

Note① : Referenced to 0dB at PEIN pin as reference level.
Note② : C-Message weighted.
Note③ : Referenced to 0dB at EXPOUT pin as reference level.

☐ Filter Characteristics

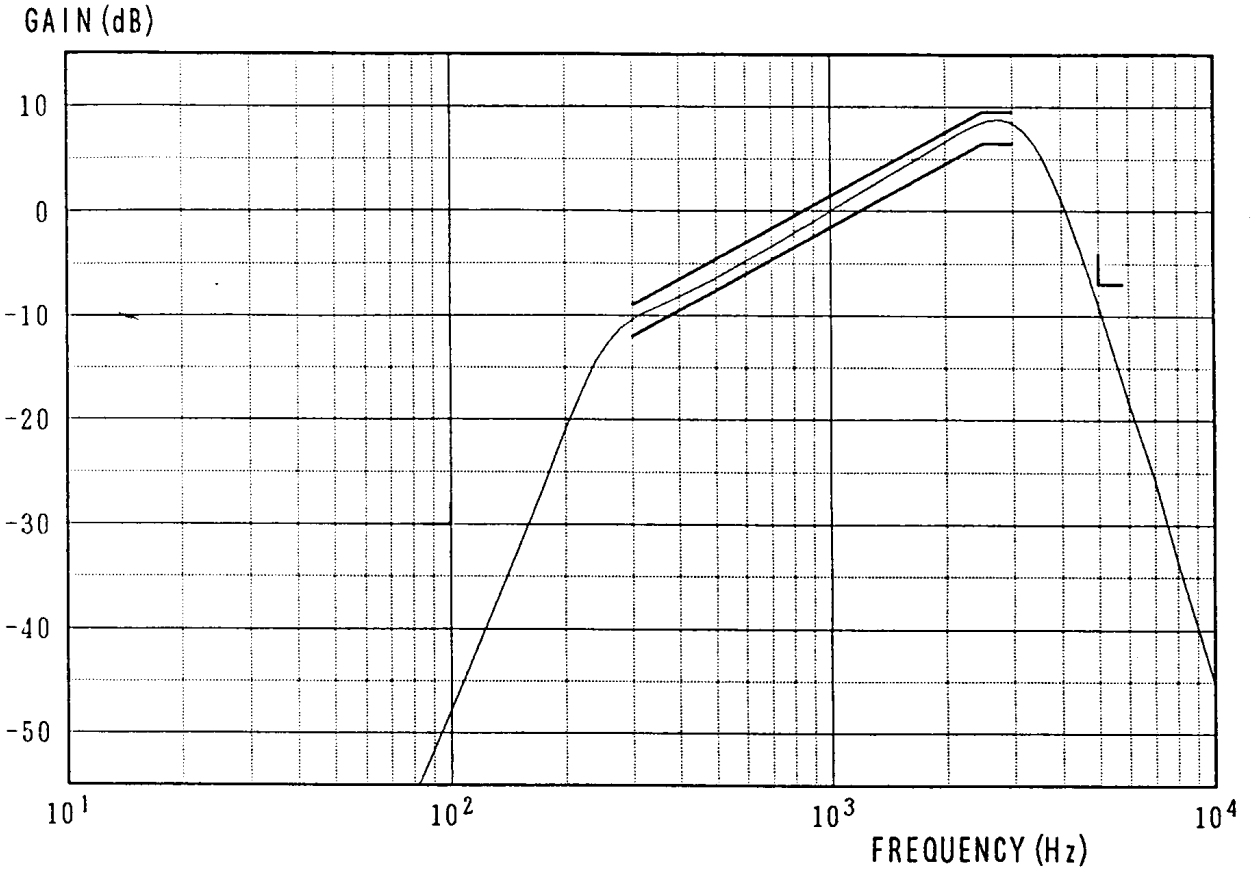


Fig.1 Total Frequency Response of Transmitter Section

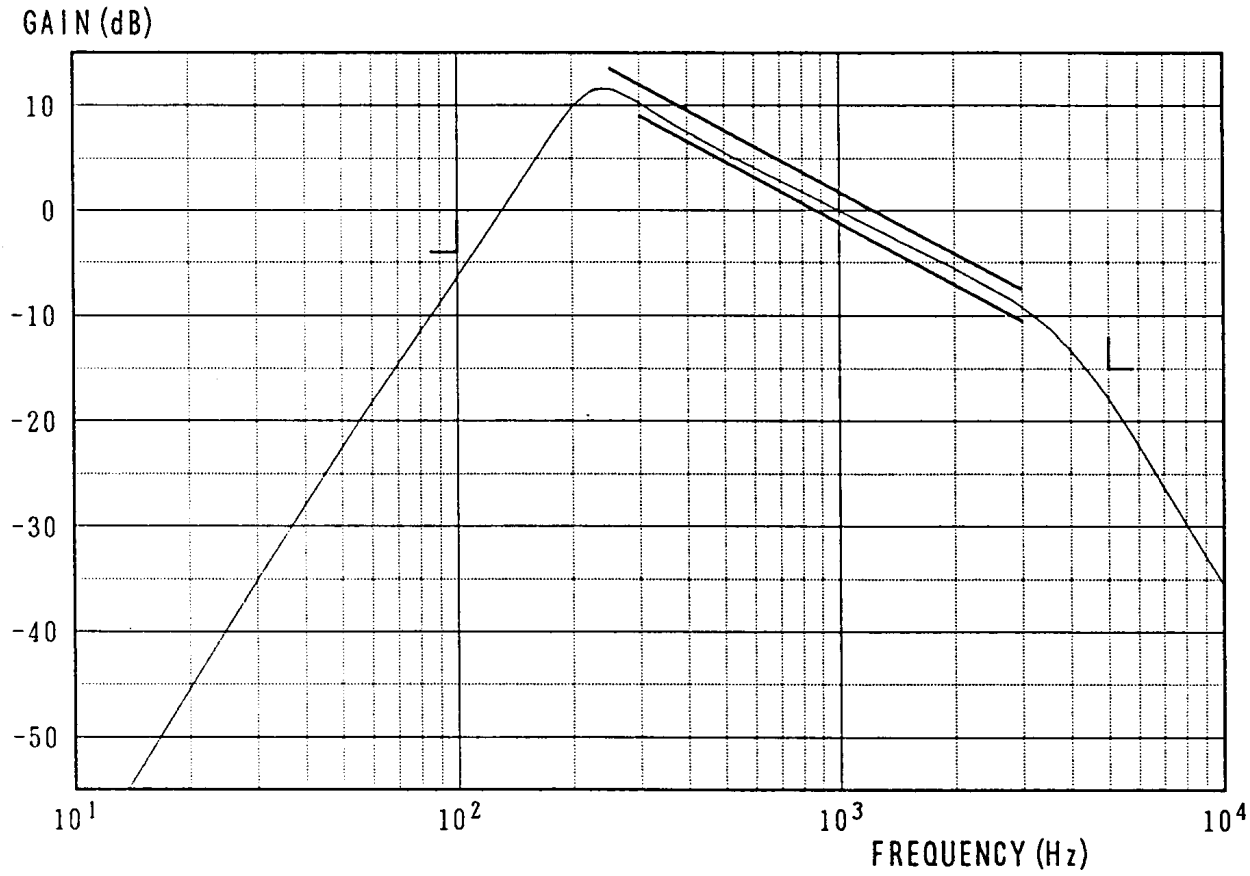


Fig.2 Total Frequency Response of Receiver Section

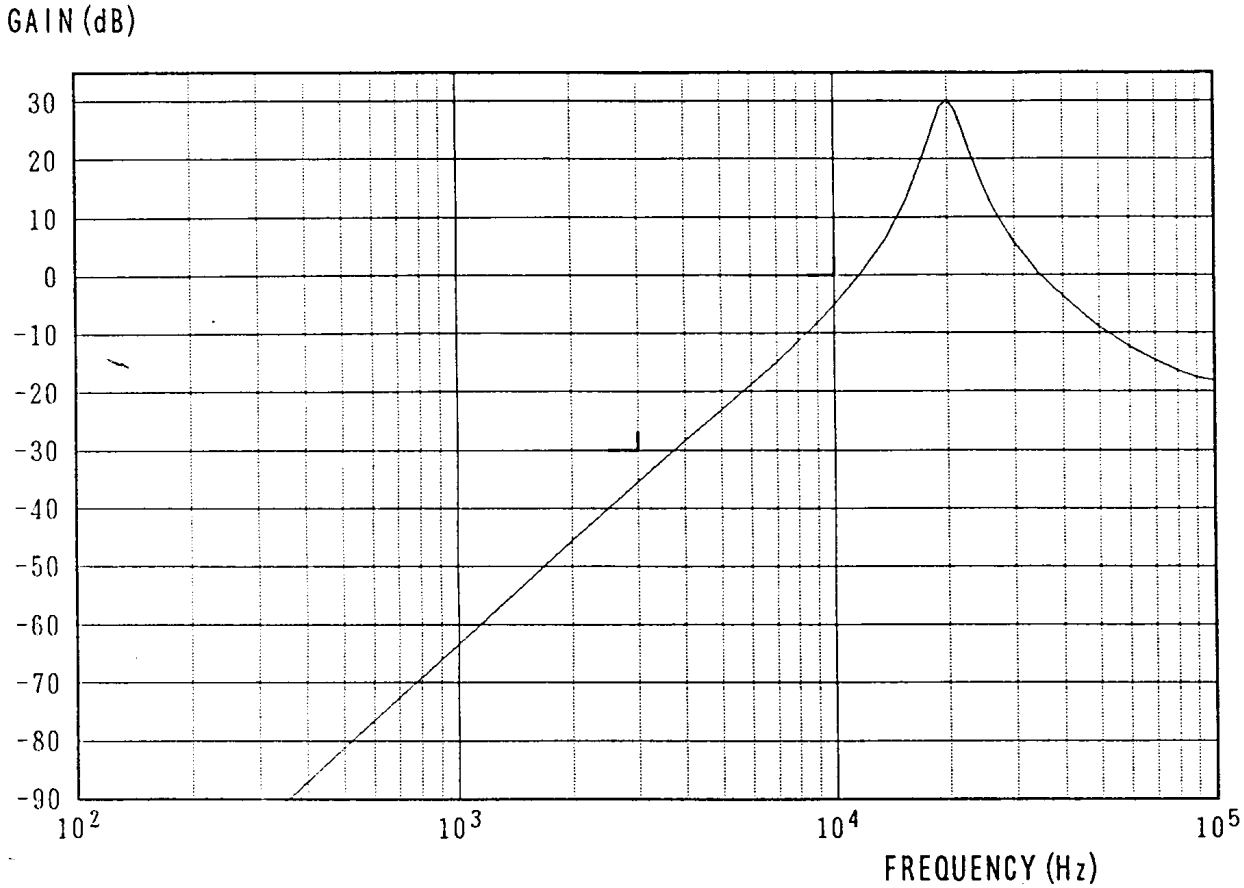


Fig.3 SQBPF Frequency Response

Digital Characteristics

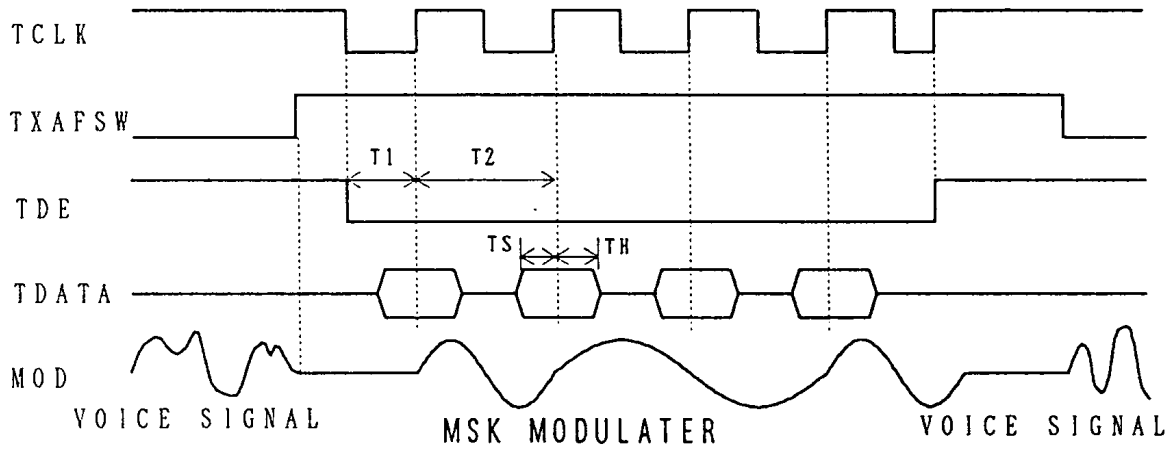
1. DC Characteristics

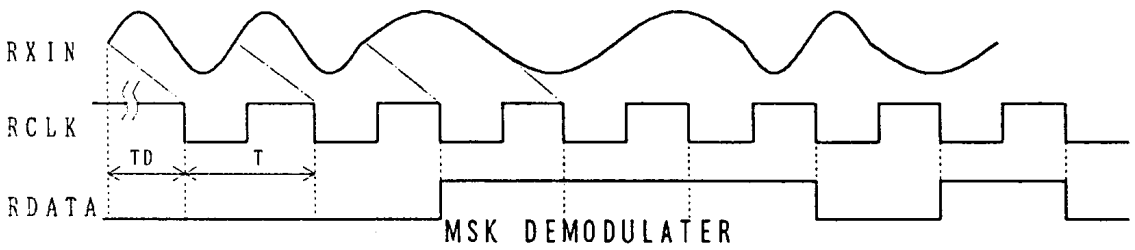
Parameter	Pin	Symbol	min	typ	max	Units
Input "High" Voltage	(1)	V_{IH}	70%VD+			V
Input "Low" Voltage	(1)	V_{IL}			30%VD+	V
Input "High" Current V_{IH}=VD+	(1)	I_{IH}			10	μA
Input "Low" Current V_{IL}=0V	(1)	I_{IL}	-150			μA
Output "Low" Voltage I_{OL}=1.6mA	(2)	V_{OL}			0.3	V
On-Chip Pull-Up Resistor Value	(1)	R_{UP}	50		200	KΩ

(1) TDE, TDATA, BS1, BS2, TXAFSW, RXAFSW, TC, GCONT, PCONT
(2) TCLK, RDATA, RCLK

2. Switching Characteristics

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fclk		3.579545		MHz
Modulator Timing					
TDE Falling to TCLK Rising	T1		208.3		μS
TCLK Period	T2		416.7		μS
TDATA Set Up Time	TS	10			μS
TDATA Hold Time	TH	10			μS
MSK Demodulator Timing					
RCLK Period	T	402.2	416.7		μS
Analog Input to RDATA Edge	TD	400		900	μS



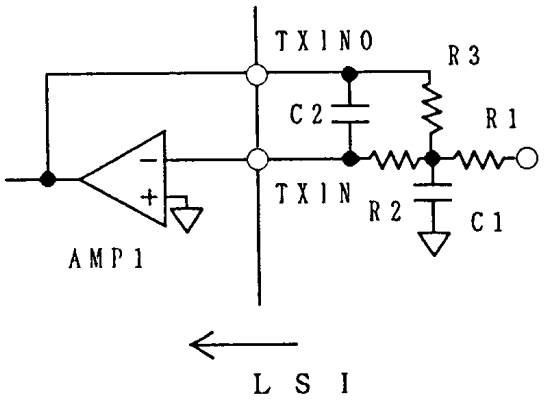


Application Circuit Examples

A. External circuit examples

① AMP1

- This is used as a transmit Mic Amp.
- Set the gain to be within 10～30dB.
- If noise higher than 50KHz on input signal is expected, an anti-aliasing filter must be included.
- A circuit configuration example below shows 2nd order low pass filter with the cut-off frequency at 10KHz.
  The filter also has 30dB gain.



C1 = 2200pF

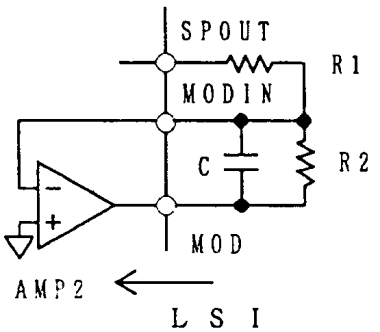
C2 = 33pF

R1 = R2 = 10k Ω

R3 = 330k Ω

② AMP2

- This is used as smoothing filter and gain adjustment of the transmit signal.
- Smoothing filter is used to elminate a 112KHz clock component contained in the splatter filter output.
- The circuit example below shows a 1st order low pass filter with the cut-off frequency set at 13KHz and it has 0dB gain.

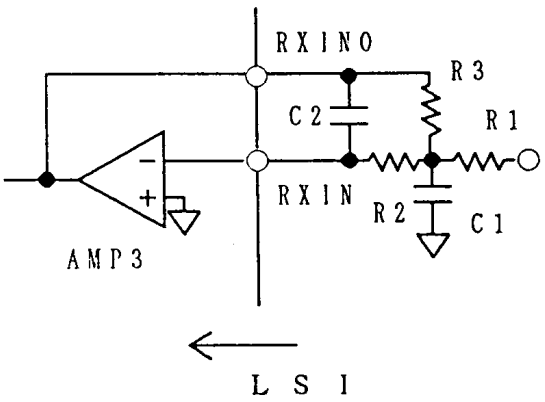


C = 220pF

R1 = R2 = 56k Ω

③ AMP3

- AMP3 is used as gain adjustment of receive signal and an anti-aliasing filter to eliminate higher-than-100KHz noise.
- Set the gain to be around 10～20dB.
- The cut-off frequency of the filter should be selected to such a value that the pass-band noise (20KHz) of the squelch band pass filter (SQBPF) is not rejected.
- Following circuit shows a 2nd order low pass filter with the cut-off frequency set at 40KHz. The filter also has 20dB gain.



C1=560pF

C2=27pF

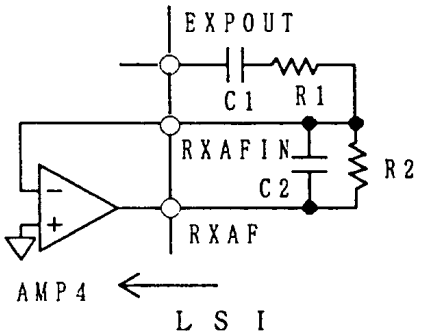
R1=10kΩ

R2=9.1kΩ

R3=100kΩ

④ AMP4

- AMP4 configures a smoothing filter and a gain adjustment circuit for the receive signal.
- The smoothing filter is used to reject 448KHz clock component contained in the expander output (EXPOUT).
- Following circuit example shows a 1st order low pass filter with the cut-off frequency set at 19KHz. The filter has 0dB gain.



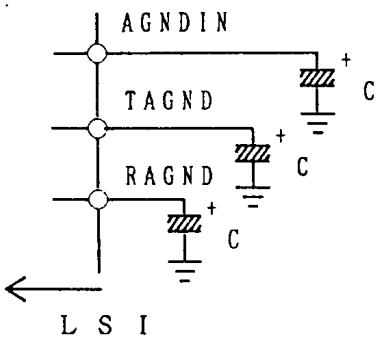
C1=0.022μF

C2=150pF

R1=R2=56kΩ

⑤ AGND stabilization capacitor

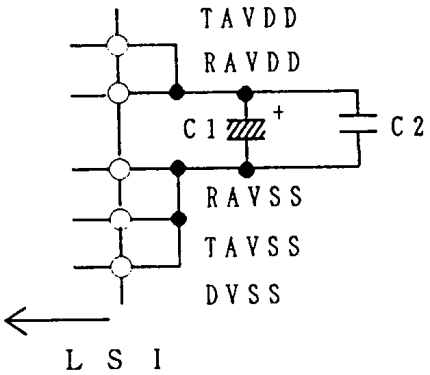
- 0.3 μF or larger capacitors should be connected between TAGND, RAGND pins and AVSS respectively in order to stabilize analog ground.
- In order to minimize effect of ripple on power-supply, an appropriate capacitor is also recommended to place between AGNDIN pin and AVSS.
- Connection Example is shown below.



C = 1 μF

⑥ Power supply stabilization capacitor

- To minimize the effect of power supply noise, a couple of capacitors should be placed between TAVDD, RAVDD pins and DVSS, TAVSS, RAVSS pins.

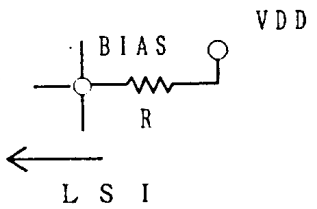


C1 = 22 μF (Electrolytic Cap.)

C2 = 0.1 μF (Ceramic Cap.)

⑦ Bias-current setting resistor

- Bias-current of Op Amp is set by connecting a resistor between Bias Pin and VDD.
  A 150K OHM (220K OHM) resistor is recommended at VDD=3V (VDD=4V) operation.

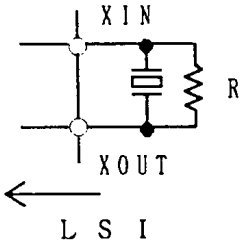


R=150k Ω (VDD=3V)

R=220k Ω (VDD=4V)

⑧ Crystal Oscillator

- Crystal resonator and a resistor should be connected as shown below for on-chip oscillator operation.
- For external clock operation, connenct XIN pin to VSS and an external clock source to XOUT pin. Be careful not to exceed clock amplitude beyond the maximum ratings.



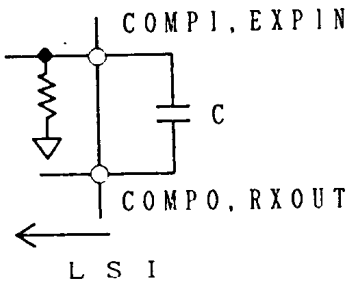
FREQUENCY: 3.58MHz

OR 3.579545MHz

R=1M Ω

⑨ AC Coupling Capacitors

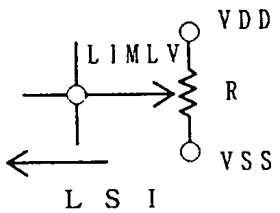
-In order to cut the DC off-set voltages generated in each function block, coupling capacitors are recommended for inter-block connections.
-COMPI pin and PEIN pin should be connected directly when a scrambler chip is not used.



C = 0.022 μF

⑩ Limitter Level Adjusting Resistor

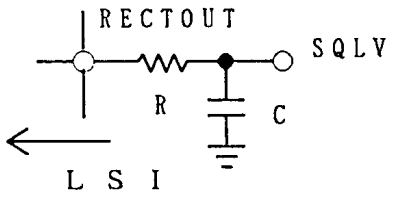
- Limitter level is adjustable by varying the DC level on LIMLV pin. The DC level applied on this pin must be above TAGND.
- The limit level is as follows :
  TAGND ± aV (a= | LIMLV-TAGND |)
- If this pin is left unconnected, a pre-determined level is set.



R = 50k Ω

⑪ Rectifier Output Smoothing Circuit

- A resistor and a capacitor should be connected as shown below in order to smooth out to a DC level a full-wave rectified output signal on RECTOUT pin.
- DC voltage at point "SQLV" below becomes equal to TAGND level when no signal is applied on rectifier input pin (RECTIN).
- SQLV Voltage will be RAGND + 0.2V when a 20KHz with -10dBm signal is input to RECTIN pin.
- SQLV voltage is used to determine the existence / non-existence of signal through succeeding compatator or AD converter.

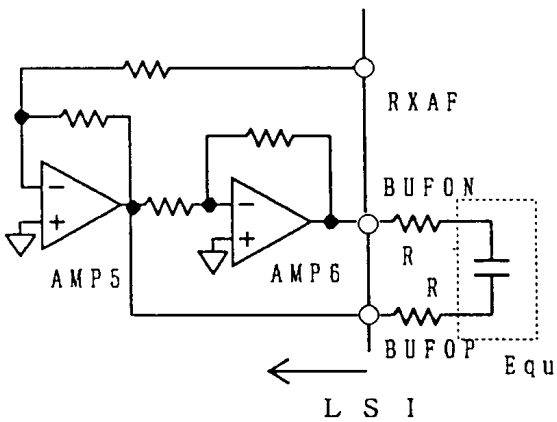


R = 100k Ω

C = 0.022 μF

⑫ Buffer Amp. for Ceramic Receiver

- Amp5 and Amp6 form a differential output buffer to enable direct drive of a ceramic receiver.
  Serial resistors should be inserted to avoid oscillation.



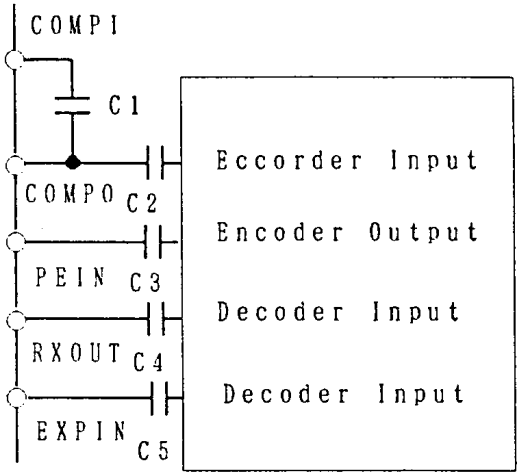
R = 220 Ω

Ceramic Receiver

Equivalent Cap. 22 ~ 140nF

B. Scrambler Chip Connection

When external scrambler is connected, please refer to the schematic below. When the frequency inverter is used, bypassing the preemphasis and deemphasis circuits is recommended in order to keep dynamic range.



C1, C3, C5 = 0.022 μF

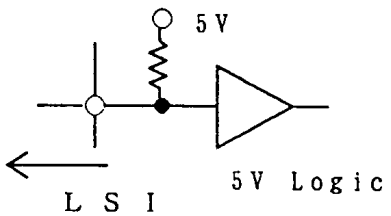
Scrambler I C

C. Logic Interface

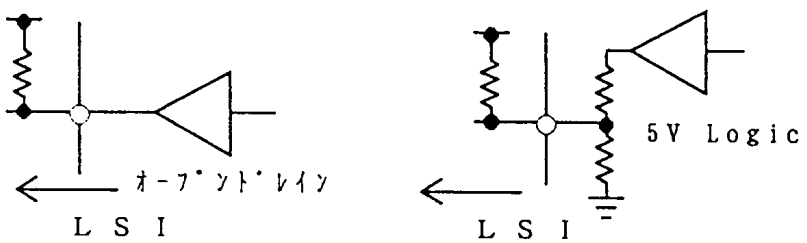
① Digital Pins of AK2351

-Output pins : Open-Drain type
-Input pins : All pins have on-chip pull-up resistors except for TC pin.

② Following logic interface is recommended when AK2351 operates at 3V power supply and it interfaces with +5V logic circuit.



Output Pin

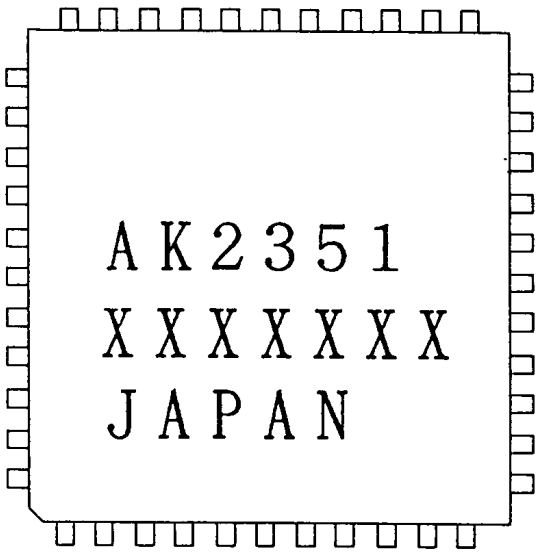


Input Pin

Package

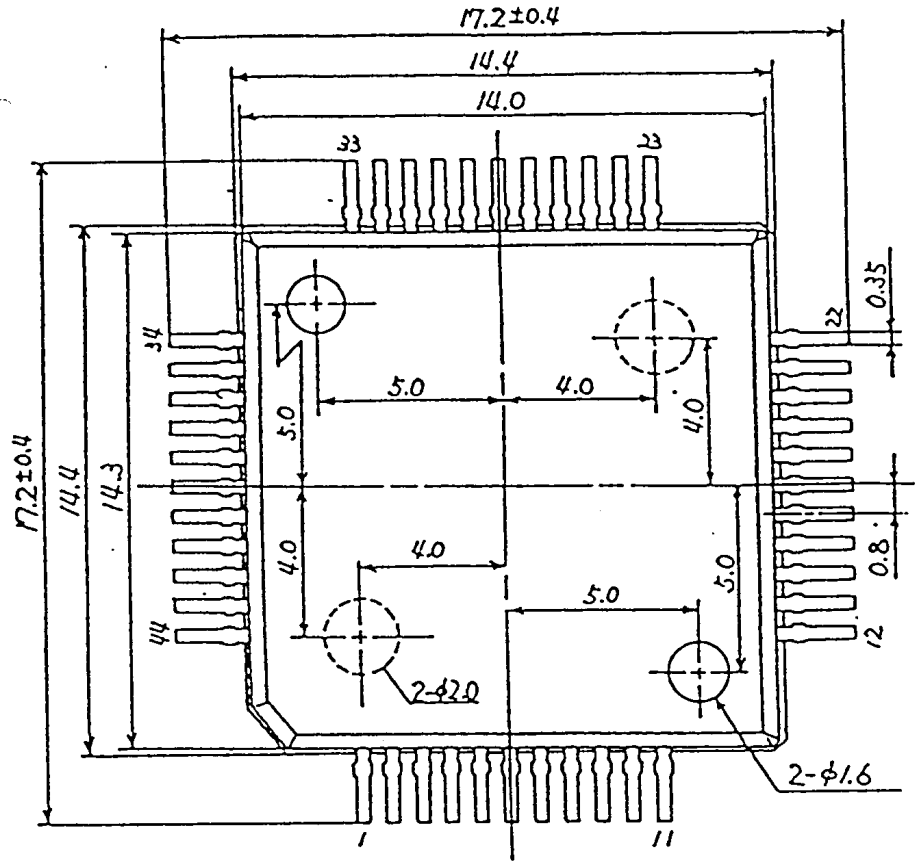
☐ Marking

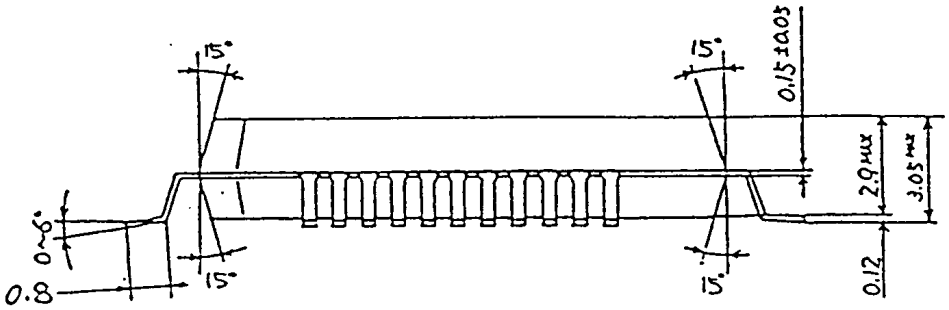
(1) Date Code: xxxxxxx (7 digits)
(2) Marketing Code: AK2351
(3) Country of Origin: JAPAN
(4) Asahi Kasei Logo



☐ Package Outline Dimensions

Unit : mm





* Specifications are subject to change without notice.