AK2504A

DS3/STS-1/E3 Transceiver

GENERAL DESCRIPTION

The AK2504A is a DSP based line transceiver. It provides the analog transmit/receive line interface functions for DS3(44.736MHz) /STS-1(51.84MHz) or E3(34.368MHz) interface.

Transmitter includes on-chip pulse shaper, B3ZS/ HDB3 Encoder. Pulse level adjustment function is very useful to put a pulse into pulse mask for any customer's system.
Receiver includes root-f equalizer, automatic-gain control, clock and data recovery, B3ZS/HDB3 Decoder, Loss-Of-Signal and Loss-Of-Lock alarm function.

Local and Remote Loop-back function is included for system level trouble shooting.

The device operates at a single +3.3 Volt supply and is transparent to the framing format.

FEATURE

- "Robust" DSP based line transceiver
- Provides Complete Analog Line Transmitter and Receiver function for DS3, STS-1 and E3 Applications
- Transmit Pulse Level Adjustment
- Provides Line Equalization, and Clock and Data Recovery Functions
- Compliance with Bellcore GR-499-CORE and GR-253-CORE, ANSI T1.102, T1.404,
- Compliance with ITU-T G.703 and G.823
- Local/Remote Loopback functions
- B3ZS/HDB3 Encoder/Decoder
- Low voltage supply : +3.3V

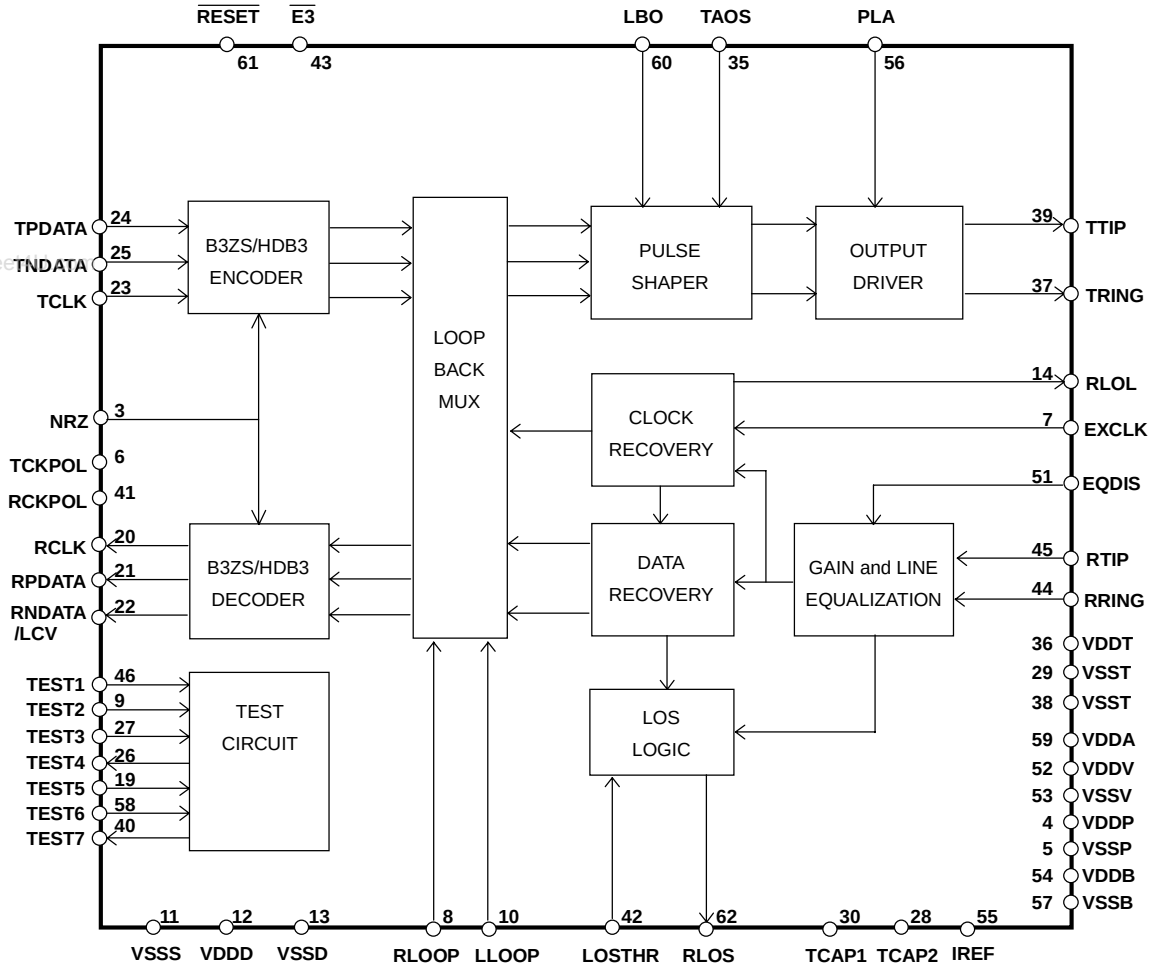
PACKAGE

- 64 pin LQFP

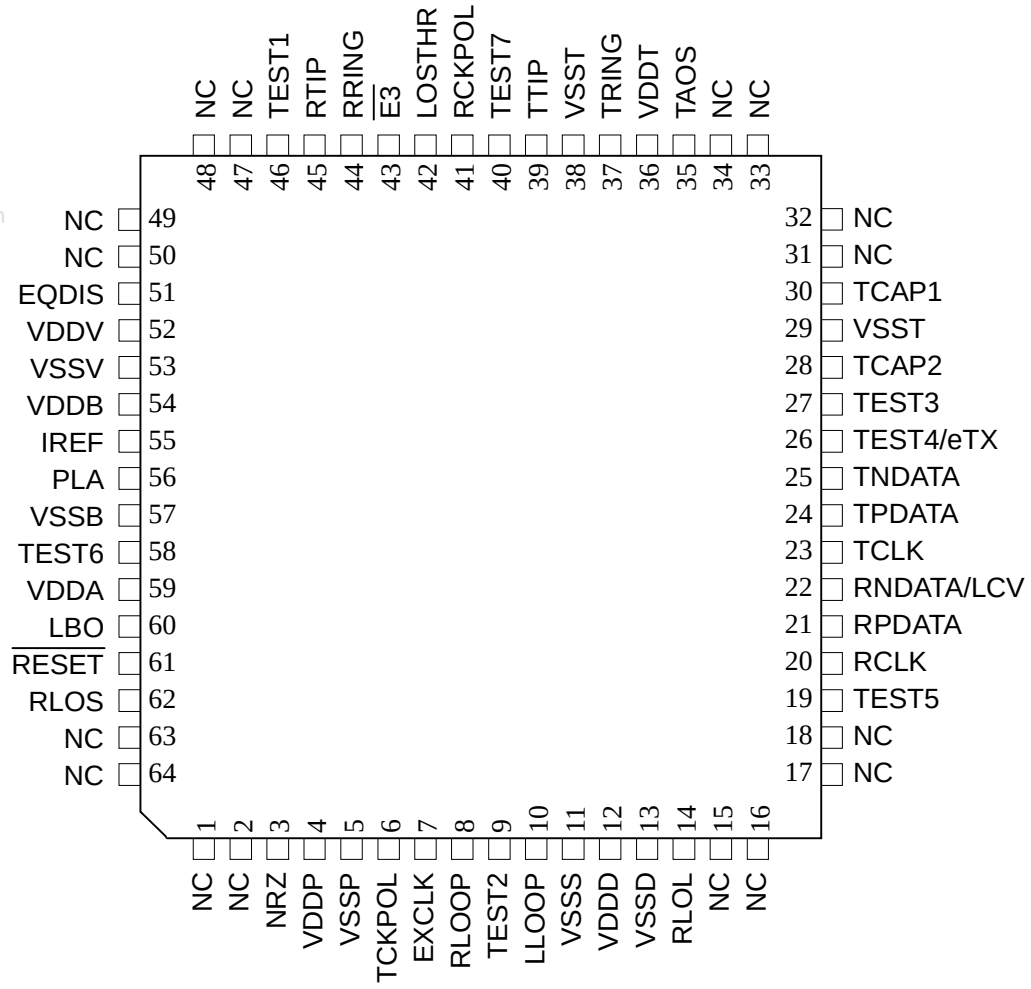
APPLICATIONS

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-3 cross connect.
- Interfacing E3 network transmission equipment.
- Interfacing customer premises equipment to a line.

BLOCK DIAGRAM



PIN LOCATION



NC: No Connection. Leave these pins open.

PIN CONDITION

No.	Pin Name	I/O	Pin Type	Maximum AC load	Minimum DC load	Status on Reset	Remarks
3	NRZ	I	CMOS				
4	VDDP	-					
5	VSSP	-					
6	TCKPOL	I	CMOS				
7	EXCLK	I	CMOS				
8	RLOOP	I	CMOS				
9	TEST2	I	CMOS				
10	LLOOP	I	CMOS				
11	VSSS	-					
12	VDDD	-					
13	VSSD	-					
14	RLOL	O	CMOS	15pF		"H"	
19	TEST5	I	CMOS				
20	RCLK	O	CMOS	15pF		"H"	
21	RPDATA	O	CMOS	15pF		"L"	
22	RNDATA /LCV	O	CMOS	15pF		"L"	
23	TCLK	I	CMOS				
24	TPDATA	I	CMOS				
25	TNDATA	I	CMOS				
26	TEST4	O	CMOS				
27	TEST3	I	CMOS				
28	TCAP2	O	Analog				Note 1
29	VSST	-					
30	TCAP1	O	Analog				Note 1

Note:

*) NC pin number : No. 1, 2, 15, 16, 17, 18, 31, 32 NC: No Connection. Leave these pins open.

1)External capacitor (0.1 uF) is connected to VSS.

No.	Pin Name	I/O	Pin Type	Maximum AC load	Minimum DC load	Status on Reset	Remarks
35	TAOS	I	CMOS				
36	VDDT	-					
37	TRING	O	Analog			Hi-Z	
38	VSST	-					
39	TTIP	O	Analog			Hi-Z	
40	TEST7	O	CMOS				
41	RCKPOL	I	CMOS				
42	LOSTHR	I	Analog				
43	$\overline{E3}$	I	CMOS				
44	RRING	I	Analog				
45	RTIP	I	Analog				
46	TEST1	I	CMOS				
51	EQDIS	I	CMOS				
52	VDDV	-					
53	VSSV	-					
54	VDDB	-					
55	IREF	O	Analog				Note 2
56	PLA	O	Analog				Note 3
57	VSSB	-					
58	TEST6	I	CMOS				
59	VDDA	-					
60	LBO	I	CMOS				
61	$\overline{RESET}$	I	CMOS				Note 4
62	RLOS	O	CMOS	15pF		"H"	

Note

*)NC pin number : No. 33, 34, 47, 48, 49, 50, 63, 64 NC: No Connection. Leave these pins open.

2)External resister 4.7 kΩ±1% should be connected between IREF and VSS.

3)External resister should be connected between PLA and VSS.

Normally 1.33kΩ is connected for DS3/STS-1 or 1.27kΩ for E3.

4)Pulled up to VDD with internal register. (typical 50k Ω)

PIN DESCRIPTION

Receive

No.	Pin Name	I/O	Function
42	LOSTHR	I	**Loss of Signal Threshold Control** (See Table 15) The voltage forced on this pin controls the input loss-of-signal threshold. Two settings are provided by forcing VSS or VDD.
14	RLOL	O	**Receive PLL Loss-of-Lock** Active High alarm. If the recovered clock frequency is larger than approximately 0.5% of EXCLK, RLOL alarm goes High.
45	RTIP	I	**Receive Tip Input** Receive input for differential AMI signal. Requires a 1:1 transformer.
44	RRING		**Receive Ring Input** Receive input for differential AMI signal. Requires a 1:1 transformer.
62	RLOS	O	**Receive Loss-of-Signal.** This pin is set high on loss of the incoming signal at RIN.
7	EXCLK	I	**External Reference Clock.** A valid DS3/STS-1/E3 clock must be provided at this input. The EXCLK frequency determines the operating frequency of the device.
20	RCLK	O	**Recovered Clock.**
22	RNDATA /LCV	O	**Receive Negative Data/Line Code Violation Indicator** This pin's function depends on the input level. NRZ = Low : Receive Negative Data output NRZ = High : Bipolar Violation Output 1 bit period of High level signal is output if a bipolar violation not corresponding to the appropriate coding rule or a code error is detected in the incoming data stream. The violation pulse corresponding to the appropriate coding rule is removed from the incoming data.
21	RPDATA	O	**Receive Positive Data** This pin's function depends on the input level. NRZ = low : Receive Positive Data output NRZ = high : NRZ data output
41	RCKPOL	I	**RCLK Polarity select.** RCKPOL=L : Received data is output on the rising edge of RCLK. RCKPOL=H : Received data is output on the falling edge of RCLK.
51	EQDIS	I	**Equalizer Disable.** When EQDIS=H, Equalizer is disable.
59	VDDA	-	**Power Supply for ADC.** +3.3 volts.
52	VDDV	-	**Power Supply for VGA.** +3.3 volts.
53	VSSV	-	**Ground for VGA.** 0 volts.
4	VDDP	-	**Power Supply for PLL.** +3.3 volts
5	VSSP	-	**Ground for PLL.** 0 volts.
54	VDDB	-	**Power Supply for Bandgap Reference.** +3.3 volts.
57	VSSB	-	**Ground for Bandgap Reference.** 0 volts.

Transmit

No.	Pin Name	I/O	Function
24	TPDATA	I	**Transmit Positive Data/NRZ data** This pin's function depends on the input level. NRZ = Low : Positive AMI data output NRZ = High : NRZ data
25	TNDATA	I	**Transmit Negative Data** This pin's function depends on the input level. NRZ = Low : Negative AMI data output NRZ = High : Should be tied to VSS
23	TCLK	I	**Transmit Clock** TPDATA and TNDATA are sampled on the rising or falling edge of TCLK. Sampling edge must be assigned by TCKPOL pin.
6	TCKPOL	I	**TCLK Polarity select.** TCKPOL=Low : Transmit data is sampled on the rising edge of TCLK. TCKPOL=High : Transmit data is sampled on the falling edge of TCLK.
39	TTIP	O	**Transmit Tip / Ring Output** AMI signal output. Requires a 1:1CT transformer. Hi-Z when $\overline{\text{RESET}}$ = Low.
37	TRING	O	
56	PLA	I	**Pulse Level Adjustment** Transmit pulse level can be adjusted by the external resister. Normally 1.33kΩ is connected for DS3/STS-1 or 1.27kΩ for E3. If the signal power level is larger than a requirement, you can tweak it by increasing the value of this resister.
3	NRZ	I	**NRZ mode Enable** Active High input enables NRZ data interface with TPDATA and RPDATA. NRZ | TPDATA TNDATA | RPDATA RNDATA 0 | Positive Negative | Positive Negative 1 | NRZ (VSS) | NRZ LCV In NRZ mode, TNDATA should be tied to VSS and RNDATA indicates LCV.
60	LBO	I	**Line Built Out** If LBO is set to High, Line Built Out function is enable. LBO input: Low — Cable length: 225 – 450ft LBO input: High — Cable length: 0 – 225ft This pin is active only with $\overline{\text{E3}}$ pin set to High(DS3/STS-1 mode).
30	TCAP1	O	**Reference Voltage Output for the TX driver.** An external capacitor (0.1µF±20%) should be connected to VSSA.
28	TCAP2	O	**Reference Voltage Output for the TX driver.** An external capacitor (0.1µF±20%) should be connected to VSSA.
35	TAOS	I	**Transmit All Ones Select** Active High input. A continuous AMI all 1's pattern to be transmitted from TTIP and TRING. Transmit rate is defined by TCLK.
36	VDDT	-	**Power Supply for Transmitter.** +3.3 volts.
29, 38	VSST	-	**Ground for Transmitter.** 0 volts

Others

No.	Pin Name	I/O	Function
43	$\overline{E3}$	-	**DS3/STS-1 or E3 select pin** High : DS3/STS-1 Low : E3
55	IREF	O	**Current Reference Output** External resistance (4.7 kΩ±1%) should be connected to VSSA.
8	RLOOP	I	**Remote Loop Back** Active High input. RPDATA and RNDATA are transmitted from TTIP and TRING using RCLK. Input High on both RLOOP and LLOOP are inhibited.
10	LLOOP	I	**Local Loop Back** Active High input. TPDATA,TNDATA and TCLK are looped back to RPDATA, RNDATA and RCLK. Input High on both RLOOP and LLOOP are inhibited.
61	$\overline{RESET}$	I	**Active low RESET.** Pulled up to VDD with internal resister.
46	TEST1	I	**Test Mode.** Should be connected to VSS. TEST1=High : The part goes into Test mode. TEST1=Low : The part goes into the Normal operation mode.
9	TEST2	I	Should be connected to VSS.
27	TEST3	I	Should be connected to VSS.
26	TEST4	O	Output “Low” when TEST1=Low (Normal operation mode)
19	TEST5	I	Should be connected to VSS.
58	TEST6	I	Should be connected to VSS.
40	TEST7	O	Should be open.
12	VDDD	-	**Power Supply for Digital.** +3.3 volts.
13	VSSD	-	**Ground for Digital.** 0 volts
11	VSSS	-	**Ground for Substrate.** 0 volts

FUNCTIONAL DESCRIPTION

The AK2504A provides the basic transmit and receive functions of a high-speed line card.

Signal Requirements

DS3/STS1

Pulse characteristics are specified at the DSX-3.

Table 1. DS3 Interface Specification

Parameter	Specification
Line Rate	44.736Mbps±20ppm
Line Code	B3ZS
Test Load	75Ω±5%
Standards	GR-499-CORE , ANSI T1.102 , T1.404

Table 2. STS-1 Interface Specification

Parameter	Specification
Line Rate	51.840Mbps±20ppm
Line Code	B3ZS
Test Load	75Ω±5%
Standards	GR-253-CORE , ANSI T1.102

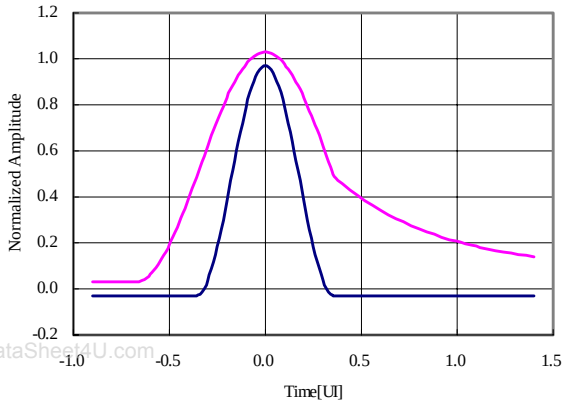


Fig. 1 DSX-3 Pulse Mask

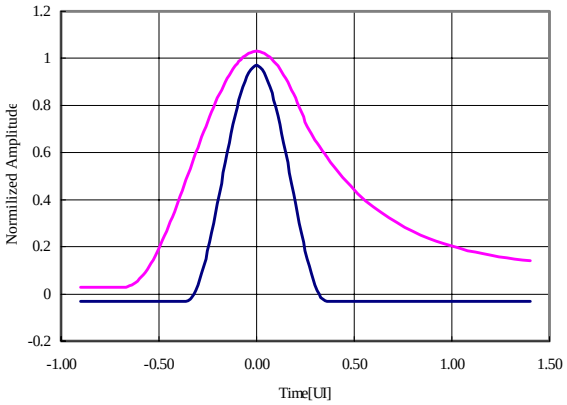


Fig. 2 STS-1 Pulse Mask

Table 3. DS3 Pulse Mask and Equations (ANSI T1.102, T1.404, GR-499-CORE)

Lower Curve		Upper Curve	
Time	Equation	Time	Equation
$-0.85 \le T \le -0.36$	-0.03	$-0.85 \le T \le -0.68$	0.03
$-0.36 \le T \le 0.36$	$0.5\{1+\sin[(\pi/2)(1+T/0.18)]\}-0.03$	$-0.68 \le T \le 0.36$	$0.5\{1+\sin[(\pi/2)(1+T/0.34)]\}+0.03$
$0.36 \le T \le 1.4$	-0.03	$0.36 \le T \le 1.4$	$0.08+0.407e^{-1.84(T-0.36)}$

Table 4 STS-1 Pulse Mask and Equations (GR-253-CORE, T1.102)

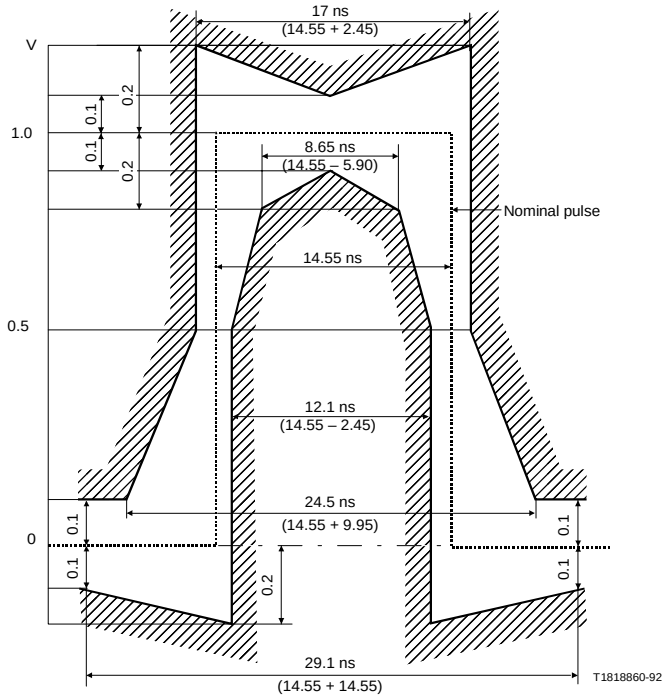
Lower Curve		Upper Curve	
Time	Equation	Time	Equation
$-0.85 \le T \le -0.36$	-0.03	$-0.85 \le T \le -0.68$	0.03
$-0.36 \le T \le 0.36$	$0.5\{1+\sin[(\pi/2)(1+T/0.18)]\}-0.03$	$-0.68 \le T \le 0.26$	$0.5\{1+\sin[(\pi/2)(1+T/0.34)]\}+0.03$
$0.36 \le T \le 1.4$	-0.03	$0.26 \le T \le 1.4$	$0.1+0.61e^{-2.4(T-0.26)}$

E3

Pulse characteristics are specified at the output ports

Table 5. E3 Pulse Specification (G.703)

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Fig.3), irrespective of the sign
Pair(s) in each direction	One coaxial pair
Test load impedance	75 Ωs resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05



Pulse mask at the 34 368-kbit/s interface

Fig. 3 E3 Pulse Mask

Logic Data Interface

AK2504A can handle Positive/Negative data and NRZ data.

Positive/Negative data Interface

If NRZ pin = Low, the transmitter accepts Positive/Negative transmit data on TPDATA/TNDATA and the receiver outputs Positive/Negative received data on RPDATA/RNDATA. In this mode, B3ZS/HDB3 Encoder/Decoder is disable. Transmit and Received data is output transparently.

NRZ data Interface

If NRZ pin = High, the transmitter accepts NRZ transmit data on TPDATA (TNDATA should be tied to VSS). The receiver outputs NRZ received data on RPDATA. In this mode, B3ZS/HDB3 Encoder/Decoder is enable. LCV alarm will be indicated on RNDATA whenever a bipolar violation is detected in the incoming data stream.

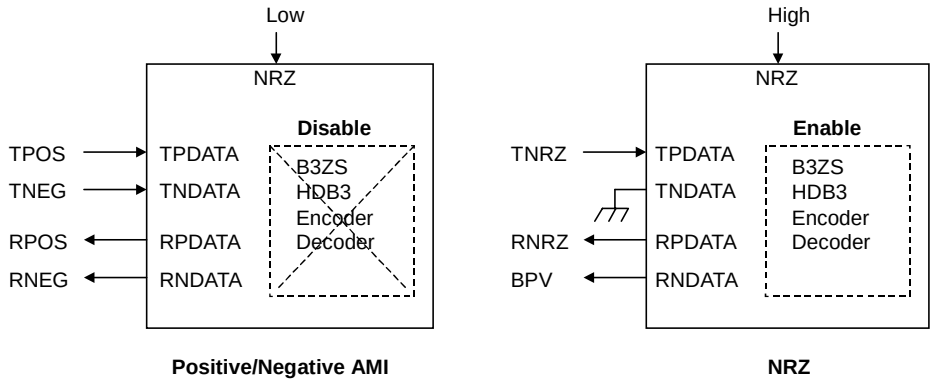


Fig. 4 Logic Data Interface

Line Code Violation

If a bipolar violation not corresponding to the appropriate coding rule or a code error is detected in the incoming data stream, LCV is set high for one bit period. The violation pulse corresponding to the appropriate coding rule is removed from the incoming data.

Bipolar Violation

B3ZS, HDB3 :	B, V	(+1,+1) or (-1,–1)	→	RPDATA	---	1, 1
				LCV	---	0, 1
HDB3:	B, 0, V	(+1, 0,+1) or (-1, 0,–1)	→	RPDATA	---	1, 0, 1
				LCV	---	0, 0, 1

Coding Violation (With an even number of Bs since the last V)

B3ZS :	0, V	(0,+1) or (0,–1)	→	RPDATA	---	0, 1
				LCV	---	0, 1
HDB3:	0, 0, V	(0, 0,+1) or (0, 0,–1)	→	RPDATA	---	0, 0, 1
				LCV	---	0, 0, 1

Excessive Zeros

B3ZS :	0, 0, 0	→	RPDATA	---	0, 0, 0
			LCV	---	0, 0, 1
HDB3:	0, 0, 0, 0	→	RPDATA	---	0, 0, 0, 0
			LCV	---	0, 0, 0, 1

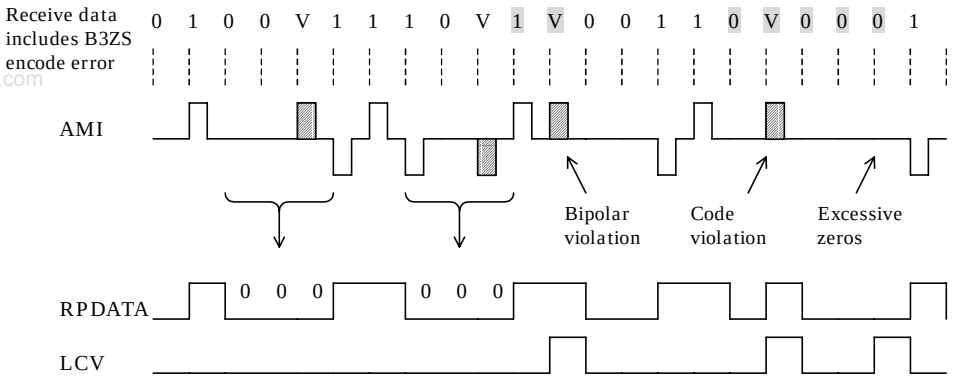


Fig. 5 RPDATA and LCV outputs in NRZ mode (B3ZS)

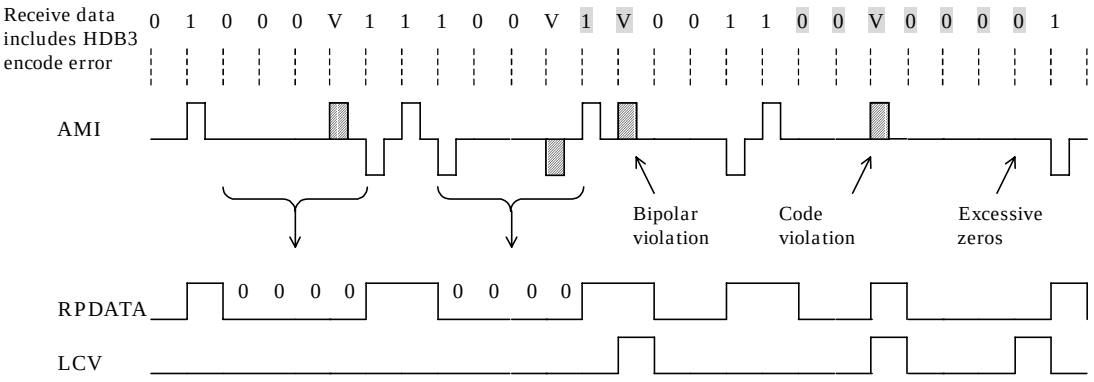


Fig. 6 RPDATA and LCV outputs in NRZ mode (HDB3)

Pulse Shaper

Pulse Shaper generates a waveform meeting the pulse mask such as described in Table 3,4,5.
The input data of Pulse Shaper is the sampled data of TPDATA and/or TNDATA pins on the rising or falling edge of TCLK. Polarity of TCLK is selected by TCKPOL pin.

Line Built Out

When LBO = High, the transmit pulse is output through LBO circuit which makes transmit pulse filtered with the frequency response equivalent to the 225ft cable.

Table 6 Transmit Pulse Amplitude (DS3/STS-1)

LBO	Cable Length	DS3, STS-1
Low	225 – 450 ft	1150mVpk(typ)
High	0 – 225ft	800mVpk(typ)

Note; LBO pin is active only with $\overline{E3}$ pin set to High(DS3/STS-1 mode).

Transmit All Ones Select

If TAOS pin is high, continuos AMI 1s are transmitted from TTIP/TRING. While this All 1s pattern is transmitted, the input data on TPDATA/TNDATA are ignored. In Local Loopback mode (LLOOP pin is high), TAOS request is accepted and the input data on TPDATA/TNDATA are loopback to RPDATA/RNDATA. In Remote Loopback mode (RLOOP pin is high), TAOS request is accepted and the recoverd data is output to RPDATA/RNDATA.

Line Short Protect

If Line is short, there is no large current on the transmit output driver because that the driver is a current source drive type.

Equalization

DS3/STS1

The incoming data may have the loss of cable and/or flat. Cable type and length from the cross-connect are specified as shown in Table 8. Equalizer compensates appropriately for a nominal DSX-3/STS-1 pulse as attenuated by 450 feet of 728A cable.

Table 8 DS3/STS-1 Cable Specification

Parameter	Specification	Remarks
Cable Type	Type 728A coaxial cable (or equivalent)	
Cable Length	0 – 450 feet (from DSX-3 point)	Fig.7–(1)(2)

E3

The incoming data may have the cable loss as shown in Table 9. Equalizer compensates appropriately for a nominal E3 pulse as attenuated by the cable.

Table 9 E3 Cable Specification

Parameter	Specification	Remarks
Cable Loss	0 – 12dB	Fig.7–(1)(2)

Equalizer Bypass

If the incoming signal is attenuated by flat loss only (zero cable loss), the internal equalizer should be bypassed with EQDIS=1. The level of the incoming signal should satisfy the RIN input range (50mVpk - 1000mVpk for DS3/STS-1, 90mVpk - 1200mVpk for E3).

Table 10 Equalizer Bypass Control

EQDIS	Equalizer
0	Enable
1	Bypass

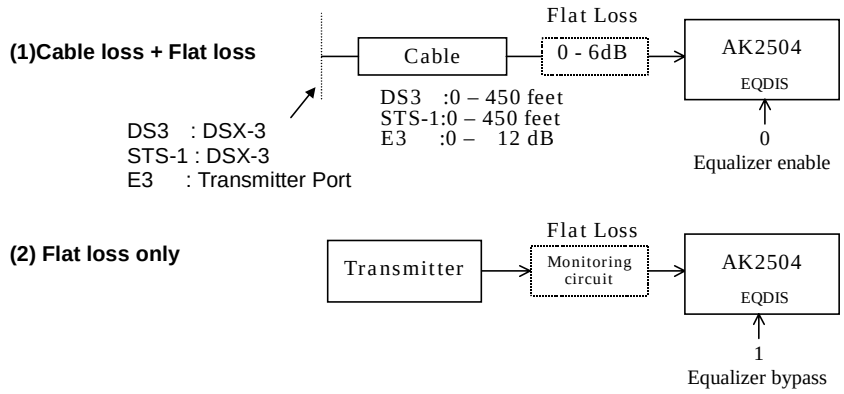


Fig. 7 AK2504A Application

Clock Acquisition

If a valid input signal is assumed to be already present at the analog input, the maximum time between the application of device power and error-free operation is typically 20 ms.

Table 11 PLL Lock Acquisition Time

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND** = 0V)

	Conditions	min	typ	Max	Units
Power up	Power : Off -> On Input data : Valid		20		ms
Input data restore	Power : On Input data : Loss -> Valid		1.0	5.0	ms

**) GND=VSSP= VSSV= VSSB=VSST=VSSS=VSSD=0V

Output Jitter

Typical output jitter characteristics is shown in the table of ANALOG SPECIFICATIONS .

Jitter Transfer

Jitter transfer characteristics is shown in the table of ANALOG SPECIFICATIONS.

Jitter Tolerance

Typical jitter tolerance characteristics is shown in the table of ANALOG SPECIFICATIONS.

DS3/STS-1

Compliance with GR-499-CORE, GR-253-CORE, G.752, G.824

E3

Compliance with ITU-T G.823.

Loopback

AK2504A has two loopback modes, which are Remote Loopback mode and Local Loopback mode. Each function of those is shown in Table 12 and Fig. 8.

Table 12 Loopback Function

Mode	RLOOP	LLOOP	Function	
Remote	1	0	RPDATA → TTIP RNDATA → TRING	Transmit rate is determined by RCLK. TPDATA/TNDATA are ignored.
Local	0	1	TPDATA → RPDATA TNDATA → RNDATA TCLK → RCLK	Transmit rate is determined by TCLK. TPDATA/TNDATA are ignored.
	1	1	Not permitted that both RLOOP and LLOOP are high.	

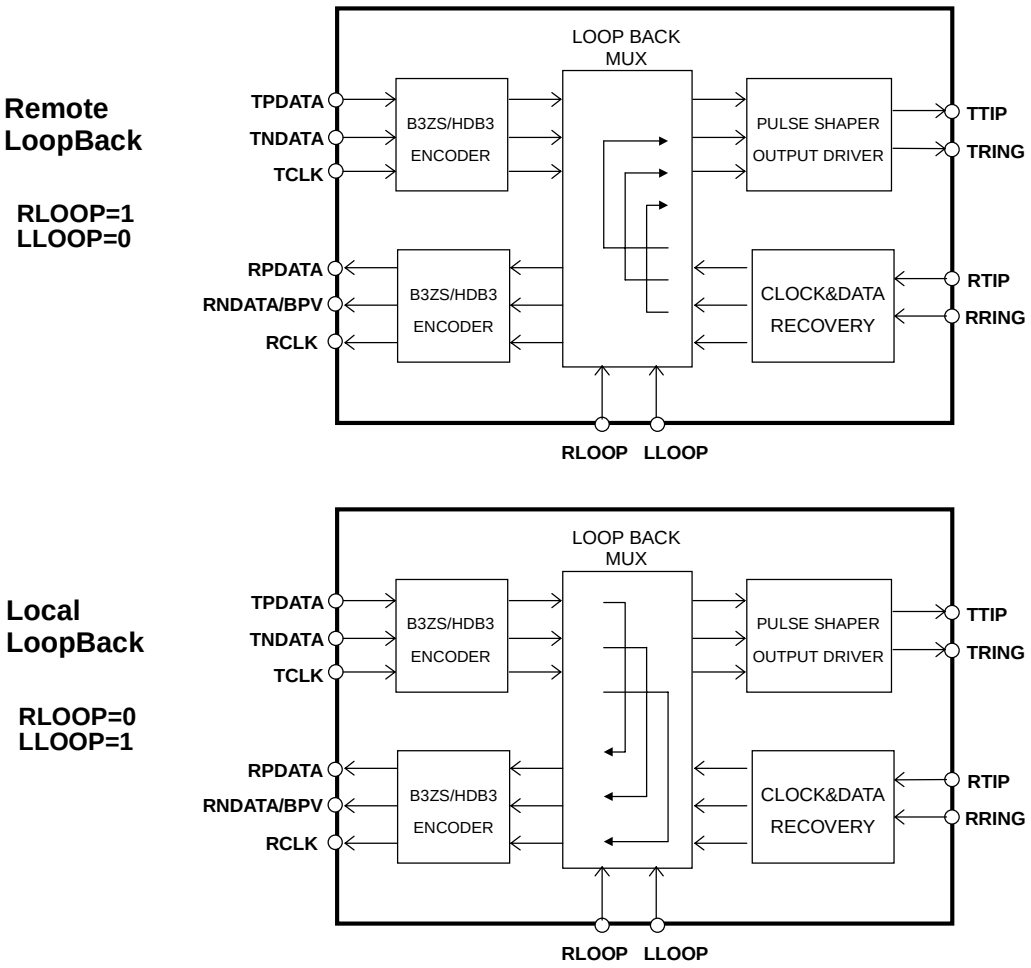


Fig. 8 Loopback Path

TX and RX Output status related to NRZ, TAOS, RLOOP, LLOOP input

Table 13 TX and RX Output status

E3B	NRZ	TAOS	RLOOP	LLOOP	TTIP/TRING	RPDATA/RNDATA
X	0	1	1	0	AMI ones	Recovered data
0	1	1	1	0	AMI ones	Recovered data(UNHDB3)
1	1	1	1	0	AMI ones	Recovered data(UNB3ZS)
X	0	0	1	0	Recovered data	Recovered data
0	1	0	1	0	Recovered data	Recovered data(UNHDB3)
1	1	0	1	0	Recovered data	Recovered data(UNB3ZS)
X	0	1	0	1	AMI ones	TPDATA/TNDATA
0	1	1	0	1	AMI ones	TPDATA/TNDATA(UNHDB3)
1	1	1	0	1	AMI ones	TPDATA/TNDATA(UNB3ZS)
X	0	0	0	1	TPDATA/TNDATA	TPDATA/TNDATA
0	1	0	0	1	TPDATA/TNDATA(HDB3)	TPDATA/TNDATA(UNHDB3)
1	1	0	0	1	TPDATA/TNDATA(B3ZS)	TPDATA/TNDATA(UNB3ZS)
X	X	1	0	0	AMI ones	Recovered data
X	0	0	0	0	TPDATA/TNDATA	Recovered data
0	1	0	0	0	TPDATA/TNDATA(HDB3)	Recovered data(UNHDB3)
1	1	0	0	0	TPDATA/TNDATA(B3ZS)	Recovered data(UNB3ZS)

Loss-of-Lock Detection

If the recovered clock frequency is larger than approximately 0.5% of EXCLK, RLOL alarm goes High.

External Reference Clock

An external reference clock EXCLK is used to set the frequency of the PLL. The frequency of EXCLK should be within the ideal clock±100ppm.

Reset

AK2504A goes into RESET status if $\overline{\text{RESET}}$ input is low.
Output pins status is as follows during the low input on $\overline{\text{RESET}}$.

RLOS : High
RLOL : High
RPDATA : Low
RNDATA : Low
RCLK : High

Test Mode

The AK2504A goes into Test Mode when TEST1 pin is High.

Loss of Signal

DS3/STS-1

AK2504A detects the loss of signal by analog and digital methods. Loss of Signal function in DS3/STS-1 mode is as follows.

Analog Loss of Signal(ALOS)

Analog loss detector operates as follows.

- Analog loss detector monitors the peak level of the incoming signal.
- If the peak level falls below Alarm set threshold as shown in Table 14, output pins status is shown in the diagram below.

Table 14 Analog Loss-of-Signal thresholds (DS3/STS-1/E3)

LOSTHR Voltage	Clear Alarm Level		Set Alarm Level		Units
	Min. Upper Threshold	Max. Upper Threshold	Min. Lower Threshold	Max. Lower Threshold	
VSS	80	160	70	150	mVpk
VDD	50	110	40	100	mVpk

Notes:

- Set Alarm Level is 0.5dB lower than Clear Alarm Level.

Digital Loss of Signal(DLOS)

Digital loss detector operates as follows.

- A digital loss detector monitors consecutive 0s and 1s density in recovered data.
- RLOS is set high if 175±5 consecutive 0s is detected.
- RPDATA,RNDATA are set low if ALOS is detected.
- RLOS is set low if 33% 1s density (58 1s in 175 consecutive bits) and no consecutive 100 0s are detected.

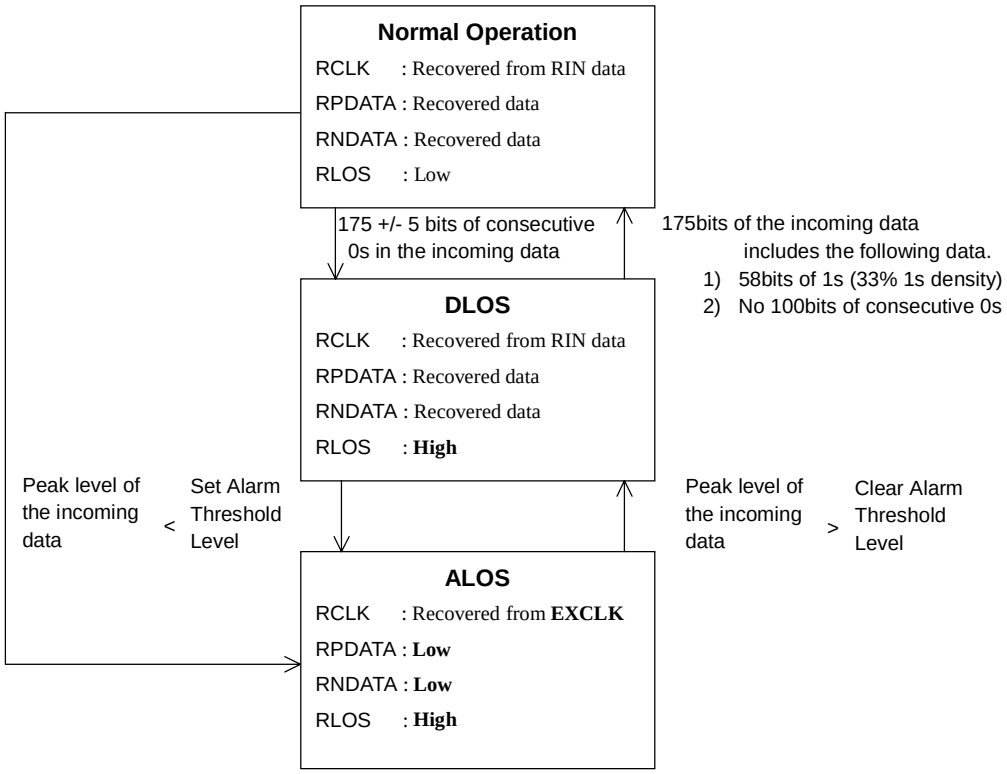


Fig. 9 Loss of Signal state diagram (DS3/STS-1)

Loss of Signal

E3

AK2504A detects the loss of signal by analog and digital methods. Loss of Signal function in E3 mode is as follows.

- Analog loss detector monitors the peak level of the incoming signal.
- If the peak level falls below Set Alarm Threshold Level as shown in Table 15, DLOS circuit starts counting the number of the incoming data bits as described in the following section “DLOS”.

- If DLOS circuit detects consecutive 128±5 bits of the incoming data lower than Set Alarm Threshold Level, AK2504A alarms Loss of Signal by setting RLOS high. Other output pins status is as shown in the diagram below.
- RLOS is set low if 32±5 bits of the incoming data higher than Clear Alarm Threshold Level are detected.

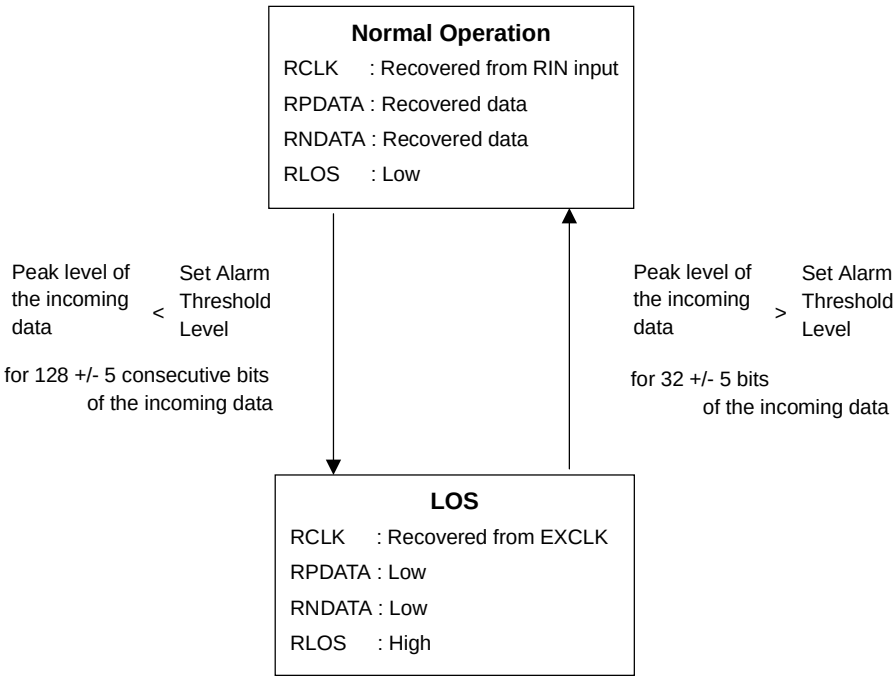


Fig. 10 Loss of Signal state diagram (E3)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND) (Note 1)	V+	-0.3	4.6	V
Input Voltage, Any Pin	Vin	GND-0.3	(V+)+0.3	V
Input Current, Any Pin (Note 2)	Iin	-	10	MA
Ambient Operating Temperature	TA	-40	85	°C
Storage Temperature	Tstg	-65	150	°C
Power Dissipation	PD	-	1	W

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note; 1.GND=VSSV=VSSP=VSSB=VSST=VSSD=VSSS=0V
2.Transient currents of up to 100 mA will not cause SCR latch up.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min	Typ	Max	Units
DC Supply (referenced to GND)		V+		3.0	3.3	3.6	V
Ambient Operating Temperature		TA		-40	25	85	°C
Supply Current:	*DS3*	IS	PN20	-	200	220	mA
	STS-1		PN20	-	210	230	mA
	E3		PN20	-	160	180	mA
EXCLK Frequency	*DS3*			44.736 - 100ppm	44.736	44.736 + 100ppm	MHz
	STS-1			51.84 - 100ppm	51.84	51.84 + 100ppm	MHz
	E3			34.368 - 100ppm	34.368	34.368 + 100ppm	MHz

RECEIVER ANALOG SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V)

Parameter	Condition	Min	Typ	Max	Units
Jitter Transfer with repetitive 100 pattern (Note 3)	3dB Bandwidth	-	205	-	kHz
	Peaking	-	0.05	0.1	dB
Jitter Tolerance (Note 4)	5kHz		20		Uipp
	10kHz		15		Uipp
	60kHz		2		Uipp
	300kHz		0.6		Uipp
	1MHz		0.4		Uipp
Signal Noise Immunity (Note 5)		-	8	12	dB
Output Jitter (Note 3)	All one's pattern	-	1.4	-	nsp-p
	Repetitive 1000 pattern	-	1.8	-	nsp-p
Output Clock Duty Cycle (Note 3)		45	-	55	%
Receiver Input Range	*DS3/STS1*	50	-	1000	mVpk
	E3	90	-	1200	mVpk
DLOS detection	*DS3/STS1*	170	175	180	bits
Loss Detection	*E3*	123	128	133	bits
RIN to RPDATA Delay Time				8	bits

Note; 3. Measured with repetitive input at nominal DSX-3 level(DS3/STS-1), nominal G.703 level(E3) with (V+)=3.3V, TA=25°C

4. Typical performance is shown in Fig 11.

5. Measured with sinusoidal noise, peak amplitude of noise is 11dB down from peak amplitude of signal. The noise frequency is 22MHz(DS3), 25MHz(STS-1), 17MHz(E3).

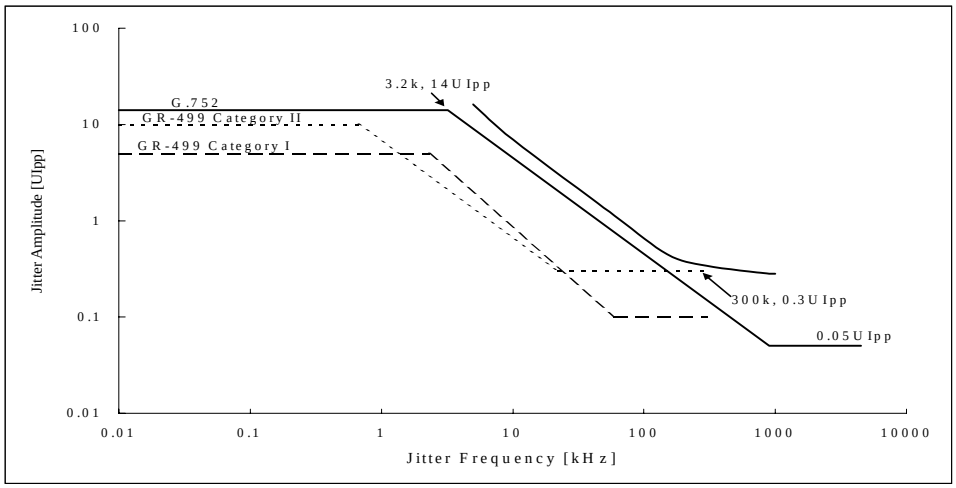


Fig. 11 Jitter Tolerance

TRANSMITTER ANALOG SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V)

Parameter	Condition		Min	Typ	Max	Units
Transmitter amplitude (Note 6)	*DS3/STS1*	LBO=1	700	800	900	mVpk
		LBO=0	1050	1150	1250	mVpk
	E3		920	1000	1080	mVpk

Note; 6. Measured at the line side of the transformer.

DIGITAL CHARACTERISTICS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VIH	(V+) x 0.7	-	(V+)	V
Low-Level Input Voltage	VIL	GND	-	0.5	V
High-Level Output Voltage IOUT=-40µA	VOH	(V+) x 0.8	-	(V+)	V
Low-Level Output Voltage IOUT=1.6mA (Note 7) IOUT=0.4mA (Note 8)	VOL	GND	-	0.4	V
Input Leakage Current (Note 9)				±10	µA

Note; 7. RCLK, RPDATA, RNDATA
8. RLOS, RLOL, TEST4, TEST7
9. Except for $\overline{\text{RESET}}$

RECEIVER SWITCHING SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V; Input: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
RCLK Pulse Width	*DS3*	Tpwh	10.1	11.177	12.2	ns
	(Note 10, 11)	Tpwl	10.1	11.177	12.2	ns
RCLK Pulse Width	*STS-1*	Tpwh	8.7	9.645	10.6	ns
	(Note 12, 11)	Tpwl	8.7	9.645	10.6	ns
RCLK Pulse Width	*E3*	Tpwh	13.1	14.548	16.0	ns
	(Note 13, 11)	Tpwl	13.1	14.548	16.0	ns
EXCLK Duty Cycle (EXCLK Min Rise/Fall time : 5ns)			45	-	55	%
Rise Time, RCLK	(Note 11)	tr	-	-	3.5	ns
Fall Time, RCLK	(Note 11)	tf	-	-	3.5	ns
Delay Time: RCLK high to RPDATA/RNDATA	(Note 14)	Tdcrd	0	-	3.5	ns

TRANSMITTER SWITCHING SPECIFICATIONS

(TA = Tmin to Tmax; V+ = 3.3V±0.3V; GND = 0V; Input: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
TCLK Duty Cycle (TCLK Min Rise/Fall time : 5ns)			30	-	70	%
Rise Time, TCLK	(Note 11)	tr	-	-	3.5	ns
Fall Time, TCLK	(Note 11)	tf	-	-	3.5	ns
Setup Time, TPDATA/TNDATA to TCLK Falling		Tstdc	4	-	-	ns
Hold Time, TPDATA/TNDATA to TCLK Falling		Thtdc	5	-	-	ns

Note; 10. Assumes PLL is locked to 44.736 MHz signal.
11. The sum of the pulse widths must always meet the frequency specifications.
12. Assumes PLL is locked to 51.84 MHz signal
13. Assumes PLL is locked to 34.368MHz signal.
14. Load cap = 15pF.

Fig. 12 Signal Rise and Fall Characteristics

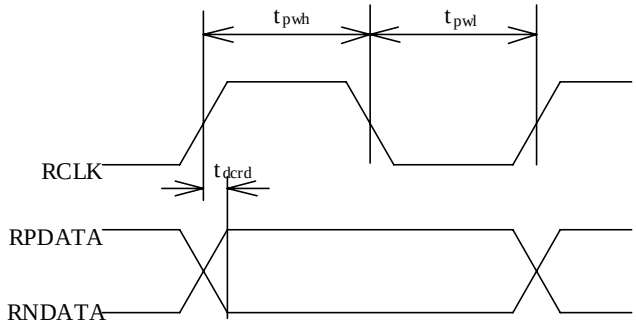


Fig. 13 Recovered Clock and Data Switching Characteristics

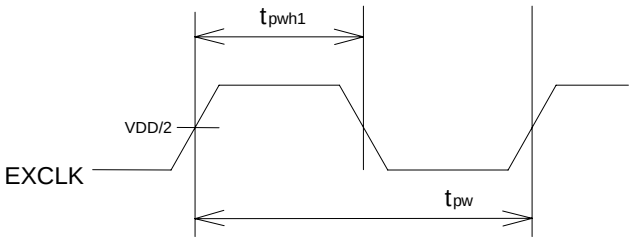


Fig. 14 EXCLK Duty Cycle Requirements

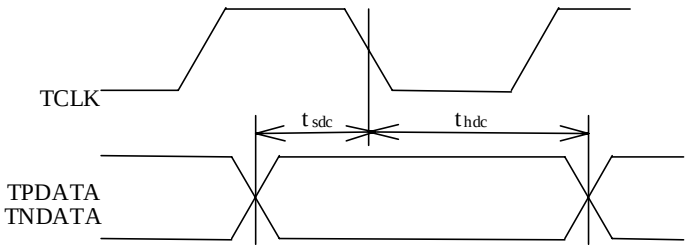
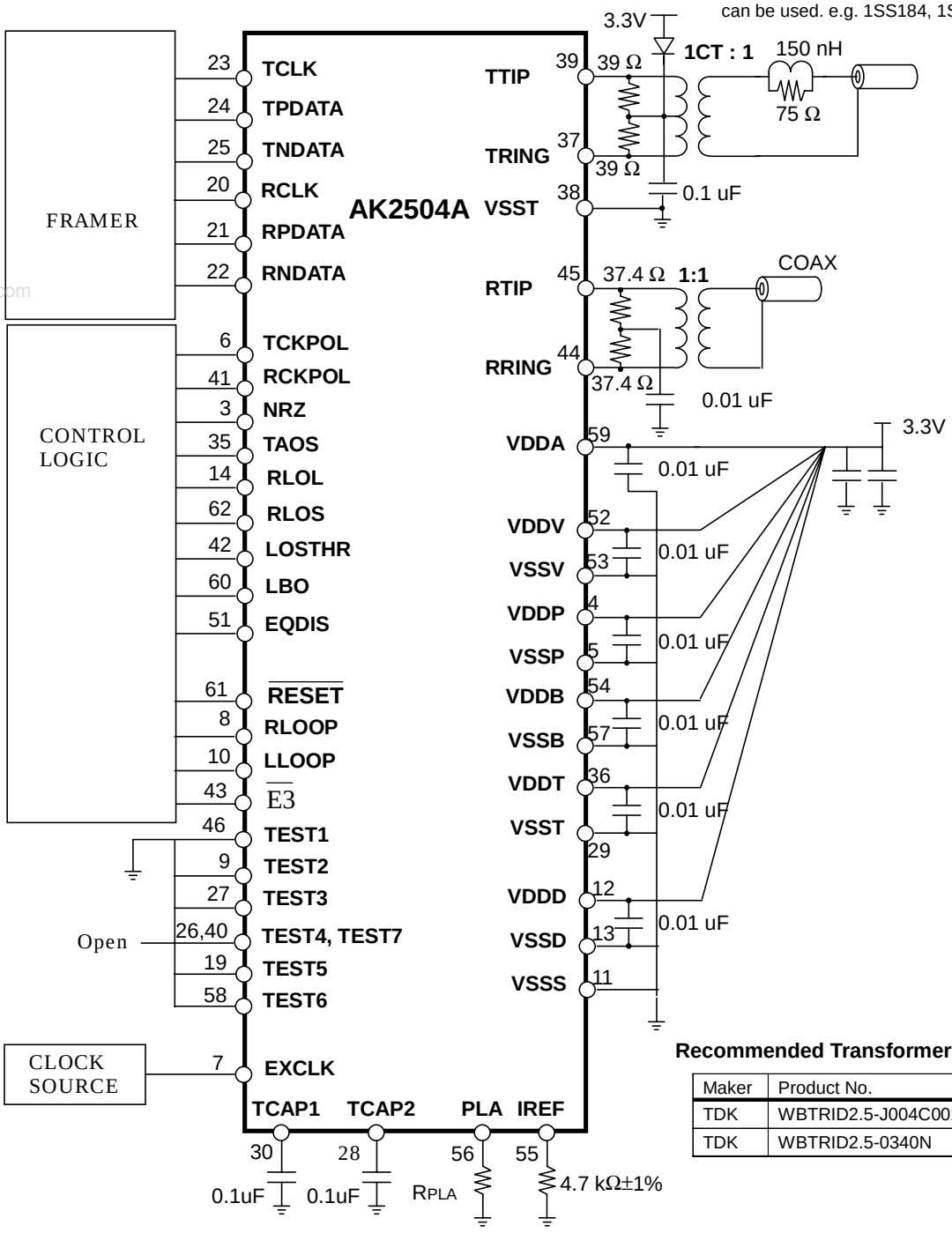


Fig. 15 Transmitter Switching Characteristics

Application Circuit Example

Note :
Leave the following NC pins open.
Pin 1,2,15,16,17,18,31,32,33,34,47,48,49,50,63,64.

Recommended Diode :
Any diode with V(forward) = 0.58V to 0.89V for I(forward)=10mA in all temperature range can be used. e.g. 1SS184, 1SS181



Recommended Transformer :

Maker	Product No.	Ratio
TDK	WBTRID2.5-J004C002	1CT:1
TDK	WBTRID2.5-0340N	1:1

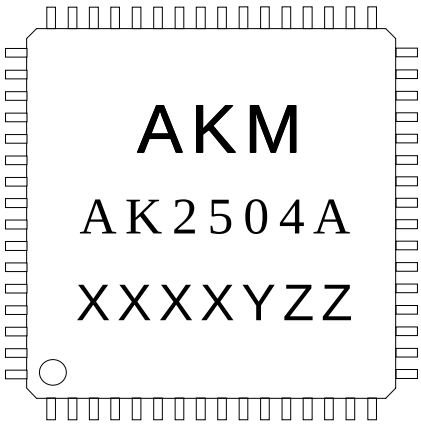
R_{PLA}: 1.33kΩ ±1% for DS3/STS-1, 1.27kΩ ±1% for E3

NOTE) If the power of transmit signal is larger than the requirement, the power can be reduced by increasing the value of R_{PLA}.

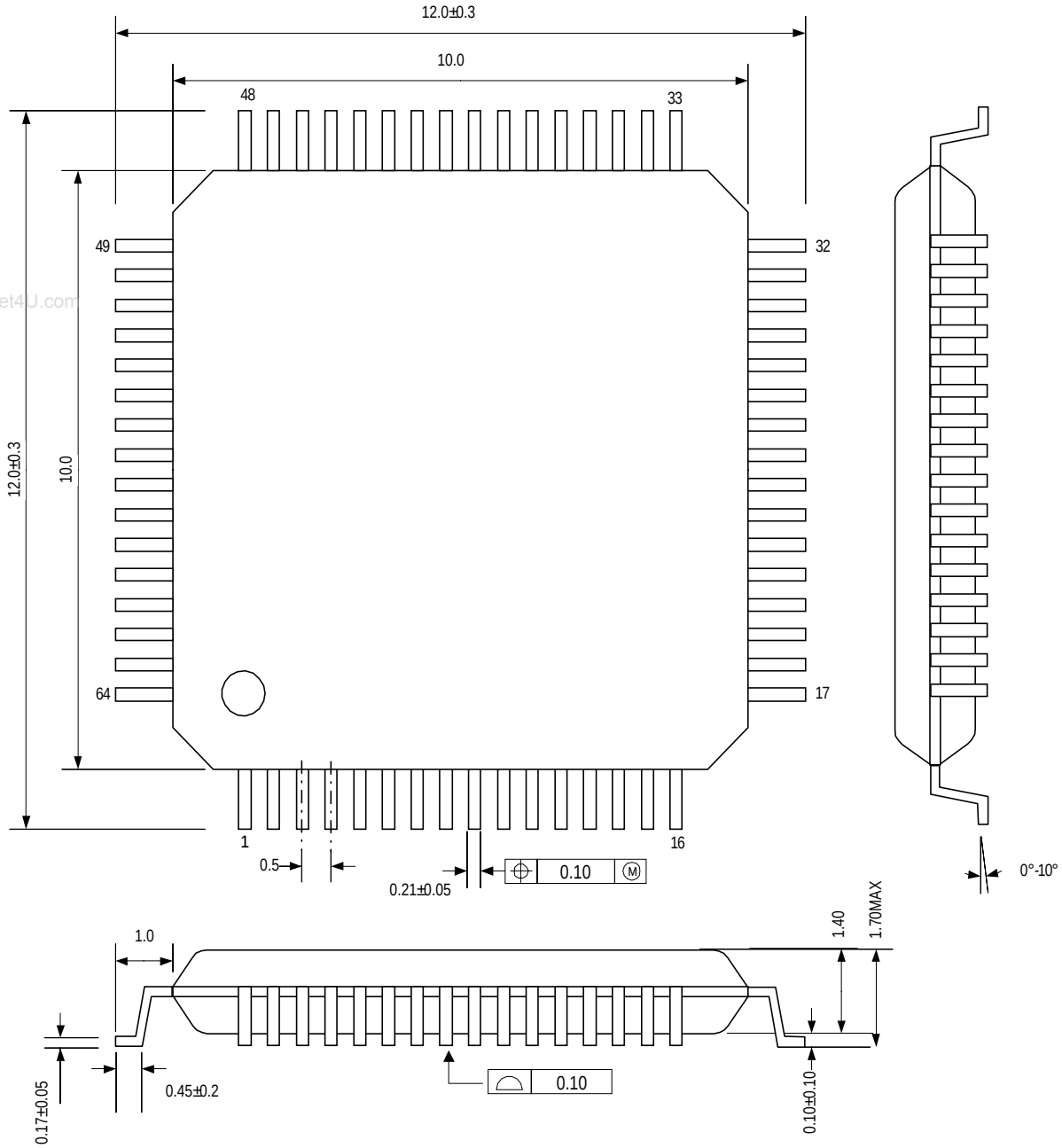
Marking

- 64pin LQFP

(1)Pin #1 indication
(2)Date Code: 7digits XXXXYZZ
(3)Marketing Code: AK2504A
(4)AKM Logo



Outline Dimensions



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