

**AK4203****Stereo Cap-less LINE-Amp and Video-Amp****GENERAL DESCRIPTION**

The AK4203 is an audio stereo cap-less line driver with 1-channel video driver. It eliminates the need for large DC-blocking capacitors with a built-in Charge-pump circuit. The AK4203 achieves 2Vrms outputs with excellent linearity 2Vrms output by single 3.3V power supply. The AK4203 is available in small 16-pin TSSOP, saving the system space and cost.

**FEATURE****Audio Line-Amp**

- Differential Input
- Stereo Cap-less Amplifier (No DC-blocking capacitors required)
- Line-Out level: 2.0Vrms
- THD+N: -90dB
- S/N: 102dB
- Output gain: 6dB
- Low-pass Filter:  $f_c = 130\text{kHz}$
- Pop Noise Free Ground-referenced Output

**Video Amp**

- 1ch Stereo Cap-less Amplifier (No DC-blocking capacitors required)
- Integrated Video Amplifier (+6dB)
- Input Level: 1.5Vpp (max)
- SN: 75dB(typ), Bandwidth: 100kHz ~ 6MHz
- LPF: -0.5dB @ 6.75MHz (typ), -43dB @ 27MHz (typ)
- Video Mute Function
  
- Power Supply: 3.0V ~ 3.6V
- Ta: -20 ~ 85°C
- Package: 16TSSOP

■ Block Diagram

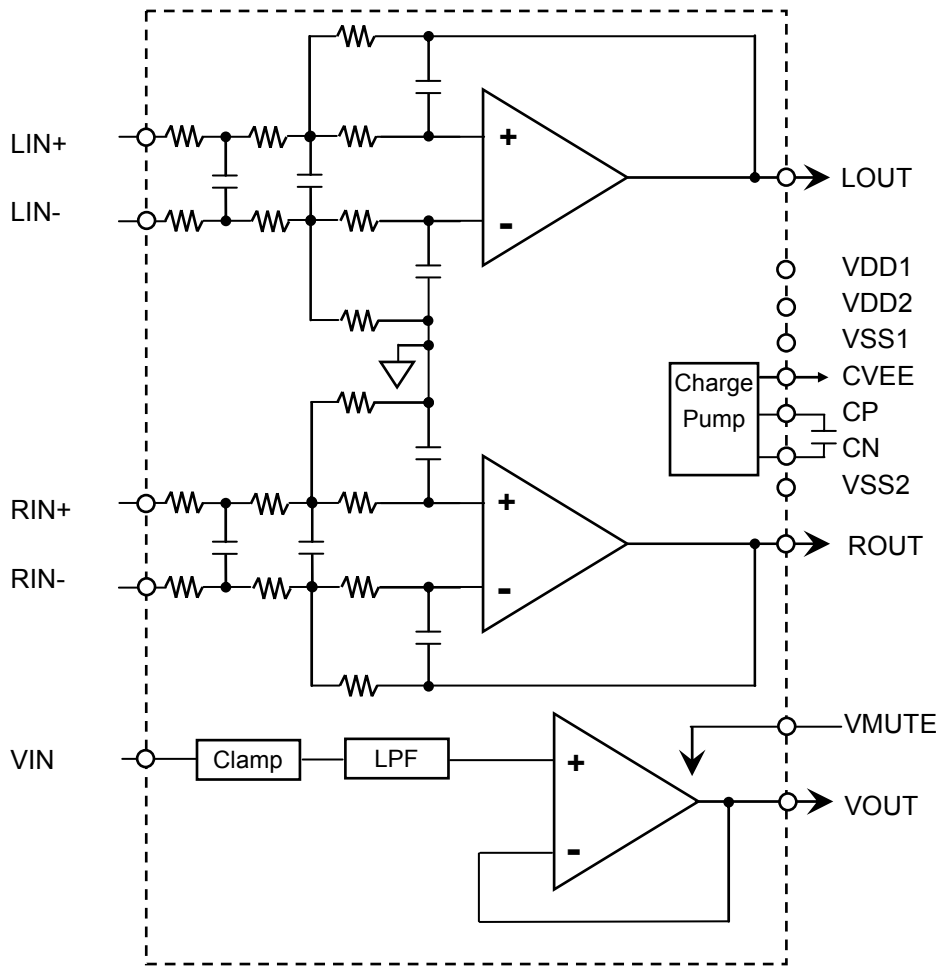


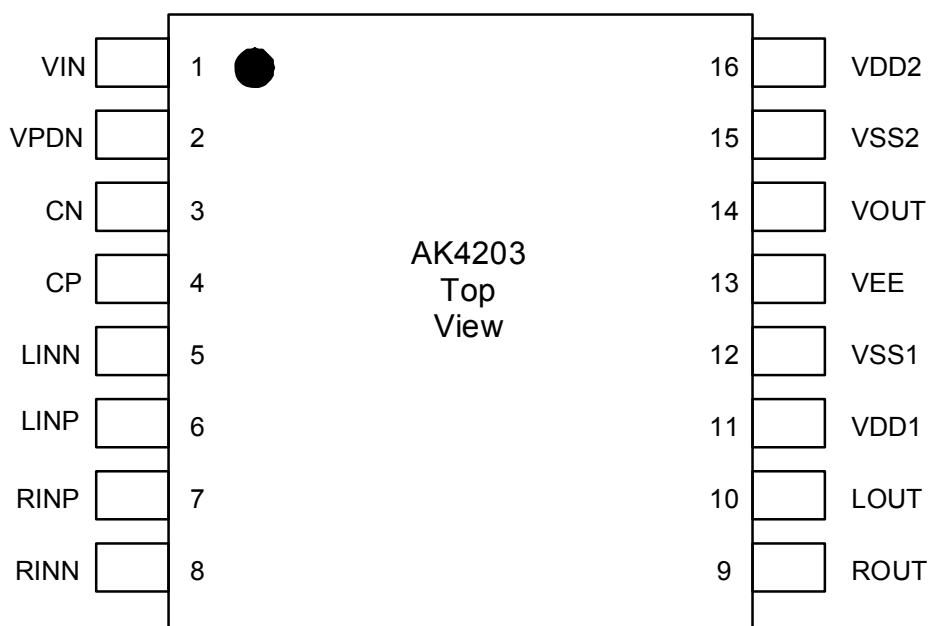
Figure 1. AK4203 Block Diagram

■ **Ordering Guide**

AK4203ET  
AKD4203

-20 ~ +85°C      16pin TSSOP (0.65mm pitch)  
Evaluation board for AK4203

■ **Pin Layout**



<b>PIN/FUNCTION</b>
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No.	Pin Name	I/O	Function
1	VIN	I	Video Signal Input pin
2	VPDN	I	Video Mute pin
3	CN	I	Negative Charge Pump Capacitor Terminal pin
4	CP	O	Positive Charge Pump Capacitor Terminal pin
5	LINN	I	Lch Audio Negative Input pin
6	LINP	I	Lch Audio Positive Input pin
7	RINP	I	Rch Audio Positive Input pin
8	RINN	I	Rch Audio Negative Input pin
9	ROUT	O	Audio Output pin (R channel)
10	LOUT	O	Audio Output pin (L channel)
11	VDD1	-	Power Supply 1 pin, 3.0V~3.6V Connect to VSS1 with a 0.1μF ceramic capacitor in parallel with a 10μF 3.3V electrolytic capacitor.
12	VSS1	-	Ground 1 pin
13	VEE	O	Negative Voltage Output pin Connect to VSS1 with a 10μF 3.3V electrolytic capacitor.
14	VOUT	O	Video Signal Output pin
15	VSS2	-	Ground 2 pin
16	VDD2	-	Power Supply 2 pin, 3.0V~3.6V Connect to VSS2 with a 0.1μF ceramic capacitor in parallel with a 10μF 3.3V electrolytic capacitor.

### ■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Digital Input	VPDN	VSS1
Audio Input	LINP/N, RINP/N	VSS1
Audio, Video Output	AOUT, VOUT	Open

<b>ABSOLUTE MAXIMUM RATINGS</b>
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(VSS1=VSS2 =0V (Note 1))

Parameter	Symbol	min	max	Unit
Power Supply	VDD1 VDD2	-0.3	4.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Audio Input Voltage (Note 4)	VINA	VEE -0.3	VDD1 +0.3	V
Video Input Voltage	VINV	-0.3	VDD2 +0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages are respect to ground.

Note 2. VSS1 and VSS2 must be connected to the same analog plane.

Note 3. VDD1 and VDD2 must be the same voltage.

Note 4. VEE: The VEE pin voltage

VEE is generated by the internal charge pump circuit. VEE voltage is “-VDD1 +0.2V” (typ).

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

<b>RECOMMEND OPERATING CONDITIONS</b>
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(VSS1=VSS2 =0V)

Parameter	Symbol	min	typ	max	Unit
Power Supply	VDD1	3.0	3.3	3.6	V
	VDD2	3.0	3.3	3.6	V

Note 3. VDD1 and VDD2 must be the same voltage.

Note: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

<b>ELECTICAL CHARACTERISTICS</b>
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(Ta=25°C; VDD1= VDD2 = 3.3V; VSS1= VSS2 = 0V)

Power Supplies					
Parameter		min	typ	max	Unit
Power Supply (VDD1+VDD2) Normal Operation (Note 5)			18	30	mA

Note 5. No input and no load.

**ANALOG CHARACTERISTICS (Audio)**

( $T_a=25^{\circ}\text{C}$ ;  $V_{DD1}=V_{DD2}=3.3\text{V}$ ;  $V_{SS1}=V_{SS2}=0\text{V}$ ; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz;  $R_L=5\text{k}\Omega$ , unless otherwise specified)

Parameter	min	typ	max	Unit
Output Level (Note 6)	-	2	-	Vrms
Gain	-	6	-	dB
THD+N (at 2Vrms output, $V_{DD1}\geq 3.135\text{V}$ )	-	90	-	dB
Dynamic Range (-60dBFS with A-weighted)	-	102	-	dB
S/N (A-weighted)	-	102	-	dB
Inter channel Isolation	-	100	-	dB
Output Offset Voltage	-	$\pm 0$	$\pm 5$	mV
LPF Frequency Response	-3dB	-	130	kHz

Note 6.  $V_{DD1}\geq 3.135\text{V}$ , THD+N=-90dB.

**ANALOG CHARACTERISTICS (Video)**

( $T_a=25^{\circ}\text{C}$ ;  $V_{DD1}=V_{DD2}=3.3\text{V}$ ;  $V_{SS1}=V_{SS2}=0\text{V}$ ; unless otherwise specified, Note 7, Note 8)

Parameter	Conditions	min	typ	max	Unit
Input Signal				1.5	Vpp
Output Gain	Input=0.2Vp-p, 100kHz	-	6	-	dB
Output Signal	$f=100\text{kHz}$ , THD=-30dB.	2.52			Vpp
Frequency Response	Response at 6.75MHz	-	-0.5	-	dB
Input=0.2Vpp, Sin Wave (0dB at 100kHz)	Response at 27MHz	-	-43	-	dB
Group Delay Distortion	$ GD3\text{MHz}-GD6\text{MHz} $	-	10	-	nsec
S/N (*)	BW= 100kHz to 6MHz.	-	81		dB
Load Resistance	$R1+R2$ (Note 9)	140	150	160	$\Omega$
Load Capacitance	C1 (Note 9)			400	pF
	C2 (Note 9)			15	pF

Note 7. The analog characteristics are specified at the pin of each output.

Note 8. Input Sync Tip Level=-0.43V~-0.14V(the sync chip level based on the pedestal level)

Horizontal Line Sync Pulse=4.0 $\mu\text{s}$  ~5.4 $\mu\text{s}$ , Equalizing Pulse=2.0 $\mu\text{s}$  ~2.7 $\mu\text{s}$ , Serration Pulse=4.0 $\mu\text{s}$  ~5.4 $\mu\text{s}$

Note 9. Refer to the [Figure 2](#).

\*CCIR 567 weighting.

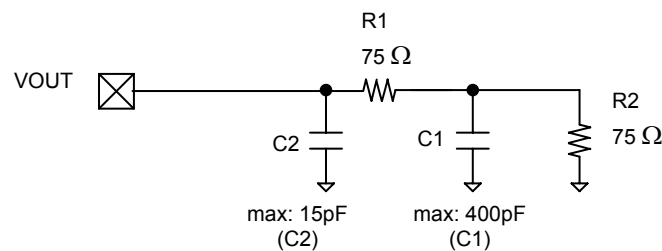


Figure 2. Load Resistance  $R1+R2$  and Load Capacitance  $C1/C2$ .

**OPERATION OVERVIEW**

■ **Charge Pump Circuit**

Internal negative power supply circuit (Figure 3) supplies the negative voltage to the video amp and the video amp 0V output is used for a pedestal level in Figure 4 and Figure 5. Therefore, the output coupling capacitor can be removed.

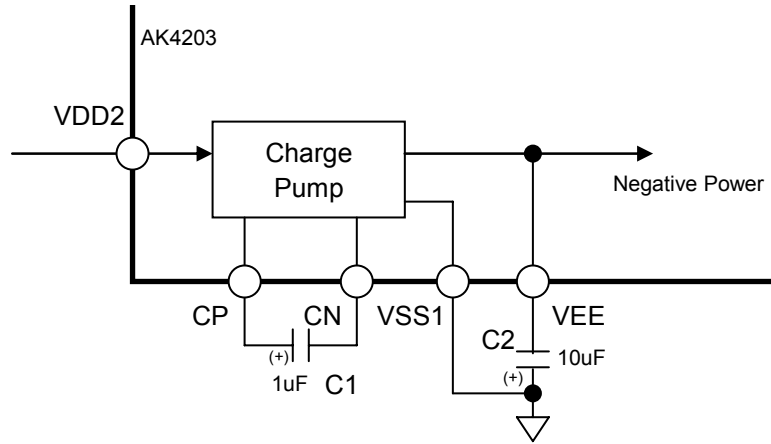


Figure 3. Charge Pump Circuit

Note 10. C1 and C2 should be low ESR (Equivalent Series Resistance) capacitors. When those capacitors have the polarity, each positive polarity pins should be connected to CP and VSS1 side.

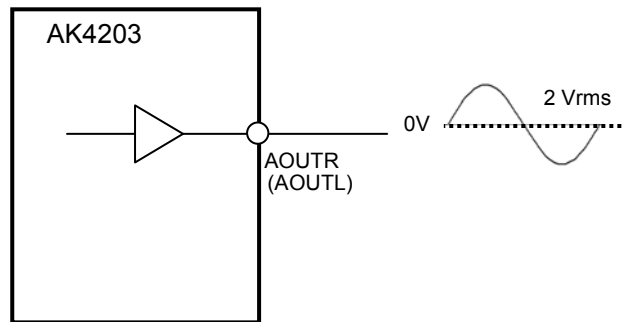


Figure 4. Audio Signal Output

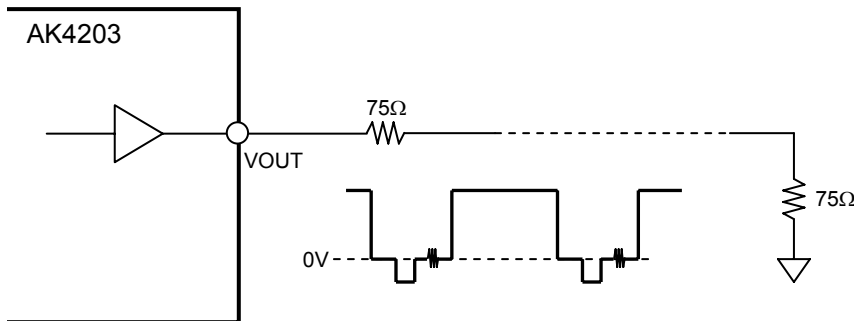


Figure 5. Video Signal Output

## ■ Audio Circuit Power-Up Sequence

When power supply pins of the AK4203 are fed, the audio circuit and charge pump are powered-up automatically as shown below.

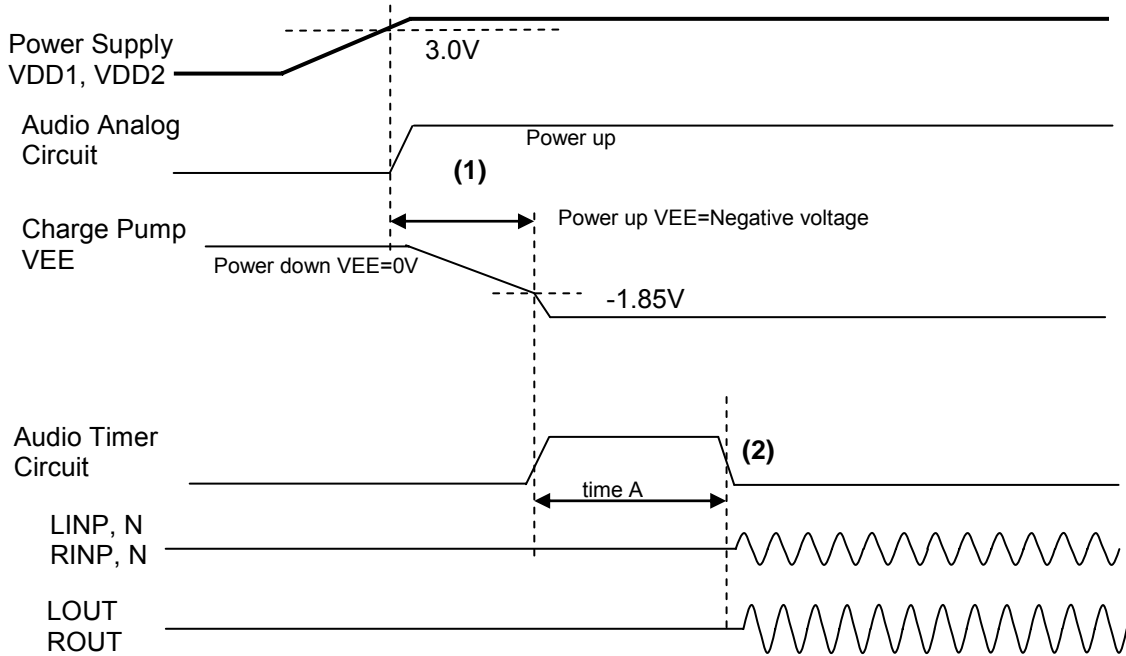


Figure 6. System Reset Diagram

Note:

- (1) When VDD1 and VDD2 are powered-up, audio analog output is connected to VSS internally via a mute switch. The charge pump is powered-up in slow start mode and VEE reaches -1.85V in 0.4ms. Do not apply a negative voltage to LINP/N and RINP/N pins until the charge pump output is stabilized.
- (2) When the VEE reaches -1.85V, the audio timer circuit starts counting the "timeA" period (max. 15ms).
- (3) After the "timeA" period, the mute switch is released and the audio output is enabled.
- (4) No audible click noise occurs under normal conditions.



■ Video Circuit Power-Up Sequence

The video circuit of the AK4203 is powered-up when the VPDN pin becomes “H”.

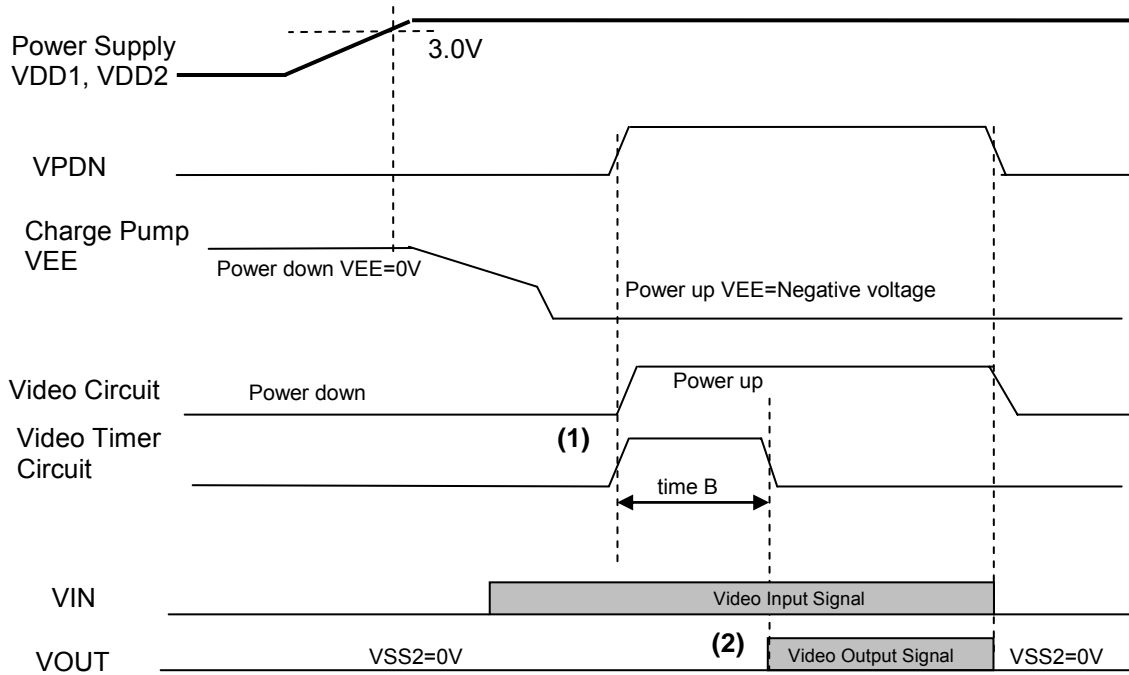


Figure 7. System Reset Diagram

Note:

- (1) When the VPDN pin goes to “H”, the video timer circuit starts counting “time B” period (max. 100ms).
- (2) After the “time B” period, the video output becomes enabled exiting 0V state.

**SYSTEM DESIGN**

Figure 8 shows the system connection diagram for the AK4203. An evaluation board [AKD4203] demonstrates the optimum layout, power supply arrangements and measurement results.

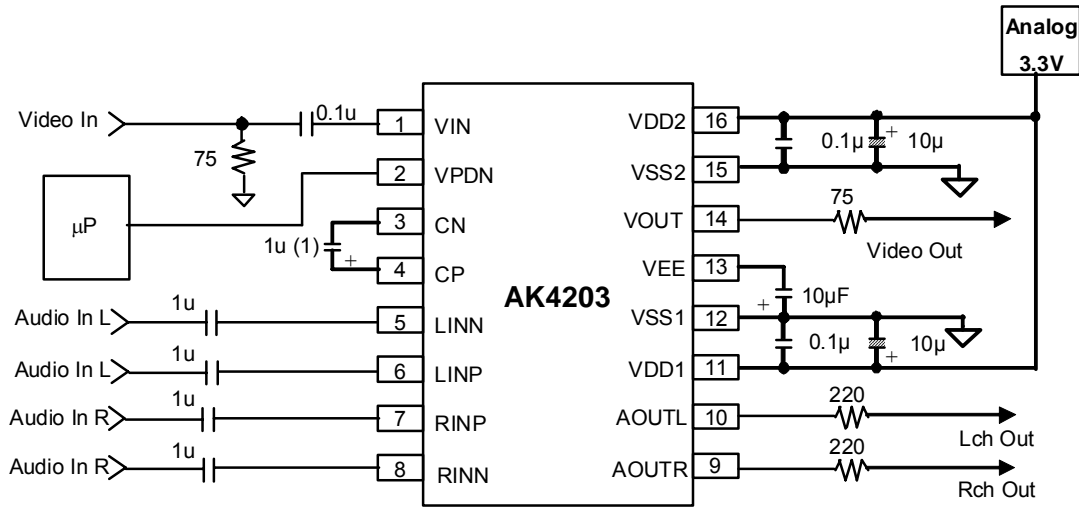


Figure 8. Typical Connection Diagram

## 1. Grounding and Power Supply Decoupling

The AK4203 requires careful attention to power supply and grounding arrangements. VDD1 and VDD2 are usually supplied from the analog supply in the system. If VDD1 and VDD2 are supplied separately, they must be powered-up at the same time. VSS1 and VSS2 pins must be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

## 2. Notes for Drawing a Board

Analog input and output pins should be as near as possible in order to avoid unwanted coupling into the AK4203. Unused pins should be open.

## 3. Analog Input

### 3-1. Audio Signal Input

The audio signal inputs are differential input. The output signal of LINP/RINP has the same phase. Connect a capacitor about 1 $\mu$ F to each input pin for AC coupling.

### 3-2. Video Signal Input

Tip Sync level is fixed by an internal clamp circuit. Connect a capacitor about 0.1 $\mu$ F to the VIN pin for AC coupling.

## 4. Analog Output

### 4-1. Audio Signal Output

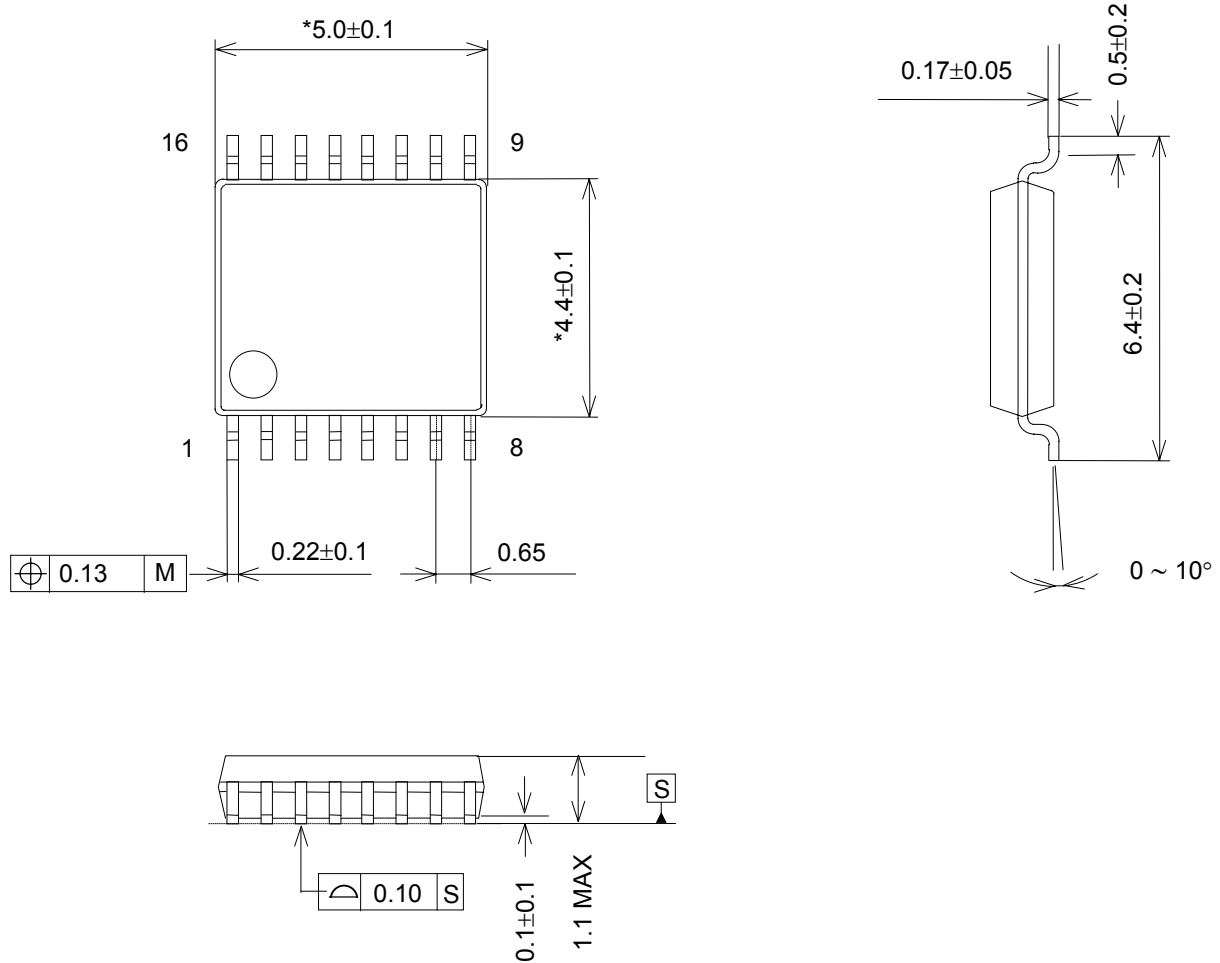
The audio signal outputs are single-ended output. The output ranges to 2.0V<sub>rms</sub> (typ) centered VSS (0V, typ) via LPF. The DC offset is less than  $\pm 5$ mV.

### 4-2. Video Signal Output

The integrated 1-channel video amplifier has drivability for a load resistance of 150 $\Omega$ . The output gain is +6dB (typ) via LPF. DC offset is less than  $\pm 100$ mV.

PACKAGE

16pin TSSOP (Unit: mm)

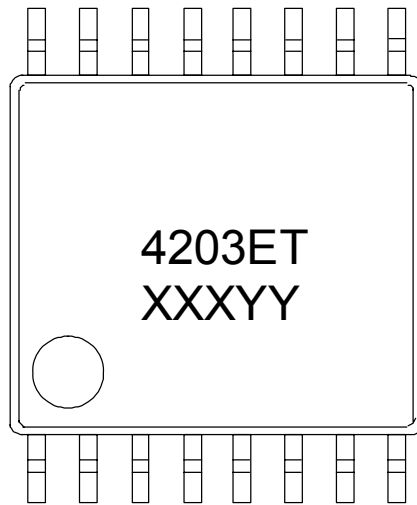


NOTE: Dimension "\*" does not include mold flash.

■ Package & Lead Frame Material

- Package molding compound: Epoxy Resin, Halogen (Br, Cl) Free
- Lead frame material: Cu Alloy
- Lead frame surface treatment: Solder (Pb free) Plate

**MARKING**



- 1) Pin #1 indication
- 2) Date Code: XXXYY (5 digits)  
     XXX: Date Code  
     YY: Lot#
- 3) Marketing Code: 4203ET

**REVISION HISTORY**

Date (YY/MM/DD)	Revision	Reason	Page	Contents
12/02/16	00	First Edition		

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