



# AK4360

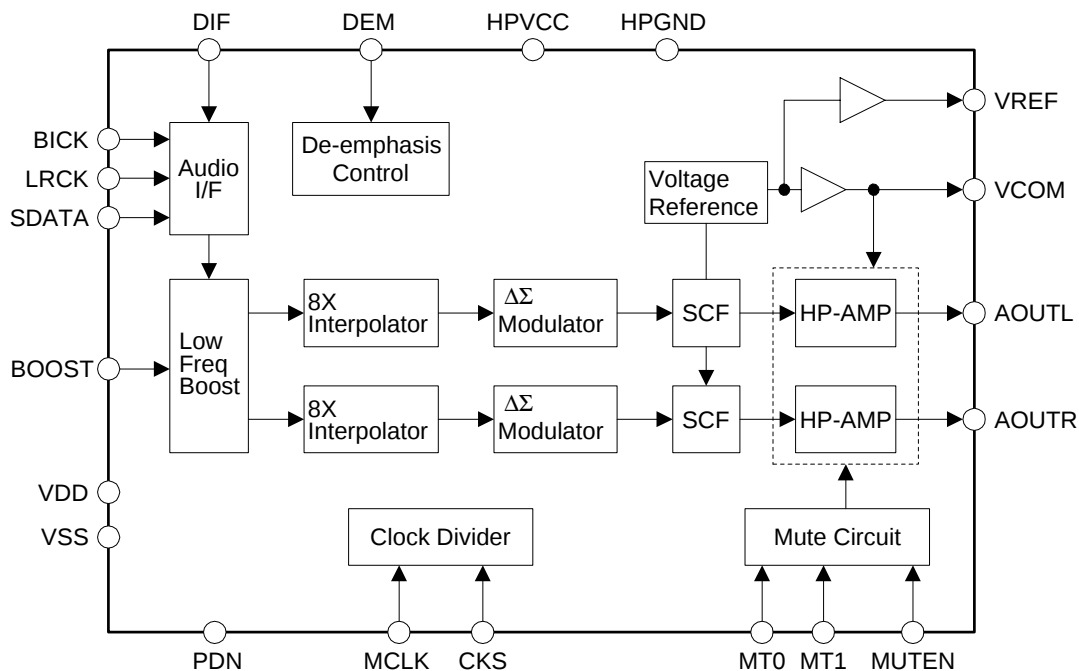
## Low Power 2ch $\Delta\Sigma$ DAC with HP-AMP

### GENERAL DESCRIPTION

The AK4360 is a 20bit low voltage & power DAC with Headphone Amplifier for digital audio system. The AK4360 uses the new developed Multi-Bit  $\Delta\Sigma$  architecture, this new architecture achieves S/N=92dB at low voltage operation. The AK4360 integrates SCF increasing performance for systems with excessive clock jitter. The low power and small package make this point ideal for the portable audio system like MD, MP3, etc.

### FEATURES

- **Advanced Multi-Bit  $\Delta\Sigma$  DAC**
- **Sampling Rate Ranging: 8kHz ~ 50kHz**
- **On chip perfect filtering 8 times FIR interpolator**
- **Digital de-emphasis for 44.1kHz sampling**
- **Master clock: 256fs or 384fs**
- **Digital Audio I/F Format: 2's compliment, MSB first**
  - 20bit I<sup>2</sup>S or 16bit LSB justified
- **THD+N: -48dB (-11dB output)**
- **D-Range, S/N: 92dB**
- **Low Frequency Boost Function**
- **Click Noise Free Circuit**
- **On chip Headphone Amplifier**
  - 6.5mW x 2ch@16 $\Omega$  (THD+N = 10%, HPVCC = 1.2V)
- **Low Voltage Operation: DAC: 2V (1.8V~3.3V), HP-AMP: 1.2V (0.9V~3.3V)**
- **Low power Dissipation: 12mW**
- **Ta = -10 ~ 70°C**
- **Small Package: 24pin VSOP**



## ■ Ordering Guide

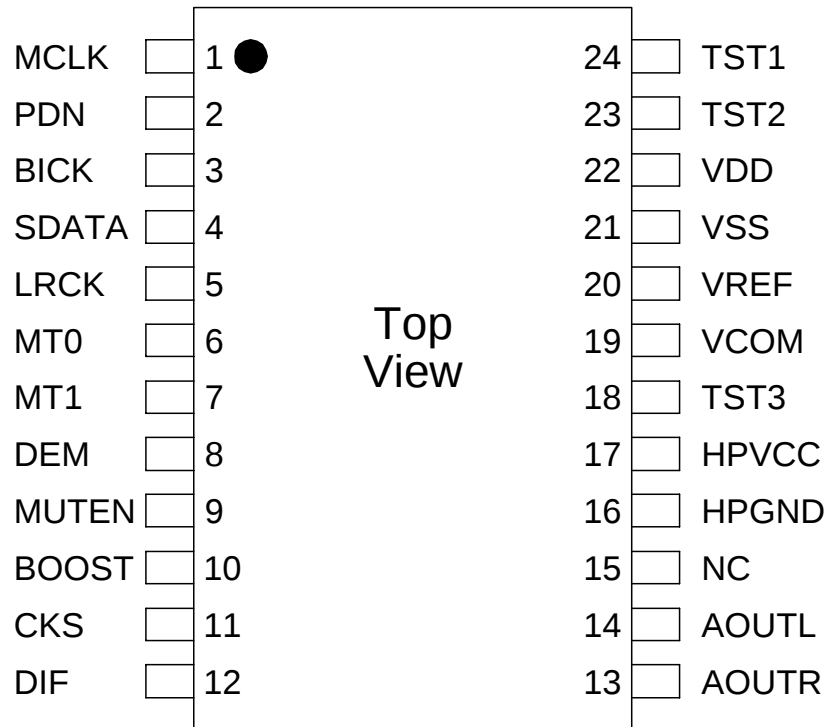
AK4360VF  
AKD4360

-10 ~ +70°C

24pin VSOP (0.65mm pitch)

Evaluation Board for AK4360

## ■ Pin Layout



| PIN/FUNCTION |          |     |                                                                                                                                                                            |
|--------------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| No.          | Pin Name | I/O | Function                                                                                                                                                                   |
| 1            | MCLK     | I   | Master Clock Pin                                                                                                                                                           |
| 2            | PDN      | I   | Power-Down Pin (Internal pull-down pin)<br>When at “L”, the AK4360 is in power-down mode and is held in reset.<br>The AK4360 should always be reset upon power-up.         |
| 3            | BICK     | I   | Audio Serial Data Clock Pin                                                                                                                                                |
| 4            | SDATA    | I   | Audio Serial Data Input Pin                                                                                                                                                |
| 5            | LRCK     | I   | Input/Output Channel Clock Pin                                                                                                                                             |
| 6            | MT0      | I   | MUTE Timer select Pin                                                                                                                                                      |
| 7            | MT1      | I   |                                                                                                                                                                            |
| 8            | DEM      | I   | De-emphasis Enable Pin<br>When at “H”, de-emphasis of fs=44.1kHz is enabled.                                                                                               |
| 9            | MUTEN    | I   | Mute pin (Internal pull-down pin)<br>When at “L”, analog outputs are muted.<br>(Analog outputs are connected to HPGND.)                                                    |
| 10           | BOOST    | I   | Low Frequency Boost Enable Pin<br>“H”: Enable “L”: Disable                                                                                                                 |
| 11           | CKS      | I   | Master Clock Select Pin<br>“L”: 256fs “H”: 384fs                                                                                                                           |
| 12           | DIF      | I   | Digital I/F format pin (Internal pull-down pin)<br>“L”: 16bit LSB justified, “H”: IIS compatible                                                                           |
| 13           | AOUTR    | O   | Rch Analog Output Pin                                                                                                                                                      |
| 14           | AOUTL    | O   | Lch Analog Output Pin                                                                                                                                                      |
| 15           | NC       | -   | NC pin (No internal bonding)                                                                                                                                               |
| 16           | HPGND    | -   | Ground Pin for Headphone Amplifier                                                                                                                                         |
| 17           | HPVCC    | -   | Power Supply Pin for Headphone Amplifier                                                                                                                                   |
| 18           | TST3     | O   | Test Pin (Always Open)                                                                                                                                                     |
| 19           | VCOM     | O   | Common Voltage Pin, 0.48V (typ, respects to VSS)<br>Normally connected to VSS pin with a 0.1μF ceramic capacitor in parallel with a 1.0μF electrolytic capacitor.          |
| 20           | VREF     | O   | Reference Voltage Output Pin, 1.2V (typ, respects to VSS)<br>Normally connected to VSS pin with a 0.1μF ceramic capacitor in parallel with a 1.0μF electrolytic capacitor. |
| 21           | VSS      | -   | Ground Pin for D/A Converter                                                                                                                                               |
| 22           | VDD      | -   | Power Supply Pin for D/A Converter                                                                                                                                         |
| 23           | TST2     | O   | Test Pin                                                                                                                                                                   |
| 24           | TST1     | I   | Test Pin (Internal pull-down pin)                                                                                                                                          |

Note: All input pins except NC and pull-down pins should not be left floating.

|                                 |
|---------------------------------|
| <b>ABSOLUTE MAXIMUM RATINGS</b> |
|---------------------------------|

(VSS, HPGND=0V; Note 1)

| Parameter                                    |                       | Symbol | min  | max            | Units |
|----------------------------------------------|-----------------------|--------|------|----------------|-------|
| Power Supplies                               | DAC                   | VDD    | -0.3 | 4.6            | V     |
|                                              | HP-AMP                | HPVCC  | -0.3 | 4.6            | V     |
|                                              | VSS – HPGND  (Note 2) | ΔGND   | -    | 0.3            | V     |
| Input Current (any pins except for supplies) |                       | IIN    | -    | ±10            | mA    |
| Input Voltage                                |                       | VIND   | -0.3 | VDD+0.3 or 4.6 | V     |
| Ambient Temperature                          |                       | Ta     | -10  | 70             | °C    |
| Storage Temperature                          |                       | Tstg   | -65  | 150            | °C    |

Note 1. All voltages with respect to ground.

Note 2. VSS and HPGND is same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

|                                         |
|-----------------------------------------|
| <b>RECOMMENDED OPERATING CONDITIONS</b> |
|-----------------------------------------|

(VSS, HPGND=0V; Note 1)

| Parameter      |        | Symbol | min | typ | max | Units |
|----------------|--------|--------|-----|-----|-----|-------|
| Power Supplies | DAC    | VDD    | 1.8 | 2.0 | 3.3 | V     |
|                | HP-AMP | HPVCC  | 0.9 | 1.2 | 3.3 | V     |

Note 1. All voltages with respect to ground.

\*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

**ANALOG CHARACTERISTICS**

(Ta=25°C; VDD=2.0V, HPVCC=1.2V, VSS=HPGND=0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; Measurement frequency=10Hz ~ 20kHz; Load impedance is a serial connection with  $R_L=16\Omega$  and  $C_L=220\mu\text{F}$ ; unless otherwise specified)

| Parameter                                                 | min  | typ   | max | Units         |
|-----------------------------------------------------------|------|-------|-----|---------------|
| <b>Headphone Output Dynamic Characteristics:</b> (Note 3) |      |       |     |               |
| THD+N (0dB Output, 6.5mW)                                 |      | -20   | -   | dB            |
| (-11dB Output, 0.5mW)                                     |      | -48   | -40 | dB            |
| (-30dB Output)                                            |      | -60   | -   | dB            |
| Dynamic Range (-60dB Output, A-weight)                    | 86   | 92    |     | dB            |
| S/N (A-weight)                                            | 86   | 92    |     | dB            |
| Interchannel Isolation                                    | 75   | 90    |     | dB            |
| <b>DC Accuracy</b>                                        |      |       |     |               |
| Interchannel Gain Mismatch                                |      | 0.3   | 0.5 | dB            |
| Gain Drift                                                | -    | 200   | -   | ppm/°C        |
| Output Voltage (-11dB Output)                             | 0.25 | 0.275 | 0.3 | Vpp           |
| Load Resistance                                           | 16   |       |     | $\Omega$      |
| <b>Power Supplies</b>                                     |      |       |     |               |
| Power Supply Current                                      |      |       |     |               |
| Normal Operation (PDN = MUTEN= "H")                       |      |       |     |               |
| VDD                                                       |      | 4.0   | 6.0 | mA            |
| HPVCC (Digital "0" Data Input)                            |      | 3.4   | 6.5 | mA            |
| Power-Down Mode (PDN = MUTEN= "L")                        |      |       |     |               |
| VDD+HPVCC (Note 4)                                        |      | 10    | 100 | $\mu\text{A}$ |
| Power Supply Rejection (Note 5)                           | -    | 50    | -   | dB            |

Note 3. Measured by Audio Precision, System Two.

Note 4. In case of power-down mode (PDN = MUTEN = "L"), all digital input pins including clock pins (MCLK, BICK and LRCK) are held VDD or VSS.

Note 5. PSR is applied to VDD with 1kHz, 100mVpp.

| FILTER CHARACTERISTICS                                             |                  |        |      |       |       |       |
|--------------------------------------------------------------------|------------------|--------|------|-------|-------|-------|
| (Ta=25°C; VDD=1.8 ~ 3.3V, HPVCC=0.9 ~ 3.3V; fs=44.1kHz; DEM = “L”) |                  |        |      |       |       |       |
| Parameter                                                          |                  | Symbol | min  | typ   | max   | Units |
| DAC Digital Filter: (Mote 6)                                       |                  |        |      |       |       |       |
| Passband                                                           | ±0.05dB (Note 7) | PB     | 0    |       | 20.0  | kHz   |
|                                                                    | -6.0dB           |        | -    | 22.05 | -     | kHz   |
| Stopband                                                           | (Note 7)         | SB     | 24.1 |       |       | kHz   |
| Passband Ripple                                                    |                  | PR     |      |       | ±0.02 | dB    |
| Stopband Attenuation                                               |                  | SA     | 57   |       |       | dB    |
| Group Delay                                                        | (Note 8)         | GD     | -    | 19.1  | -     | 1/fs  |
| Group Delay Distortion                                             |                  | ΔGD    |      | 0     |       | μs    |
| DAC Digital Filter + Analog Filter: (Note 6)                       |                  |        |      |       |       |       |
| Frequency Response                                                 | 0 ~ 20.0kHz      | FR     | -    | ±0.5  | -     | dB    |
| BOOST Filter: (Note 9)                                             |                  |        |      |       |       |       |
| Frequency Response                                                 | 20Hz             |        |      | 4.73  |       | dB    |
|                                                                    | 45Hz             |        |      | 2.6   |       | dB    |
|                                                                    | 1kHz             |        |      | 0     |       | dB    |

Note 6. BOOST = "L".

Note 7. The passband and stopband frequencies scale with fs.

For example, PB=0.4535\*fs(@ $\pm 0.05\text{dB}$ ), SB=0.546\*fs(@-54dB).

Note 8. The calculating delay time which occurred by digital filtering. This time is from setting the 20bit data of both channels to input register to the output of analog signal.

Note 9. When BOOST pin is "H", if full scale signal inputs, AK4360 clips at low frequency.

| DC CHARACTERISTICS        |        |        |     |          |               |  |
|---------------------------|--------|--------|-----|----------|---------------|--|
| (Ta=25°C; VDD=1.8 ~ 3.3V) |        |        |     |          |               |  |
| Parameter                 | Symbol | min    | typ | max      | Units         |  |
| High-Level Input Voltage  | VIH    | 70%VDD | -   | -        | V             |  |
| Low-Level Input Voltage   | VIL    | -      | -   | 30%VDD   | V             |  |
| Input Leakage Current     | Iin    | -      | -   | $\pm 10$ | $\mu\text{A}$ |  |

Note 10. PDN, MUTEN, DIF, TST1 pins have internal pull-down devices . (typ 100k $\Omega$ )

|                                  |
|----------------------------------|
| <b>SWITCHING CHARACTERISTICS</b> |
|----------------------------------|

(Ta=25°C; VDD=1.8 ~ 3.3V)

| Parameter                               | Symbol     | min     | typ     | max      | Units    |
|-----------------------------------------|------------|---------|---------|----------|----------|
| <b>Master Clock Timing</b>              |            |         |         |          |          |
| 256fs:                                  | fCLK       | 2.048   | 11.2896 | 12.8     | MHz      |
| Pulse Width Low                         | tCLKL      | 28      |         |          | ns       |
| Pulse Width High                        | tCLKH      | 28      |         |          | ns       |
| 384fs:                                  | fCLK       | 3.072   | 16.9344 | 19.2     | MHz      |
| Pulse Width Low                         | tCLKL      | 23      |         |          | ns       |
| Pulse Width High                        | tCLKH      | 23      |         |          | ns       |
| <b>LRCK Frequency</b>                   |            |         |         |          |          |
| Duty Cycle                              | fs<br>Duty | 8<br>45 | 44.1    | 50<br>55 | kHz<br>% |
| <b>Audio Interface Timing</b> (Note 11) |            |         |         |          |          |
| BICK Period                             | tBCK       | 312.5   |         |          | ns       |
| BICK Pulse Width Low                    | tBCKL      | 100     |         |          | ns       |
| Pulse Width High                        | tBCKH      | 100     |         |          | ns       |
| LRCK Edge to BICK “↑” (Note 12)         | tLRB       | 50      |         |          | ns       |
| BICK “↑” to LRCK Edge (Note 12)         | tBLR       | 50      |         |          | ns       |
| SDATA Hold Time                         | tSDH       | 50      |         |          | ns       |
| SDATA Setup Time                        | tSDS       | 50      |         |          | ns       |
| <b>Reset Timing</b>                     |            |         |         |          |          |
| PDN Pulse Width (Note 13)               | tPD        | 300     |         |          | ns       |

Note 11. Refer to the operating overview section “Audio Interface Format”.

Note 12. BICK rising edge must not occur at the same time as LRCK edge.

Note 13. The AK4360 can be reset by bringing PDN = “L” to “H” only upon power up.

# Timing Diagram

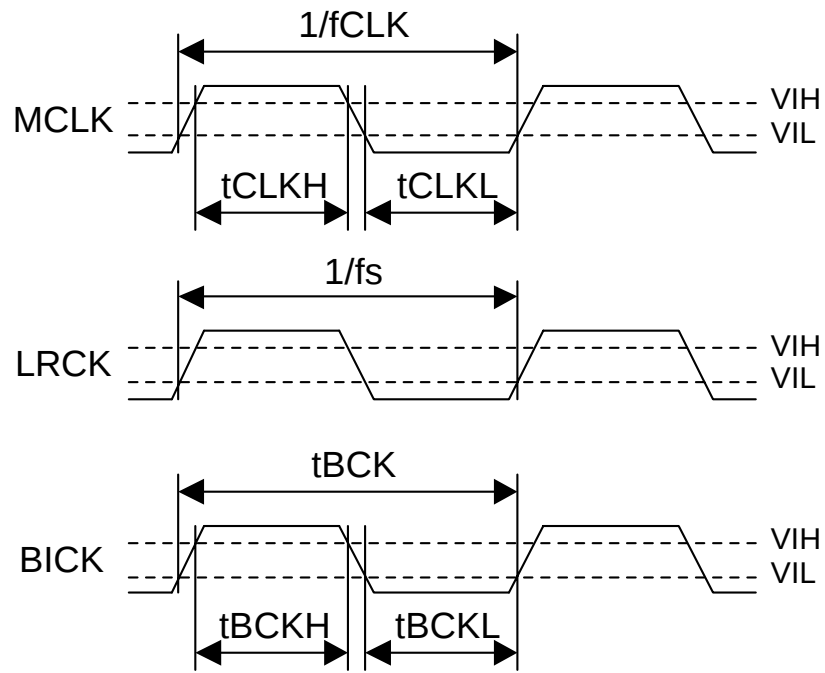


Figure 1. Clock Timing

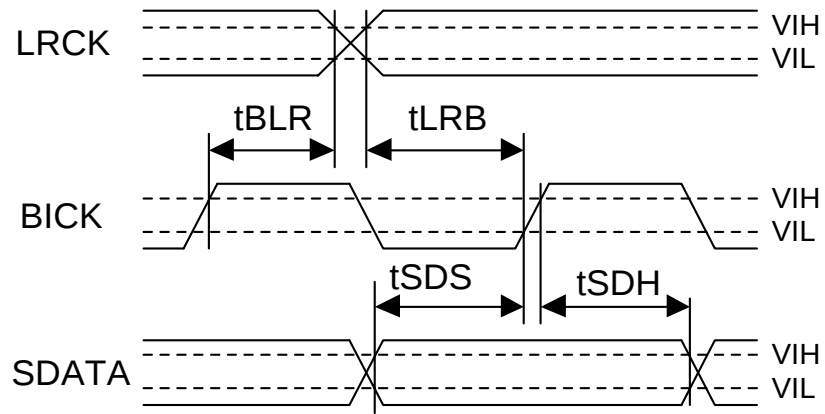


Figure 2. Audio Interface Timing

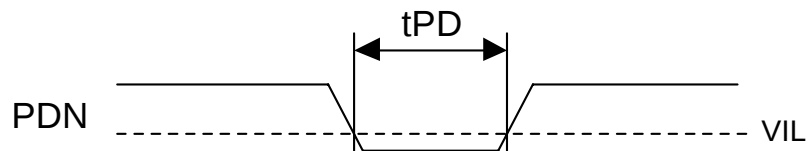


Figure 3. Power down &amp; Reset Timing

## OPERATION OVERVIEW

### ■ System Clock

The external clocks that are required to operate the AK4360 are MCLK (256fs/384fs), LRCK (fs) and BICK (32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The frequency of MCLK is determined by the sampling rate (LRCK) and CKS pin. Setting CKS = “L” selects an MCLK frequency of 256fs while setting CKS = “H” selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs\*2/3). Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK4360.

All external clocks (MCLK, BICK, LRCK) should always be present whenever the AK4360 is in normal operation mode (PDN = “H”). If these clocks are not provided, the AK4360 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4360 should be in the power-down mode(PDN = “L”).

| LRCK (fs) | MCLK             |                  | BICK (64fs) |
|-----------|------------------|------------------|-------------|
|           | CKS = “L”: 256fs | CKS = “H”: 384fs |             |
| 32.0kHz   | 8.1920MHz        | 12.2880MHz       | 2.0480MHz   |
| 44.1kHz   | 11.2896MHz       | 16.9344MHz       | 2.8224MHz   |
| 48.0kHz   | 12.2880MHz       | 18.4320MHz       | 3.0720MHz   |

Table 1. Examples of System Clock

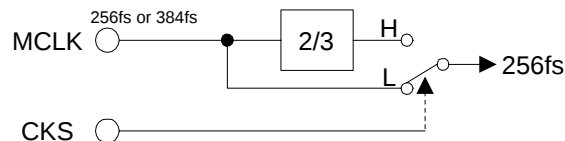


Figure 4. MCLK Divider Circuit

### ■ Audio Interface Format

The AK4360 interfaces with external system by using SDATA, BICK and LRCK pins. Two types of data format are available and one of them is selected by setting DIF pin. In mode 1, if BICK ≥ 40fs, 16bit data followed by four zeros also could be input, 18bit data followed by two zeros also could be input. In all modes, the serial data is MSB first and 2's complement format.

| DIF pin | Mode                                  | BICK   | Figure   |
|---------|---------------------------------------|--------|----------|
| L       | 0: 16bit LSB Justified                | ≥ 32fs | Figure 5 |
| H       | 1: 16bit, I <sup>2</sup> S Compatible | ≥ 32fs | Figure 6 |
|         | 1: 18bit, I <sup>2</sup> S Compatible | ≥ 36fs |          |
|         | 1: 20bit, I <sup>2</sup> S Compatible | ≥ 40fs |          |

Table 2. Audio Formats

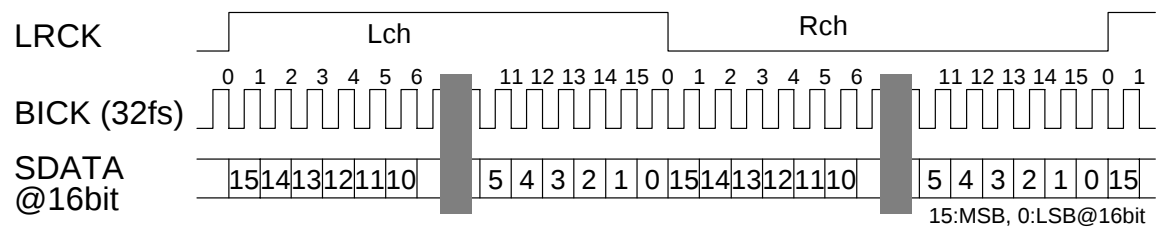


Figure 5. Mode 0 Timing

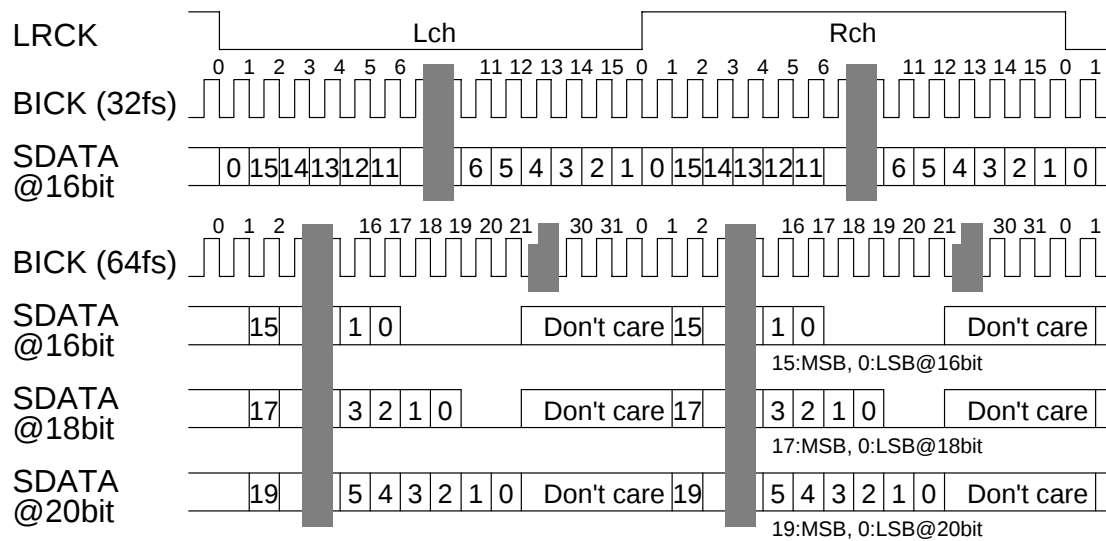


Figure 6. Mode 1 Timing

### ■ De-emphasis filter

The AK4360 includes the digital de-emphasis filter ( $t_c=50/15\mu s$ ) by IIR filter. This filter corresponds to 44.1kHz sampling. Setting DEM pin “H” enables the de-emphasis.

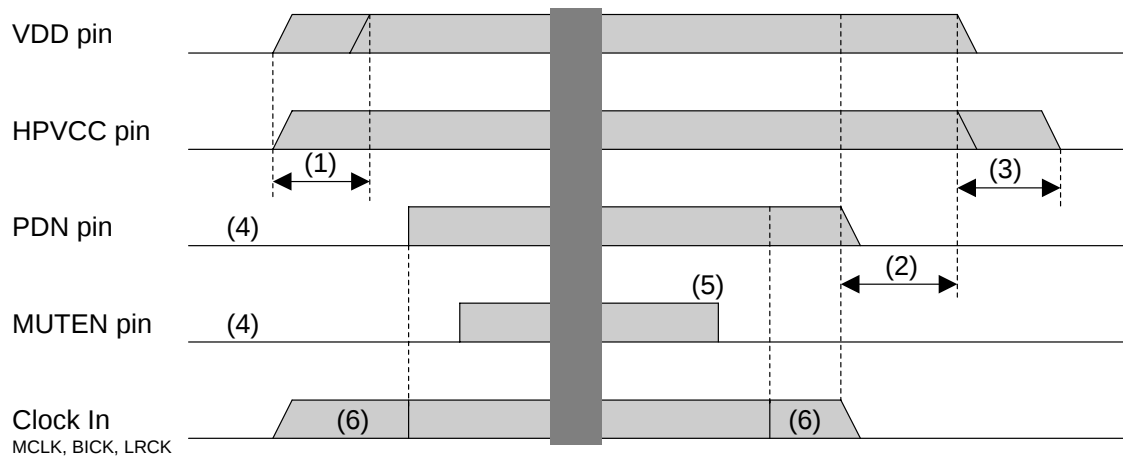
### ■ Low Frequency Boost Function

When BOOST pin goes “H”, high pass filter characteristics which is made by a external capacitor (220 $\mu F$ ) and a resistor (16 $\Omega$ ) can be corrected. The cut-off frequency is 45Hz@fs=44.1kHz.

|             | 20Hz | 45Hz   | 1kHz |
|-------------|------|--------|------|
| Boost = “L” | -8dB | -3dB   | 0dB  |
| Boost = “H” | -3dB | -0.5dB | 0dB  |

Table 3. Low Frequency Characteristics (fs = 44.1kHz)

## ■ Power Up/Down Sequence



### Notes:

- (1) HPVCC and VDD pins should be powered-up at the same time or HPVCC pin should be powered-up earlier than VDD pin.
- (2) VDD pin should be powered-down passed by more than 30ms after PDN pin = "L".
- (3) HPVCC and VDD pins should be powered-down at the same time or VDD pin should be powered-down earlier than HPVCC pin.
- (4) PDN and MUTEN pins should be "L" as the click noise occurs at power-up.
- (5) HP-Amp outputs should be muted by MUTEN pin = "L" before power-down.
- (6) In case of PDN pin = MUTEN pin = "L", the clock may be stopped.

Figure 7. Power Up/Down Sequence example

## ■ Mute Function

In the normal operation (PDN = “H” and MUTEN = “H”), the analog outputs do the gain mute operation and level mute operation when MUTEN pin goes “L”, the analog outputs are muted to HPGND (0V) finally. The level mute operation is fixed to 1024/fs. The gain mute time is set by MT0 and MT1 pins. If the sampling frequency is slow, the gain mute time can be shortened by the set of MT0 and MT1 pins (Refer to Table 4). Figure 8 shows the mute on/off timing example. \*fs means sampling frequency.

When PDN pin goes “H” and MUTEN pin goes “L”, HP-AMP is only powered-down. And when PDN and MUTEN pins go “L”, HP-AMP and DAC are powered-down. Then, power supply current about a few 10μA is flowed to internal mute control circuit from HPVCC power supply. (Refer to Table 5.)

| MT1 | MT0 | Gain Mute Time    | Level Mute Time | Total Time |
|-----|-----|-------------------|-----------------|------------|
| L   | L   | x 1 (=21845/fs)   | 1024/fs         | 22869/fs   |
| L   | H   | x 1/2 (=10923/fs) | 1024/fs         | 11947/fs   |
| H   | L   | x 1/4 (=5461/fs)  | 1024/fs         | 6485/fs    |
| H   | H   | x 3/4 (=16384/fs) | 1024fs          | 17408/fs   |

Table 4. Mute Time Setting

| Mode | PDNpin | MUTEN pin | DAC State        | HP-Amp State     |
|------|--------|-----------|------------------|------------------|
| 1    | H      | H         | Normal operation | Normal operation |
| 2    | H      | L         | Normal operation | Power-down       |
| 3    | L      | L         | Power-down       | Power-down       |
| 4    | L      | H         | Inhibit          |                  |

Table 5. About PDN and MUTEN pins

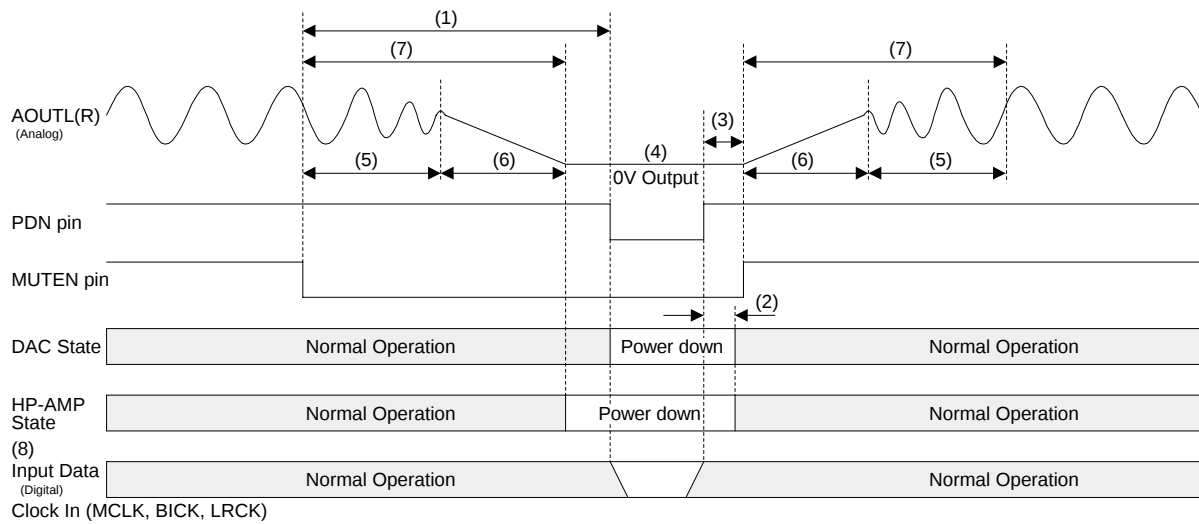


Figure 8. Mute on/off timing example

- (1): PDN pin should change "H" into "L" after analog outputs are muted.
- (2): This is time (about 1ms) until DAC and HP-AMP are powered up after PDN = "H".
- (3): After DAC and HP-AMP are powered-up, MUTEN pin should be "H".
- (4): When MUTEN pin goes "L", analog outputs are connected to HPGND.
- (5): Level mute time:  $1024/f_s = 23\text{ms}@f_s=44.1\text{kHz}$
- (6): Gain mute time:  $21845/f_s = 495\text{ms}@f_s=44.1\text{kHz}$ , MT1-0 = "00"
- (7): Mute total time:  $22869/f_s = 518\text{ms}@f_s=44.1\text{kHz}$ , MT1-0 = "00"
- (8): When the external clocks (MCLK, BICK and LRCK) are stopped, the DAC and HP-AMP should be in the power-down mode (PDN = "L", MUTEN = "L").

| $f_s$   | MT1 | MT0 | Mute Total Time              |
|---------|-----|-----|------------------------------|
| 8kHz    | H   | L   | $6485/f_s (= 811\text{ms})$  |
| 44.1kHz | H   | H   | $17408/f_s (= 395\text{ms})$ |

Table 6. Recommended Mute Time Setting Example

## SYSTEM DESIGN

Figure 9 shows the system connection diagram. An evaluation board [AKD4360] is available in order to allow an easy study on the layout of a surrounding circuit.

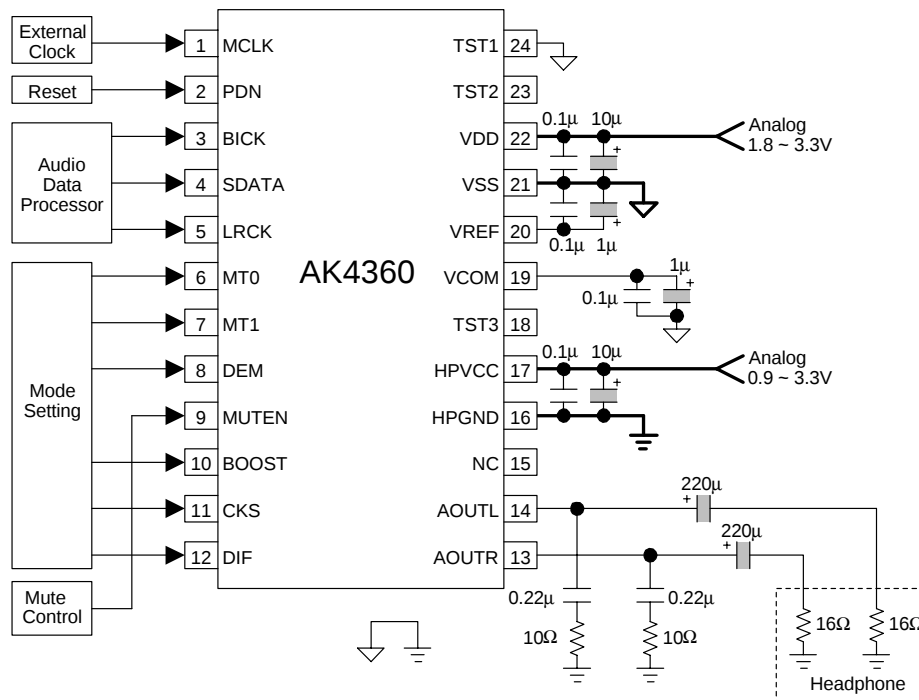


Figure 9. Typical Connection Diagram

### Notes:

- LRCK = fs, BICK ≥ 32fs, MCLK = 256fs/384fs.
- All input pins except NC and pull-down pins should not be left floating.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- Digital signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling the AK4360.

### 1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor for high frequency should be placed as near to VDD as possible.

### 2. Voltage Reference

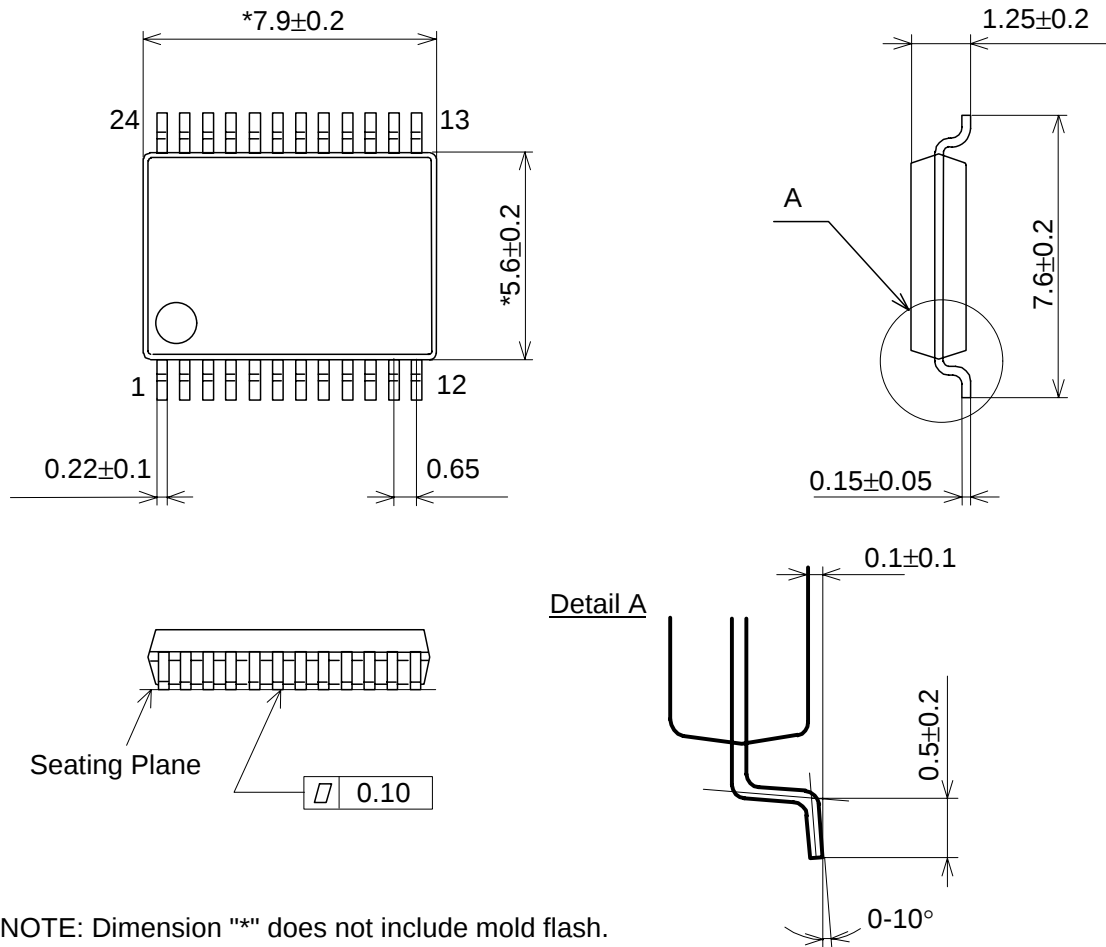
The voltage reference is output on the VREF pin. An electrolytic capacitor 1.0µF parallel with a 0.1µF ceramic capacitor are attached between VREF and VSS pins. Especially, the ceramic capacitor should be connected to VREF pin as near as possible. No load current may be taken from the VREF output pin. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the AK4360.

### 3. Analog Outputs

The analog outputs are single-ended and centered around the VCOM voltage. The output signal range is typically 1.0Vpp. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage (typ: 0.48V) for 0000H(@16bit).

|                |
|----------------|
| <b>PACKAGE</b> |
|----------------|

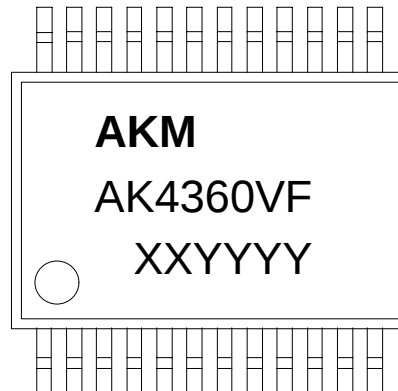
## 24pin VSOP (Unit: mm)



### ■ Package & Lead frame material

|                               |              |
|-------------------------------|--------------|
| Package molding compound:     | Epoxy        |
| Lead frame material:          | Cu           |
| Lead frame surface treatment: | Solder plate |

|                |
|----------------|
| <b>MARKING</b> |
|----------------|



Contents of XYYYYY

XX: Lot#

YYYY: Date Code

#### IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  - a. A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  - b. A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.