AK4519

Low Power 20 bit ΔΣ ADC&DAC with HPF

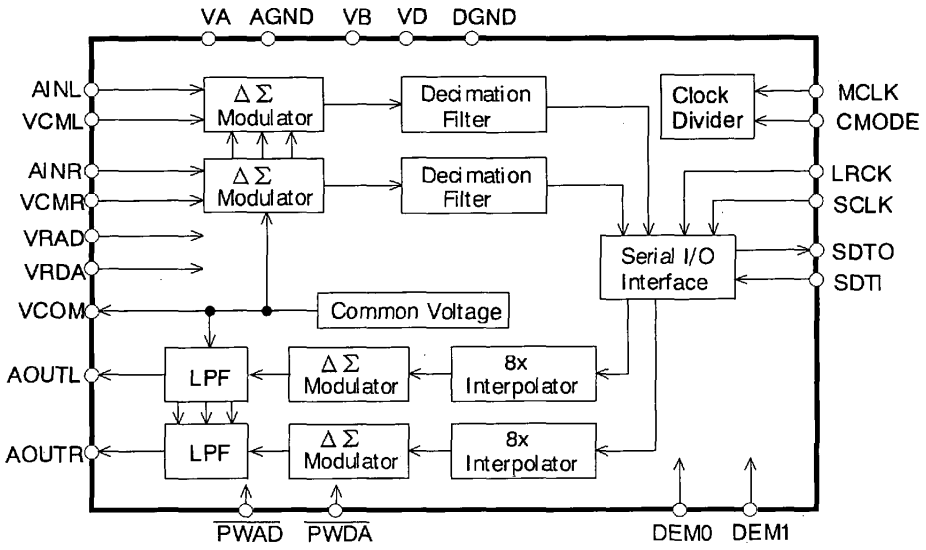
GENERAL DESCRIPTION

AK4519 is low voltage 20bit A/D & D/A converter for portable digital audio system. In the AK4519, the loss of accuracy form clock jitter is also improved by using SCF techniques for on-chip post filter. Analog signal input/output of the AK4519 are single-ended, therefore, external filter is not required.

The AK4519 is low power dissipation and be able to powered-down ADC and DAC independently, so the AK4519 is suitable for portable digital audio system.

FEATURES

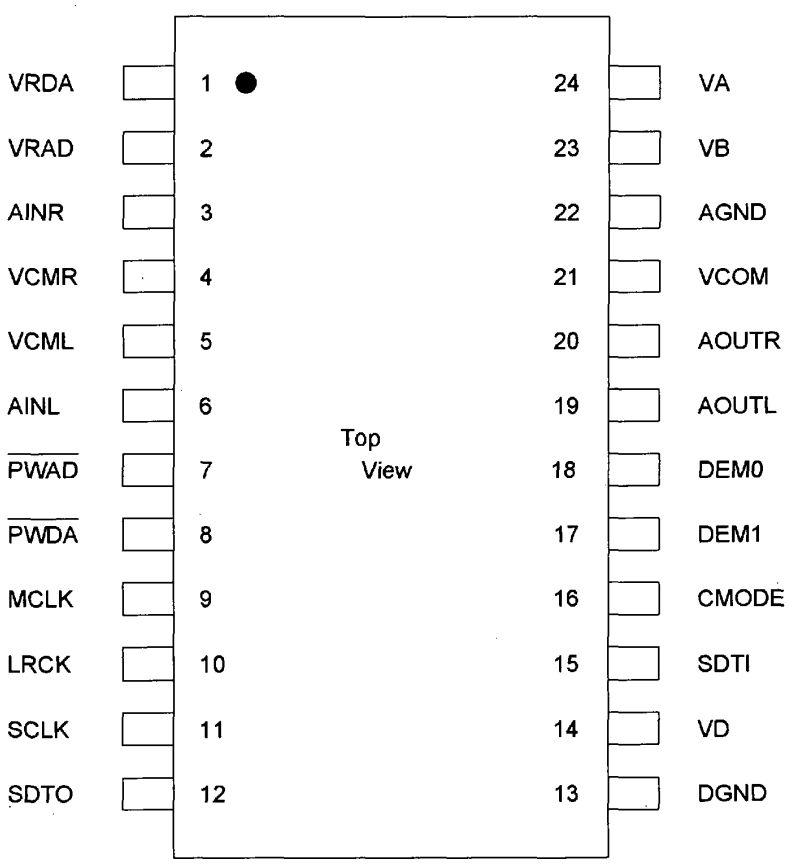
- ☐ HPF for DC-offset cancel (fc=3.4Hz)
- ☐ Single-ended ADC
  - S/(N+D): 83dB
  - Dynamic Range, S/N: 89dB at 2.5V, 90dB at 3V
- ☐ Single-ended DAC
  - 2nd order SCF + 2nd order CTF
  - Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling
  - S/(N+D): 83dB
  - Dynamic Range, S/N: 92dB at 2.5V, 93dB at 3V
- ☐ Audio I/F format
  - ADC:20bit MSB justified, DAC:20bit LSB justified, MSB First, 2's Compliment
- ☐ High Jitter Tolerance
- ☐ Sampling Rate: 8kHz to 50kHz
- ☐ Master Clock: 256fs or 384fs or 512fs
- ☐ Power Supply: 2.4 to 4.0V
- ☐ Low Power Dissipation: 33.3mW at 2.5V, 41.1mW at 3V
- ☐ Small 24pin VSOP Package



■ Ordering Guide

AK4519VF	-10~+70°C	24pinVSOP (0.65mm Pitch)
AKD4519	Evaluation board for AK4519	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	VRDA	I	Voltage Reference Input Pin for DAC, VA
2	VRAD	I	Voltage Reference Input Pin for ADC, VA
3	AINR	I	Rch Analog Input Pin
4	VCMR	O	Rch Common Voltage Output Pin, 0.45 x VA Normally connected to AGND with a 0.1uF Ceramic capacitor in parallel with a 4.7uF electrolytic.
5	VCML	O	Lch Common Voltage Output Pin, 0.45 x VA Normally connected to AGND with a 0.1uF Ceramic capacitor in parallel with a 4.7uF electrolytic.
6	AINL	I	Lch Analog Input Pin
7	$\overline{\text{PWAD}}$	I	ADC Power-Down Mode Pin "L": Power down
8	$\overline{\text{PWDA}}$	I	DAC Power-Down Mode Pin "L": Power down
9	MCLK	I	Master Clock Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	SCLK	I	Audio Serial Data Clock Pin
12	SDTO	O	Audio Serial Data Output Pin
13	DGND	-	Digital Ground Pin
14	VD	-	Digital Power Supply Pin
15	SDTI	I	Audio Serial Data Input Pin
16	CMODE	I	Master Clock Select Pin "H": 384fs or 512fs, "L": 256fs
17	DEM1	I	De-emphasis Frequency Select Pin
18	DEM0	I	De-emphasis Frequency Select Pin
19	AOUTL	O	Lch Analog Output Pin
20	AOUTR	O	Rch Analog Output Pin
21	VCOM	O	Common Voltage Output Pin, 0.45 x VA Normally connected to AGND with a 0.1uF Ceramic capacitor in parallel with a 4.7uF electrolytic.
22	AGND	-	Analog Ground Pin
23	VB	-	Substrate Pin
24	VA	-	Analog Power Supply Pin

ABSOLUTE MAXIMUM RATINGS

(AGND,DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	VA	-0.3	4.6	V
	Digital	VD	-0.3	4.6	V
	Substrate	VB	-0.3	4.6	V
	VD-VB	VDB	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VB+0.3	V
Ambient Temperature (power applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1 . All voltages with respect to ground

WARNING: Operation at or beyond these limits may result in permanent dynamic to the device.
Normal operation not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	VA	2.4	2.5	4.0	V
(Note 2)	Digital	VD	2.4	2.5	VA	V
	Substrate (Note 3)	VB	2.4	2.5	4.0	V
Voltage Reference(VRAD,VRDA pin voltage)		VREF	0.75xVA	-	VA	V

Note: 1 . All voltages with respect to ground.
2 . VA should be powered at the same time or earlier than VD.
3 . Connect to VA.

ANALOG CHARACTERISTICS

(Ta=25°C; VA,VB,VD,VRAD,VRDA=2.5V; fs=44.1kHz; Signal Frequency=1kHz;
Measurement frequency=10Hz~20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics(Note 4): Analog Source Impedance=470Ω					
Resolution				20	Bits
S/(N+D)		75	83		dB
	(Note 5)	-	83	-	
DR (-60dB Input, A-Weighted)		82	89		dB
	(Note 5)	-	90	-	
S/N (A-Weighted)		82	89		dB
	(Note 5)	-	90	-	
Interchannel Isolation		80	90		dB
Interchannel Gain Mismatch			0.2	0.3	dB
Input Voltage	(Note 6)	1.35	1.5	1.65	Vpp
Input Resistance		30	50		kΩ
Power Supply Rejection	(Note 7)		50		dB
DAC Analog Output Characteristics: (Note 8)					
Resolution				20	Bits
S/(N+D)		75	83		dB
	(Note 5)	-	83	-	
DR (-60dB Output, A-Weighted)		86	92		dB
	(Note 5)	-	93	-	
S/N (A-Weighted)		86	92		dB
	(Note 5)	-	93	-	
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.3	dB
Output Voltage	(Note 6)	1.35	1.5	1.65	Vpp
Load Resistance		10			kΩ
Load Capacitance				25	pF
Power Supply Rejection	(Note 7)		50		dB
Power Supplies					
Power Supply Current					
Analog: VA+VB					
AD+DA	$\overline{PWAD}$="H",$\overline{PWDA}$="H"		10.5	15.8	mA
AD	$\overline{PWAD}$="H",$\overline{PWDA}$="L"		4.8	7.2	mA
DA	$\overline{PWAD}$="L",$\overline{PWDA}$="H"		6.5	9.8	mA
Power down (Note 9)	$\overline{PWAD}$="L",$\overline{PWDA}$="L"		20	100	uA
Digital: VD					
AD+DA	$\overline{PWAD}$="H",$\overline{PWDA}$="H"		2.8	4.2	mA
AD	$\overline{PWAD}$="H",$\overline{PWDA}$="L"		1.8	2.7	mA
DA	$\overline{PWAD}$="L",$\overline{PWDA}$="H"		1.4	2.1	mA
Power down (Note 9)	$\overline{PWAD}$="L",$\overline{PWDA}$="L"		10	50	uA
Power consumption					
AD+DA	$\overline{PWAD}$="H",$\overline{PWDA}$="H"		33.3	50.0	mW
AD	$\overline{PWAD}$="H",$\overline{PWDA}$="L"		16.5	24.8	mW
DA	$\overline{PWAD}$="L",$\overline{PWDA}$="H"		19.8	29.8	mW
Power down (Note 9)	$\overline{PWAD}$="L",$\overline{PWDA}$="L"		75	375	uW

Notes: 4 . The offset of ADC is removed by internal HPF.
5 . These value are analog characteristics at VA=VD=VB=VRAD=VRDA=3.0V.
Then power supply current is VA+VB=10.5mA(typ.), VD=3.2mA(typ.).
6 . Input/Output of ADC and DAC scales with VA voltage to connect VRAD and VRDA pins.
ADC: 0.6 x VA(typ), DAC: 0.6 x VA(typ)
7 . PSR is applied to VA, VD with 1kHz, 50mV. VRAD, VRDA pins are held constant voltage.
8 . Measured by AD725C (SHIBASOKU). RMS mode.
9 . In case of power-down mode, all digital input pins including clocks pins(MCLK, SCLK, LRCK) are held VD or DGND.

FILTER CHARACTERISTICS

(Ta=25°C; VA,VD=2.4~4.0V; fs=44.1kHz; DEM0="1", DEM1="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 10)	±0.1dB	PB	0		19.0	kHz
	-0.55dB			20.0		kHz
	-3.0dB			22.1		kHz
Stopband		SB	30.1			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	70			dB
Group Delay (Note 11)		GD		9		1/fs
Group Delay Distortion		ΔGD			0	us
ADC Digital Filter(HPF):						
Frequency Response	-3dB	FR		3.4		kHz
(Note 10)	-0.5dB			10		kHz
	-0.1dB			22		kHz
DAC Digital Filter:						
Passband (Note 10)	±0.1dB	PB	0		20.0	kHz
	-6.0dB			22.05		kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 11)		GD		14.8		1/fs
DAC Digital Filter+Analog Filter:						
Frequency Response 0~20.0kHz		FR		±0.5		dB

Notes: 10 . The passband and stopband frequencies scale with fs.
For examples, 20.0kHz at ADC:-0.55dB, DAC:-0.1dB is 0.454 x fs.

11 . The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 20bit data of both channels to the output register for ADC. For DAC, this time is from setting the 20bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VA,VD=2.4~4.0V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-20uA)	VOH	VD-0.1	-	-	V
Low-Level Output Voltage (Iout=20uA)	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	±10	uA

SWITCHING CHARACTERISTICS

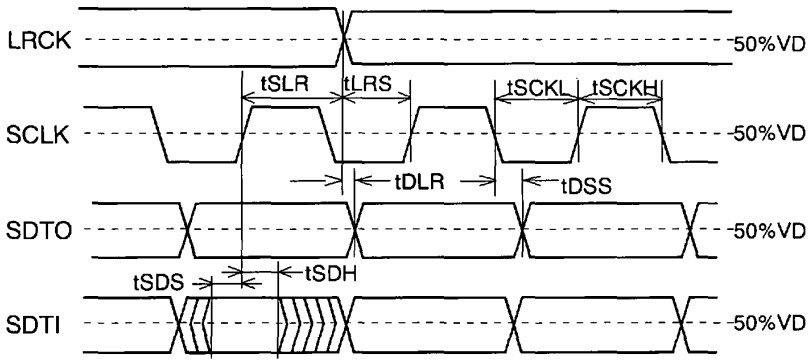
(Ta=25°C; VA,VD=2.4~4.0V; C_L=20pF)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing 256fs:	fCLK	2.048	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	3.072	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
512fs:	fCLK	4.096	22.5792	25.6	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
LRCK Frequency	fs	8	44.1	50	kHz
Duty Cycle		45		55	%
Serial Interface Timing					
SCLK Period	tSCK	312.5			ns
SCLK Pulse Width Low	tSCKL	130			ns
Pulse Width High	tSCKH	130			ns
LRCK Edge to SCLK "↑" (Note 12)	tLRS	50			ns
SCLK "↑" to LRCK Edge (Note 12)	tSLR	50			ns
LRCK to SDTO(MSB)	tDLR			80	ns
SCLK "↓" to SDTO	tDSS			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
Reset Timing					
$\overline{\text{PWAD}}$ or $\overline{\text{PWDA}}$ Pulse Width	tPW	150			ns
$\overline{\text{PWAD}}$ "↑" to SDTO valid (Note 13)	tPWV		8224		1/fs

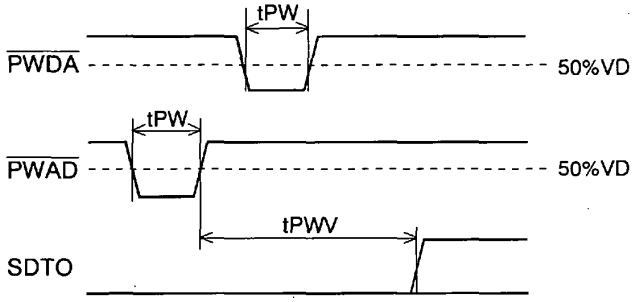
Notes: 12 . SCLK rising edge must not occur at the same time as LRCK edge.

13 . These cycles are the number of LRCK rising from $\overline{\text{PWAD}}$ rising.

■ **Timing Diagram**



Serial Interface Timing



Reset & Initialize Timing

OPERATION OVERVIEW

■ System Clock Input

The AK4519 with CMODE is used to select either MCLK=256fs or 384fs or 512fs. The relationship between the external clock applied to the MCLK input and the desired sample rate is defined in Table 1 . The LRCK clock input must be synchronized with MCLK, however the phase is not critical.
When CMODE is "H", the MCLK can be input 384fs or 512fs. The internal master clock is divided into 2/3 automatically. *fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, AK4519 may occur click noise. ADC dose not have a limit on a change timing, however, as ADC output may not meet 20bit serial data of changing in front and behind, output data should make "0" data by force from the outside. Click noise occurs when DAC is input except "0" data.

All external clocks(MCLK, SCLK, LRCK) must be present unless $\overline{\text{PWDA}}$ and $\overline{\text{PWAD}}$ ="L". If these clocks are not provided, the AK4519 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally.

fs	MCLK			SCLK
	CMODE="L"	CMODE="H"		64fs
	256fs	384fs	512fs	
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	2.048MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	2.822MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	3.072MHz

Table 1 . System Clock example

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using SCLK and LRCK inputs. The data is MSB fist, 2's compliment. The ADC is 20bit MSB justified and the DAC is 20bit, LSB justified.

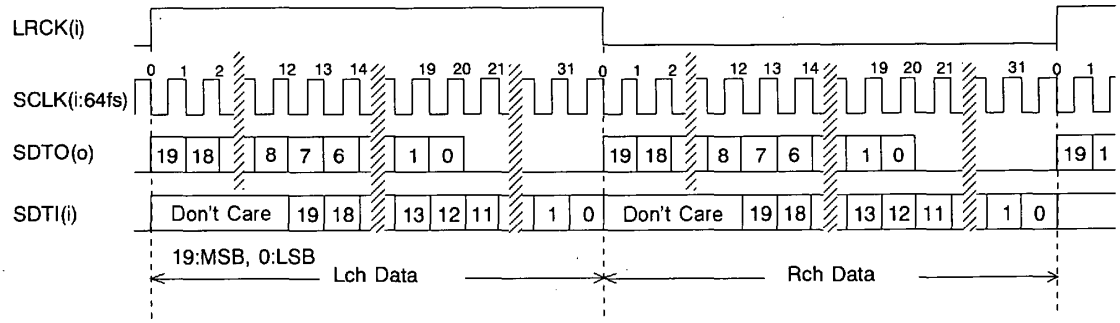


Figure 1 . Audio Interface Timing

■ **De-emphasis filter**

The DAC of AK4519 includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three frequencies(32kHz, 44.1kHz, 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 2 . De-emphasis filter control

■ **Digital High Pass Filter**

The AK4519 has a Digital High Pass Filter(HPF) for DC-offset cancel. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz and the frequency response at 20Hz is -0.12dB. It also scales with the sampling frequency(fs).

■ **Power down & Reset**

The ADC and DAC of AK4519 are placed in the power-down mode by bringing each power down pin, $\overline{\text{PWAD}}$ $\overline{\text{PWDA}}$ "L" independently and each digital filter is also reset at the same time. This reset should always be done after power-up. In case of the ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 8224 cycles of LRCK clock. This initialization cycle does not affect the DAC operation.

Figure 2 shows the power-up sequence when the ADC is powered up before the DAC power-up.

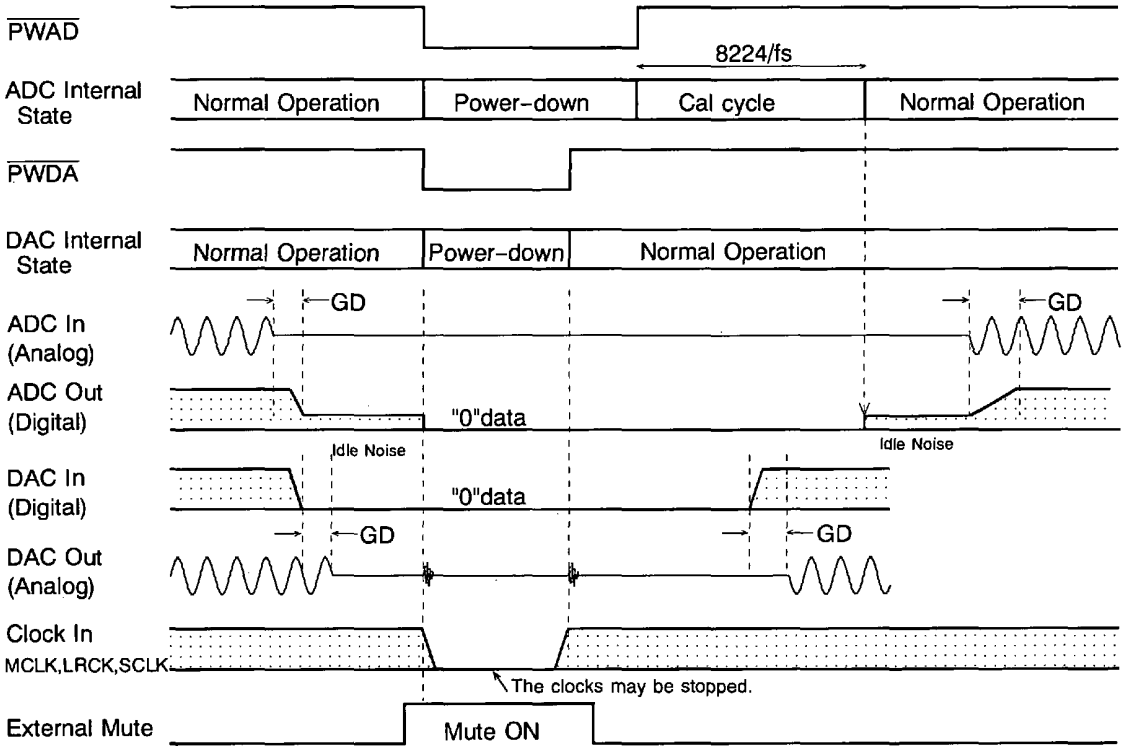


Figure 2 . Power-up sequence

SYSTEM DESIGN

Figure 3 shows the system connection diagram. An evaluation board[AKD4519] is available which demonstrates application circuits, optimum layout, power supply arrangements and measurement results.

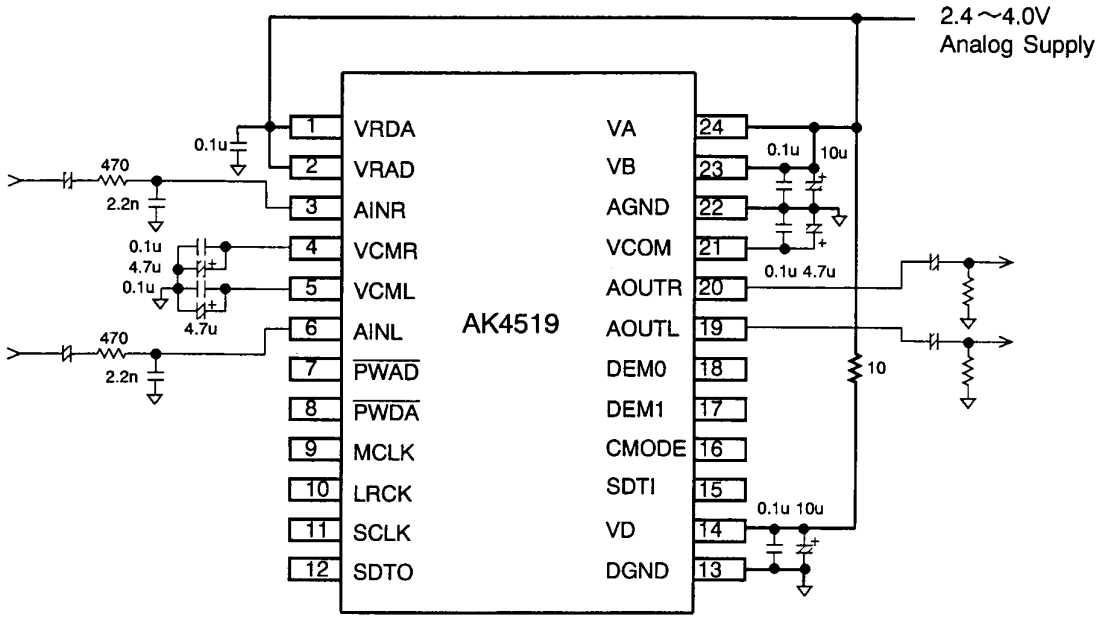


Figure 3 . System Connection Diagram Example

NOTE:

- LRCK=fs, SCLK≥40fs, MCLK=256fs at CMODE="L",
  MCLK=384fs or 512fs at CMODE="H".
- Power supply lines of VA and VD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- Electrolystic capacitor value of VCOM depends on low frequency noise of supply voltage.

1. Grounding and Power Supply Decoupling

The AK4519 requires careful attention to power supply and grounding arrangements. The VA and VB are connected together through the chip substrate and have several ohm resistance. When VD and VA are supplied separately, VA and VB should not be the higher voltage than VD. And VA and VB should be powered at the same time or earlier than VD. If so not, VA is supplied from analog supply in system and VD is supplied from VA via 10 ohms resistor. (refer to Figure 3)
System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4519 as possible, with the small value ceramic capacitor being nearest.

2. Voltage reference

The differential voltage between VRAD and VRDA sets the analog input/output range. VRAD and VRDA pins are normally connected to VA with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolystic less than 4.7uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from the VRAD, VRDA, VCOM pins in order to avoid unwanted coupling into the AK4519.

3. Analog Inputs

ADC inputs are single-ended and internally biased to VCML & VCMR with 50kΩ (typ). The input signal range scales with the supply voltage and nominally 0.6 x VA Vpp(typ). The ADC output data format 2's compliment. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative full scale. The ideal code is 00000H(@20bit) with no input signal.

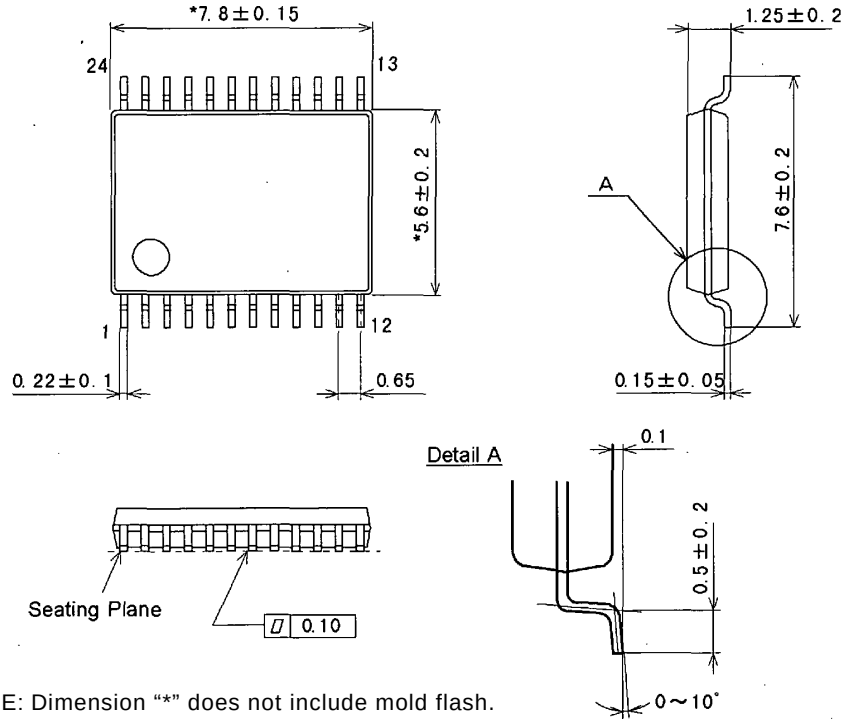
The AK4519 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter(fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VA Vpp(typ). The DAC input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required.

PACKAGE

● 24pin VSOP (Unit: mm)

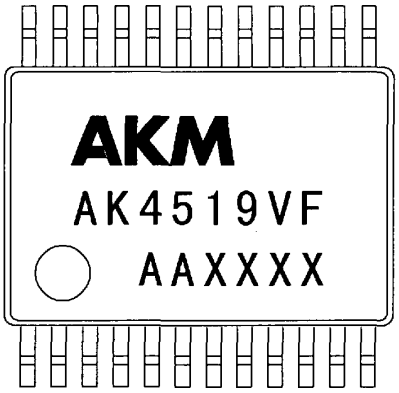


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plane

MARKING



Consist of AAXXXX

AA: Lot number

XXXX: Assembly date

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