AK4540

AC'97™ Multimedia Audio CODEC

Features:

- **Compliant with AC'97 Requirements**
  - **4 Stereo Inputs: LINE, CD, VIDEO, AUX**
  - **Speakerphone and PC BEEP Inputs**
  - **2 Independent MIC Inputs**
  - **Stereo LINE Output Mono Output**
- **20dB MIC Amplifier**
- **Analog Characteristics (S/N "A" weighted)**
  - **A/D 92dBA**
  - **D/A 90dBA**
  - **D/A+Mixer 88dBA**
  - **A-A 94dBA**
- **Programmable Power Down Modes**
- **Low Power Consumption**
  - **225mW**
- **Power Supplies**
  - **Analog : 5.0V, Digital : 5.0V**

General Description

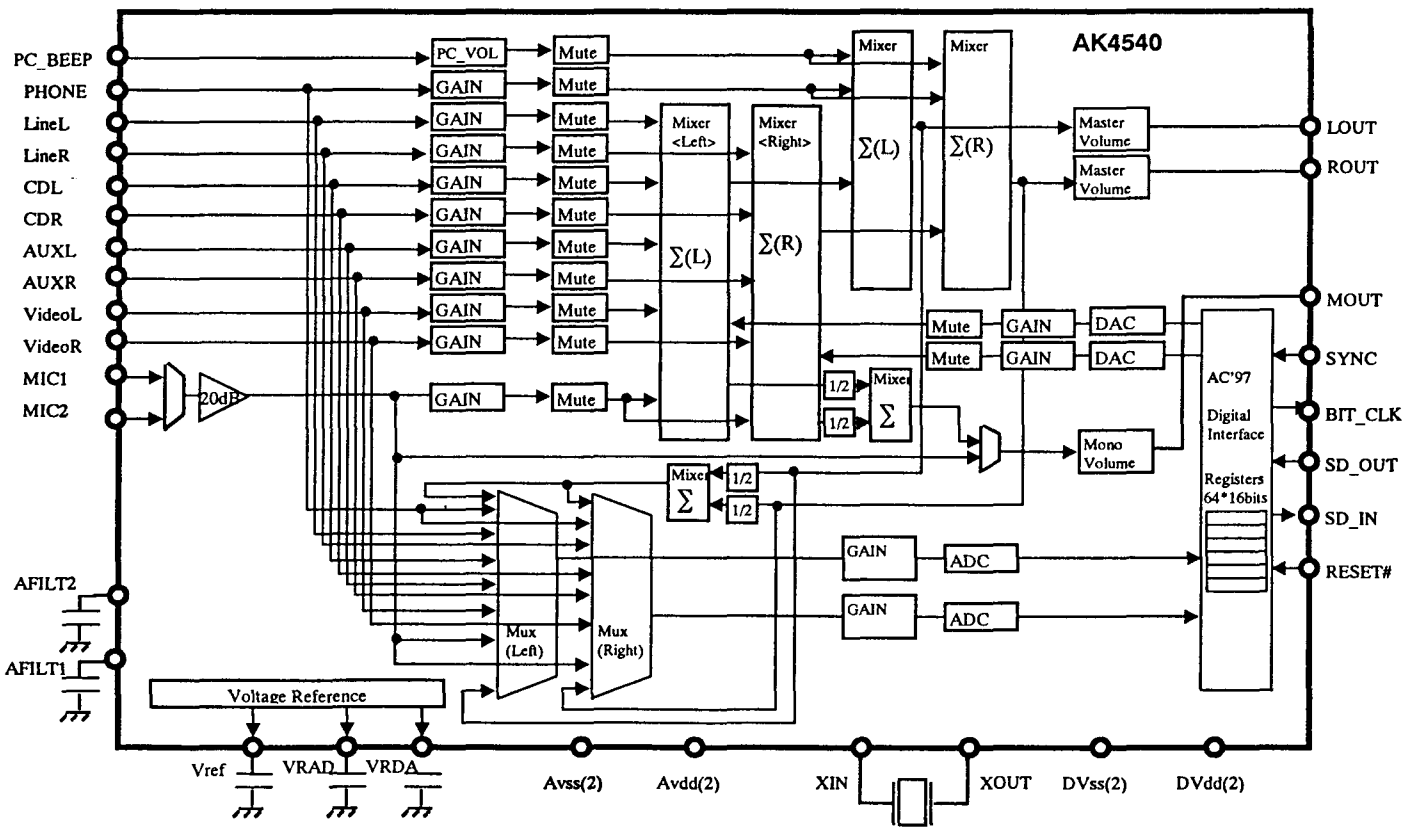
The AK4540 is multimedia codec to be compliant with Audio Codec '97 specification. The AK4540 can interface with various digital controllers which have AC-link interface.

The AK4540 operates at a fixed 48kHz sampling rate.

As the audio function is compose of the codec and digital controller , it is easy to enhance several audio functions such as 3D audio, modem, MPEG, etc.

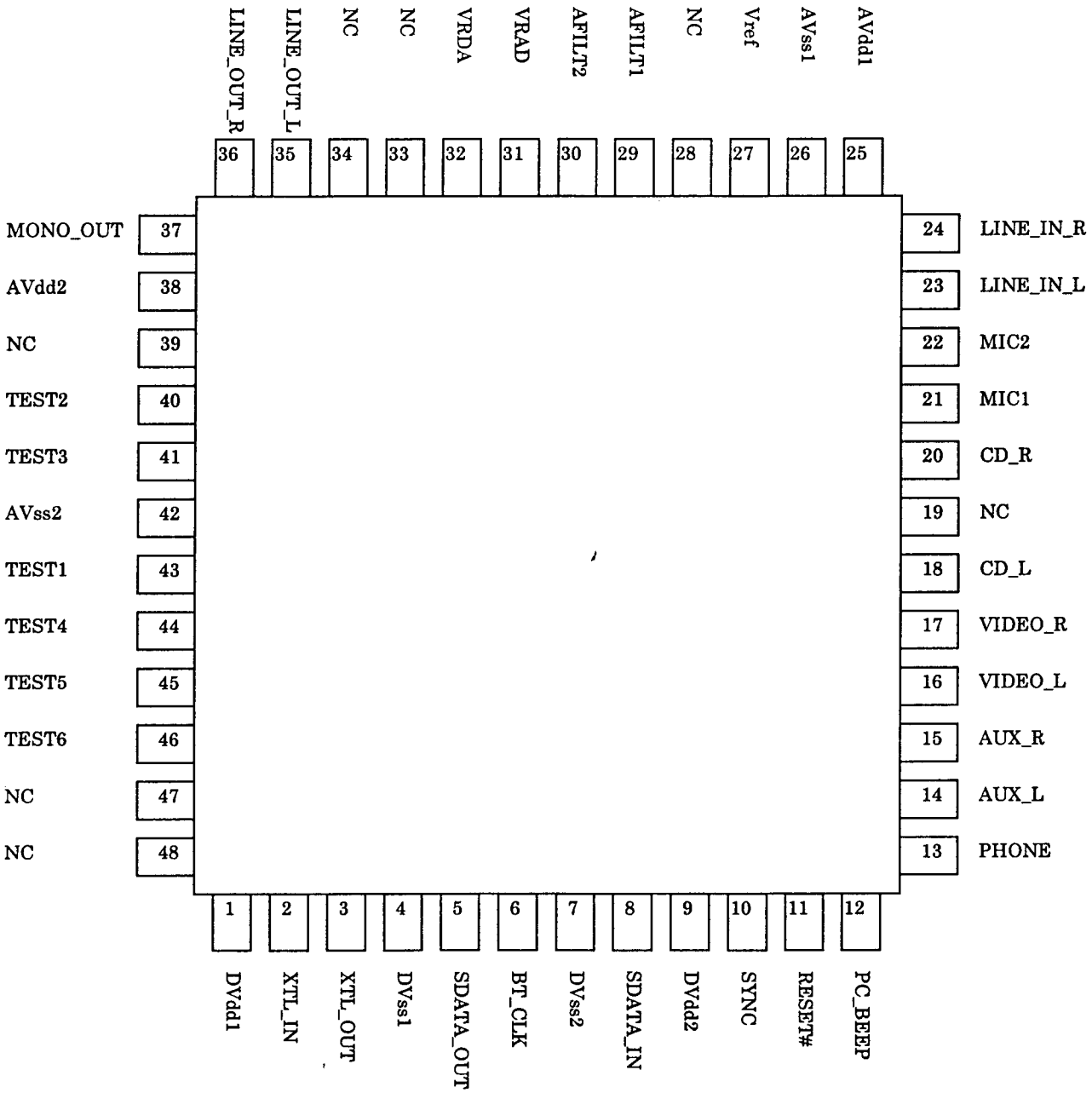
Not only the AK4540 can control power down modes precisely but also low power consumption itself, the AK4540 is suitable for both desktop PC and mobile PC.

AK4540 Block Diagram



* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

■Pin Layout


LINE_OUT_R 36
LINE_OUT_L 35
NC 34
NC 33
VRDA 32
VRAD 31
AFILT2 30
AFILT1 29
NC 28
Vref 27
AVss1 26
AVdd1 25
MONO_OUT 37
AVdd2 38
NC 39
TEST2 40
TEST3 41
AVss2 42
TEST1 43
TEST4 44
TEST5 45
TEST6 46
NC 47
NC 48
24 LINE_IN_R
23 LINE_IN_L
22 MIC2
21 MIC1
20 CD_R
19 NC
18 CD_L
17 VIDEO_R
16 VIDEO_L
15 AUX_R
14 AUX_L
13 PHONE
1 DVdd1
2 XTL_IN
3 XTL_OUT
4 DVss1
5 SDATA_OUT
6 BT_CLK
7 DVss2
8 SDATA_IN
9 DVdd2
10 SYNC
11 RESET#
12 PC_BEEP

Pin/Function

No.	Signal Name	I/O	Description
1	DVdd1	-	Digital power supply, 5V
2	XTL_IN	I	24.576MHz Crystal
3	XTL_OUT	O	24.576MHz Crystal If external clock is used, this pin should be open.
4	DVss1	-	Digital Ground
5	SDATA_OUT	I	Serial, time division multiplexed, AC97 input stream
6	BIT_CLK	O	12.288MHz serial data clock
7	DVss2	-	Digital Ground
8	SDATA_IN	O	Serial, time division multiplexed, AC97 output stream
9	DVdd2	-	Digital power supply, 5V
10	SYNC	I	48kHz fixed rate sampling rate
11	RESET#	I	AC'97 Master Hardware Reset
12	PC_BEEP	I	PC Speaker beep pass through
13	PHONE	I	From telephony subsystem speakerphone
14	AUX_L	I	Aux Left Channel
15	AUX_R	I	Aux Right Channel
16	VIDEO_L	I	Video Audio Left Channel
17	VIDEO_R	I	Video Audio Right Channel
18	CD_L	I	CD Audio Left Channel
19	NC	-	No Connection
20	CD_R	I	CD Audio Right Channel
21	MIC1	I	Desktop Microphone Input
22	MIC2	I	Second Microphone Input
23	LINE_IN_L	I	Line In Left Channel
24	LINE_IN_R	I	Line In Right Channel
25	AVdd1	-	Analog power supply, 5V
26	AVss1	-	Analog Ground
27	Vref	O	Reference Voltage : 0.1μF+ 4.7μF
28	NC	-	No Connection
29	AFILT1	O	Anti-Aliasing Fileter Cap
30	AFILT2	O	Anti-Aliasing Fileter Cap
31	VRAD	O	Vref for ADC: 0.1μF+ 4.7μF
32	VRDA	O	Vref for DAC: 0.1μF+ 4.7μF
33	NC	-	No Connection
34	NC	-	No Connection
35	LINE_OUT_L	O	Line Out Left Channel
36	LINE_OUT_R	O	Line Out Right Channel
37	MONO_OUT	O	To telephony subsystem speakerphone
38	AVdd2	-	Analog power supply, 5V
39	NC	-	No Connection
40	TEST2	-	Test input pin (This pin should be open for normal operation)
41	TEST3	-	Test input pin (This pin should be open for normal operation)
42	AVss2	-	Analog Ground
43	TEST1	-	Test output pin (This pin should be open for normal operation)
44	TEST4	-	Test input pin (This pin should be open for normal operation)
45	TEST5	-	Test input pin (This pin should be open for normal operation)
46	TEST6	-	Test input pin (This pin should be open for normal operation)
47	NC	-	No Connection
48	NC	-	No Connection

Absolute Maximum Rating

AGND, DGND=0V

Parameter		Symbol	min	max	Units
Power Supplies					
	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0(VA+0.3)	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage	Note2)	VINA	-0.3	6.0(VA+0.3)	V
Digital Input Voltage	Note2)	VIND	-0.3	6.0(VA+0.3)	V
Ambient Temperature		Ta	-10	70	°C

Note 1. All voltages with respect to ground
2. Max value is higher voltage of 6.0V or VA+0.3V
3. Digital supplies means DVDD1 and DVDD2, and they are connected to each other in the chip. AVDD2 is connected to AVDD through the substrate internally.

Warning: Operation at or beyond these limits may results in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Condition

AGND, DGND=0V

Parameter		Symbol	min	typ	max	Units
Power Supplies	AK4540	VA				
	Analog		4.75	5.0	5.25	V
	Digital		4.75	5.0	VA	V

All voltages with respect to ground.

AK4540 Analog Characteristics

Ta=25°C,AVdd=DVdd=5.0V, fs=48KHz, Signal Frequency =1kHz
All volume setting for ADC/DAC performance measurement is 0dB.

Parameter	min	typ	max	Units
Audio-ADC				
Resolution			16	Bits
S/N (A weight)	80	92		dB
S/(N+D) (-0.5dB analog input)	70	80		dB
Inter Channel Isolation	70	83		dB
Inter Channel Gain Mismatch			0.5	dB
Full Scale Input Voltage	0.88	1.0	1.12	Vrms
Power Supply Rejection		50		dB
Audio DAC: measured at AOUTL/AOUTR via MIXER path				
Resolution			16	Bits
S/N (A weighted) : mixer+DAC measured at AOUT : DAC only	 82	 88 90		 dB dB
S/(N+D)	70	85		dB
Inter Channel Isolation	70	95		dB
Inter Channel Gain Mismatch			0.5	dB
Full Scale Output Voltage	0.88	1.0	1.12	Vrms
Total Out-of-Band Noise (28.8kHz - 100kHz)		-60		dB
Power Supply Rejection		50		dB
MIC Amplifier / MUX				
Gain : 20dB is selected	18	20	22	dB
Master volume (Mono, Stereo) : 1.5dB x 32 step				
Step Size		1.5		dB
Attenuation Control Range	0		46.5	dB
PC Beep : 3dB x 16 step				
Step Size		3.0		dB
Attenuation Control Range	0		45	dB
Analog Mixer : 1.5dB x 32 step				
Step Size		1.5		dB
Gain Control Range	-34.5		+12	dB
Record Gain : 1.5dB x 16 step				
Step Size		1.5		dB
Gain Control Range	0		+22.5	dB
Mixer				
Input Voltage (except for MIC)		1.0		Vrms
Input Voltage MIC : Gain = 0dB MIC : Gain = 20dB		1 0.1		Vrms Vrms
S/N(A weighed) : 0dB setting, 1 path is selected at Mixer CD to AOUT: Other analog input to AOUT	 85	 94 94		 dB dB
Input Impedance (Input gain=0dB, record MIXER=off) PC_BEEP only Others(PHONE, LINE, CD, AUX, VIDEO) Input Impedacnce (MIC1 and MIC2)	 10 10 10	 100 50 30		 kΩ kΩ kΩ
Power Supplies				
Power Supply Current VA VD(@CL=50pF) a) Crystal Oscillation b) External Clock		 32 13 13	 48 21 21	 mA mA mA
Powerdown Mode VA VD(@CL=50pF, RESET#=0, Crystal Oscillation)		 0 3	 100 10	 μA mA

Filter Characteristics

Ta=25°C,AVdd,DVdd=5V , fs=48KHz(fixed)

Parameter	min	typ	max	Units
ADC Digital Filter				
Passband (±0.2dB) Note)	20		19.2	kHz
Stopband	28.8			kHz
Stopband Attenuation	70			dB
Group Delay			0.5	ms
DAC Digital Filter				
Passband (±0.2dB)	20		19.2	kHz
Stopband	28.8			kHz
Group Delay			0.5	ms
Stopband Rejection	70			dB
DAC Post filter				
Passband Frequency Response (0 - 19.2kHz)		±0.1		dB

Note) This frequency scales with the sampling frequency (fs).

AK4540 DC Characteristics

Ta=25°C,AVdd=DVdd=5V±5%, 50pF external load

Parameter	Symbol	min	typ	max	Units
"H" level input voltage	VIH		-	-	
XTAL_IN		0.7xDVDD			V
All pins except for XTAL_IN pin		2.2			V
"L" level input voltage	VIL	-	-		
XTAL_IN				0.3xDVDD	V
All pins except for XTAL_IN pin				0.8	V
"H" level output voltage Iout=-5mA	VOH	2.6	-	-	V
"L" level output voltage Iout= 5mA	VOL	-	-	0.55	V
Input leakage current	Iin	-	-	±10	μA

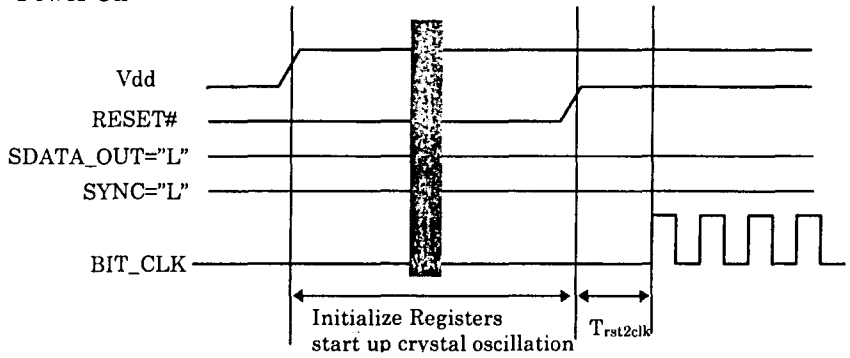
Switching Characteristics

Ta=25°C,AVdd=DVdd=5V, 50pF external load

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency Note)		-	24.576	-	MHz
AC link Interface Timing					
BIT_CLK frequency	Fbclk		12.288		MHz
BIT_CLK clock Period	Tbclk	-	81.38	750	ns
BIT_BLK low pulse width	Tclk_low	32.56	40.7	48.84	ns
BIT_BLK low pulse width	Tclk_high	32.56	40.7	48.84	ns
BIT_CLK rise time	Trise_clk	-		6	ns
BIT_CLK fall time	Tfall_clk	-	-	6	ns
			-		
SYNC frequency		-	48	-	kHz
SYNC low pulse width	Tsync_low	-	19.5	-	μs
SYNC high pulse width	Tsync_high	-	1.3	-	μs
SYNC rise time	Trise_sync	-	-	6	ns
SYNC fall time	Tfall_sync	-	-	6	ns
Setup time(SDATA_IN,SDATA_OUT)	Tsetup	15.0	-	-	ns
Hold time(SDATA_IN,SDATA_OUT)	Thold	25.0	-	-	ns
SDATA_IN rise time	Trise_din	-	-	6	ns
SDATA_IN fall time	Tfall_din	-	-	6	ns
SDATA_OUT rise time	Trise_dout	-	-	6	ns
SDATA_OUT fall time	Tfall_dout	-	-	6	ns
Cold Rest (SDATA_OUT=L, SYNC=L)					
RESET# active low pulse width	Trst_low	1.0	-	-	μs
RESET# inactive to BIT_CLK delay	Trst2clk	162.8			ns
Warm Rest Timing					
SYNC active low pulse width	Tsync_high		1.3	-	μs
SYNC inactive to BIT_CLK delay	Tsync2clk	162.8			ns
AC-link Low Power Mode Timing					
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdwn	-	-	1.0	μs
Activate Test Mode Timing					
Setup to trailing edge of RESET#	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z	Toff	-	-	50	ns
Falling edge of RESET# to "L"	Tlow			50	ns

Note) The use of crystal is recommended. If an external oscillator is used, it is input to XTAL_IN and XTAL_OUT should be open..

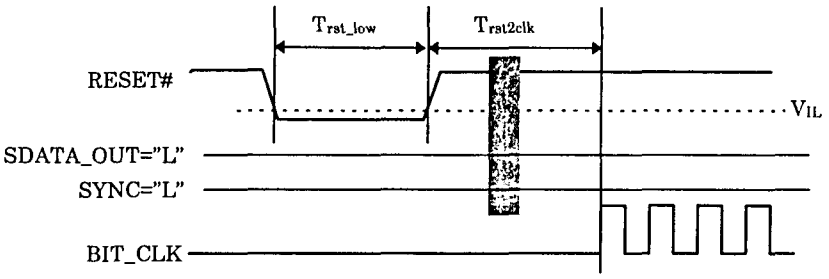
■ Power On



■Cold Reset Timing

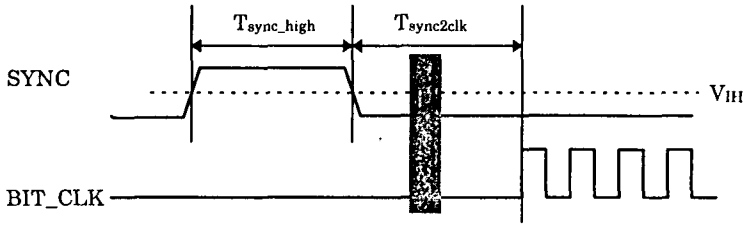
Note that both SDATA_OUT and SYNC must be low at the rising edge of RESET# in the "cold reset".
The AK4540 initializes all registers and each analog output is in Hi-Z state while RESET pin is low.
At the rising edge of RESET, the AK4540 initiates the initialization of analog circuit. The AK4540 can output A/D data after 516fs cycles later, and D/A data after 2fs cycles later from the end of initialization process.

Status bit in the slot 0 is "0" (not ready) when the AK4540 is in RESET period ("L") or in initialization process. After initialization cycles, the status bit goes to "1" (ready).

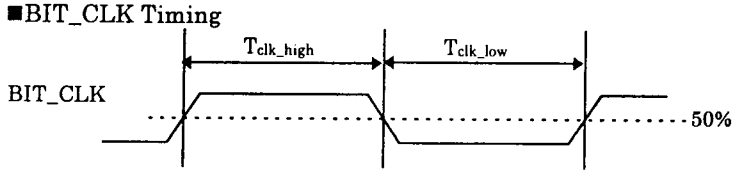


■Warm Reset

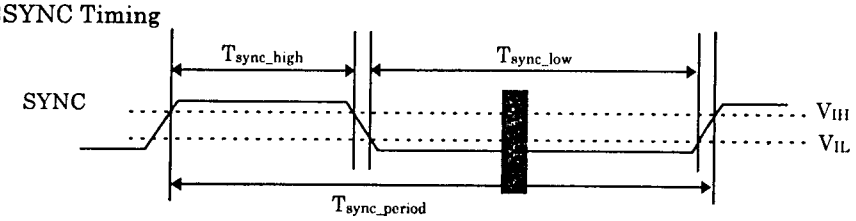
The AK4540 initiates Warm Reset process by receiving pulse on the sync line. The AK4540 clears PR4 bit in the Powerdown Control Register. Note that SYNC signal should synchronize with BIT_CLK after AK4540 starts to output BIT_CLK clock.



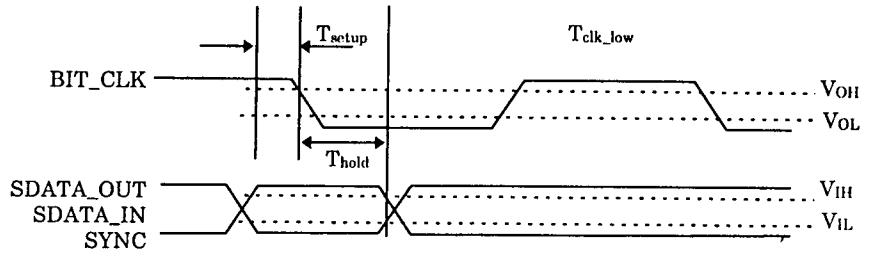
■BIT_CLK Timing



■SYNC Timing

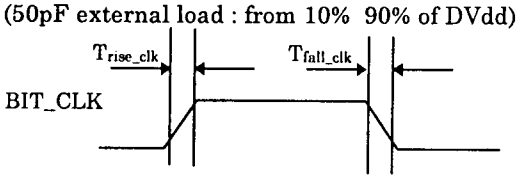


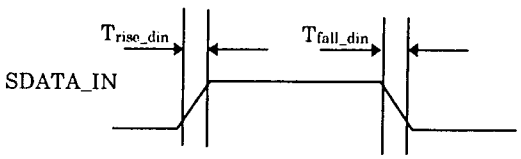
■Setup and Hold Timing

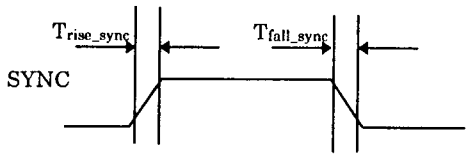


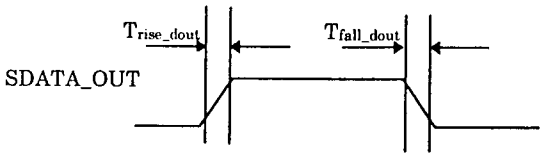
■Signal Rise and Fall Times

(50pF external load : from 10% 90% of DVdd)

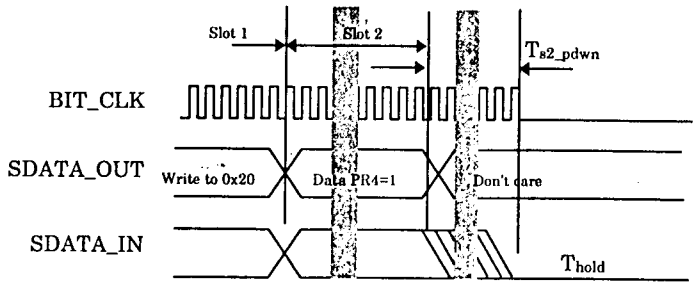




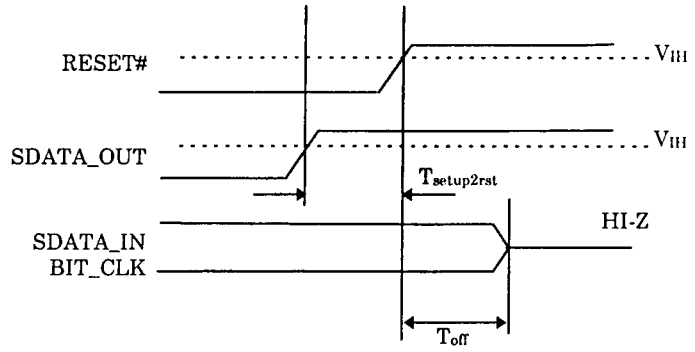




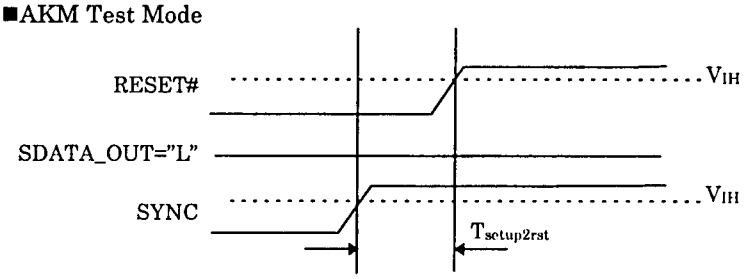
■AC-link Low Power Mode Timing



■Activate Test Mode



■AKM Test Mode



Notes:[1]

1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the rising edge of RESET# causes the AK4540 AC-link outputs to go high impedance which is suitable for ATE in circuit testing. Note that the AK4540 enters in the ATE test mode regardless SYNC is high or low.

2. Bringing both SYNC high and SDATA_OUT low for the rising edge of RESET# causes AKM test mode.

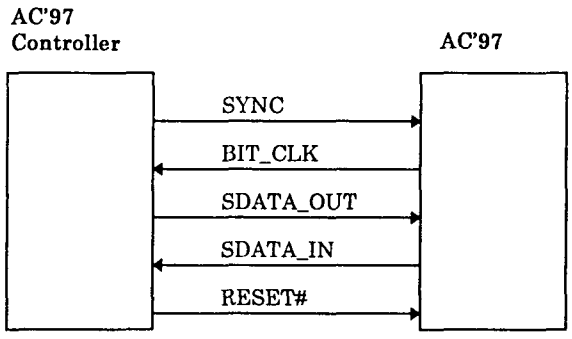
3. Once test modes have been entered, the only way to return to the normal operating state is to issue "cold reset" which issues RESET# with both SYNC and SDATA_OUT low.

[1] All the following sentences written with small italic font in this document quote the AC'97 component specification.

General Description

■AC '97 Connection to the Digital AC '97 controller

[2]AC '97 communicates with its companion AC '97 controller via a digital serial link, AC-link". All digital audio streams, and command/status information are communicated over this point to point serial interconnect. A breakout of the signals connecting the two is shown in the following figure.



■Digital Interface

The AK4540 incorporates a 5 pin digital serial interface that links it to the AC '97 controller. AC-link is a bi-directional, fixed rate(48kHz), serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. DAC and ADC resolution of the AK4540 is 16 bit resolution. The data streams currently defined by the AC '97 specification include:

- ***PCM Playback*** ***2 output slots***

2 channel composite PCM output stream

- ***PCM Record data*** ***2 input slots***

2 channel composite PCM input stream

- ***Control*** ***2 output slot***

Control register write port

- ***Status*** ***2 input slots***

Control register read port

SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, the AK4540 for outgoing data and AC '97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

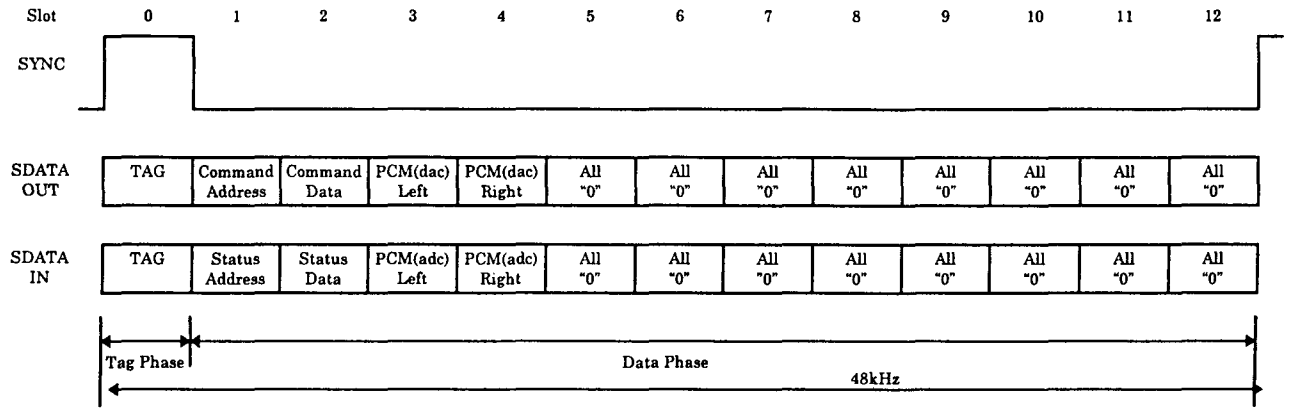
The AC-link protocol provides for a special 16-bit slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "Tagged" invalid, it is the responsibility of the source of the data, (The AK4540 for the input stream, AC '97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Note that SDATA_OUT and SDATA_IN data is delayed one BIT_CLK because AC'97 controller causes SYNC signal high at a rising edge of BIT_CLK which initiates a frame.

"Output" stream means the direction from AC'97 controller to the AK4540, and "Input" stream means the direction from the AK4540 to AC'97 controller

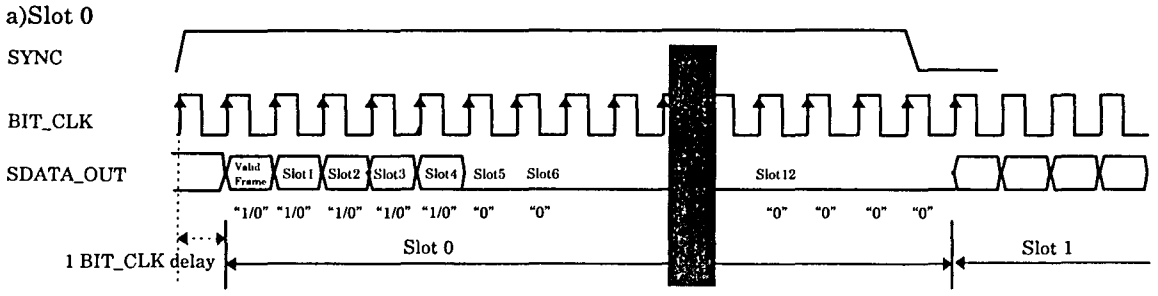
[2]All the following sentences written with small italic font in this document quote the AC'97 component specification.



There are 13 slots in one frame. The frequency of the frame (sync) is fixed to 48kHz. Only Slot 0, which is Tag phase, is 16bits, and other slots are 20bits.

AC-link Audio Output Frame (SDATA_OUT)

a)Slot 0



First the AK4540 checks the Valid Frame bit first. Note that when valid frame bit is "1", at least one of slot 1,slot 2,slot3,and slot 4 are valid, other slots (5- 12 slots) are ignored.
If the bit is "0", the AK4540 ignores the following all other TAG bits and each slots.
Next, the AK4540 checks the validity of each slot in the TAG phase (slot 0).
If each bit regarding to slots is "0", then the AK4540 ignores the slot regarding to the bit.
If "1", the slot is valid.
All bit in slot 5-12 is "0".

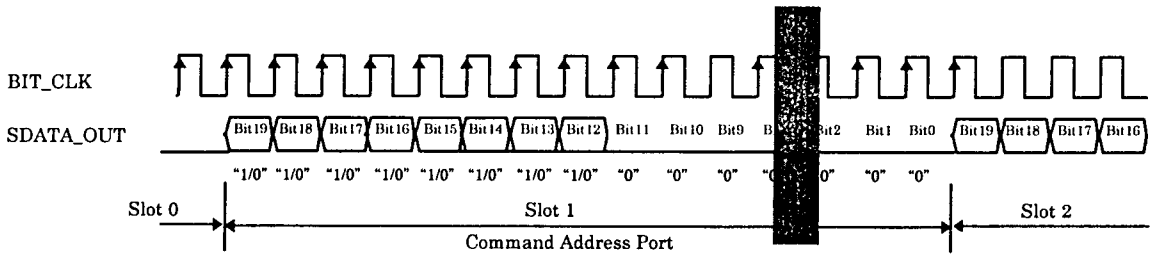
A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4540 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AK4540 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Data is output from the AC'97 controller with MSB first through SDATA_OUT pin

Valid frame bit in the slot 1 is 1 if at least 1 slot is valid ("1"). If all of slot1, slot2, slot 3, and slot4 are invalid, valid frame bit should be "0". The following table shows the relationship of valid bits and the Read/Write operation.

Slot 1 Valid Bit (Command Address)	Slot 3 Valid Bit (Command Data)	Read/Write Operation
1	1	Read/Write (Normal Operation)
0	1	Ignore
1	0	Read: Normal Operation, Write: Ignore
0	0	Ignore

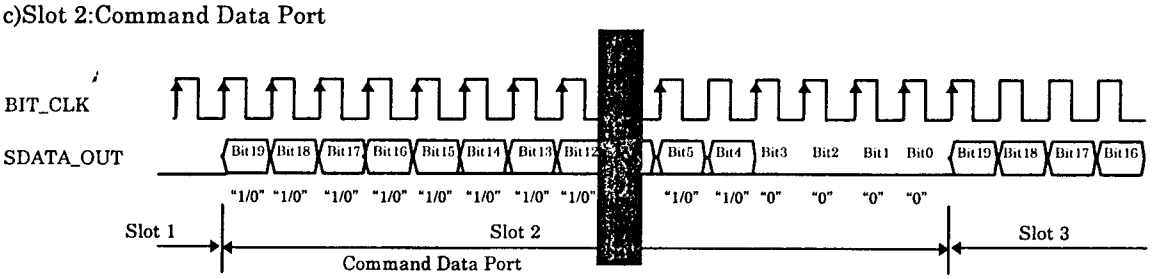
b)Slot 1:Command Address Port
This slot shows the address of command data, which is showed in the slot 2. The AK4540 has 17 16-bit valid registers, addressable on even byte boundaries. Only the even registers are valid, the access to odd register is invalid and ignored by the AK4540.



Bit 19: Read/Write command 1=read, 0=write
Bit 18:12 Control Register Index (see "Mixer Registers for the detail)
Bit 11:0 Reserved ("0")

Bit 18 is equivalent to the most significant bit of the index address data.
The AK4540 ignore the bits which are from bit 11 to bit 0.

c)Slot 2:Command Data Port



Bit19:4 Control Register Write Data (if bit 19 of slot 1 is "1", all Bit19:4 should be "0")
Bit3:0 Reserved("0")

If the bit 19 in the slot 1 is "0", AC'97 controller must output Command Data Port data to the slot 2 ***in the same frame***. If the bit 19 in the slot 1 is "1", the AK4540 discard Command Data Port data.

Bit 19 is equivalent to D15 bit of mixer register value.

d)Slot 3 PCM Playback Left Channel (16bits)
Playback(DAC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4540 is 16bit, lower 4 bits are ignored. AC'97 controller should stuff bit3-0 with "0". If valid bit (slot 3) in the slot 0 is invalid ("0"), the AK4540 interprets the data as all "0".
Bit19:4 Playback data
Bit 3:0 "0"

e)Slot 4 PCM Playback Right Channel (16bits)
Playback data format is MSB first. Data format is 2's complement. As the resolution of the AK4540 is 16bit, lower 4 bits are ignored. AC'97 controller should stuff bit3-0 with "0". If valid bit (slot 4) in the slot 0 is invalid ("0"), the AK4540 interprets the data as all "0".
Bit19:4 Playback data
Bit 3:0 "0"

f)Slot6-12 Reserved
The AK4540 ignores these slots. All bits should be stuffed with "0" by the AC'97 controller.

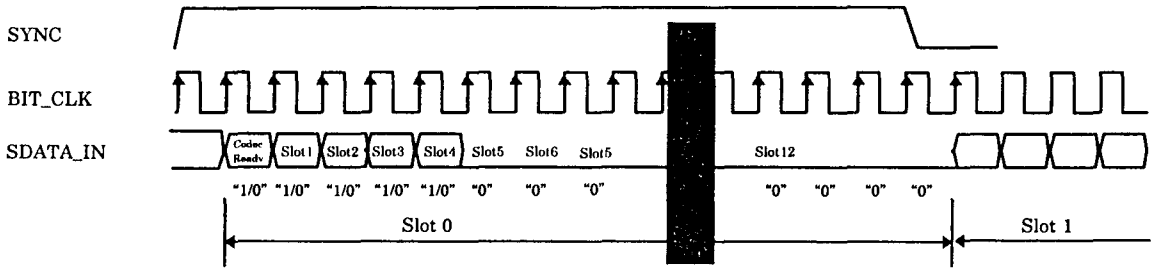
AC-link Input Frame(SDATA_IN)

Each AC-link frame consists of 12 20-bit slots and 1 16-bit special tag phase.

a)Slot 0

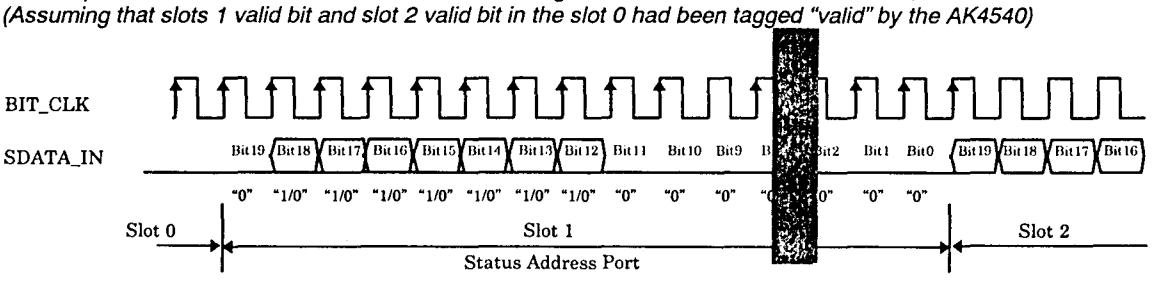
Slot 0 is a special time frame, and consists of 16 bit. Slot 0 is also named as Tag phase. If the first bit in the slot 1 is valid, the AK4540 is ready for normal operation. [3]If the "Codec Ready" bit is invalid, the following bits and remaining slots are all "0". AC'97 controller should ignore the following bits in the slot 0 and all other slots. If the bit is "1", the next 12 bits corresponding 12 slots are valid.

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4540 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AK4540 transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.



b)Slot 1 Status Address Port

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 valid bit and slot 2 valid bit in the slot 0 had been tagged "valid" by the AK4540)



This address shows register index for which data is being returned in the slot 2.
This address port is the copy of slot 1of output frame, and index address input to SDATA_OUT is loop backed to AC'97 controller through SDATA_IN.

b)Slot 2: Status Data Port

Status data addressed by command address port of Output Stream is output through SDATA_IN pin.
If slot 2 bit in the Tag Phase is invalid, all bits are stuffed with "0".

Bit19:4 Control Register Read Data (the contents of indexed address in the slot 1)
Bit3:0 "0"

Note that the address of Status Data Port data are consistent with Status Address Port data of the slot 1 ***in the same frame***. If the read operation is issued in the frame N by AC'97 controller, Status Data Port data is output through SDATA_IN in the frame N+1. **Note that data is output in only this frame, only one time and that the following frames are invalid if the next read operation is not issued.**

c)Slot 3 PCM Record Left Channel

Record(ADC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4540 is 16bit, lower 4 bits are ignored. If ADC block is powered down, slot-3 valid bit bit in the slot 0 is invalid ("0"), and data is output as all "0".

AC'97 Bit19:4 Audio ADC left channel output
Bit3:0 "0"

[3] When the AC'97 is not ready for normal operation, output bits are not specified in the documents.

d)Slot 4 PCM Record Right Channel
Record(ADC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4540 is 16bit, lower 4 bits are ignored. If ADC block is powered down, slot-4 valid bit in the slot 0 is invalid ("0"), and data is output as all "0".
Bit19:4 Audio ADC right channel output
Bit3:0 "0"

e)Slot 5 Modem Line Codec
As the AK4540 does not incorporate modem codec, all bits are stuffed with "0".
Bit19:0 "0"

f)Slot 6 Microphone Record Data
As the AK4540 does not incorporate 3rd ADC codec, all bits are stuffed with "0".
Bit19:0 "0"

g)Slot 7-12 Reserved
Bits19:0 "0"

■Mixer Registers

Ecah Register is 16 bit wide. Note that the AK4540 output all "0" if AC'97 controller try to read the value of invalid address.

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	0000h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	X	X	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
26h	Powerdown Ctrl/Stat	X	X	X	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na
7Ch	Vendor ID1	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"1"	"0"	"1"	"0"	"0"	"1"	"0"	"1"	"1"	414Bh
7Eh	Vendor ID2	"0"	"1"	"0"	"0"	"1"	"1"	"0"	"1"	X	X	X	X	X	X	X	X	4D00h

*) Vender ID of AKM is "AKM" :This ID has been approved by Microsoft.
*) The AK4540 outputs "X" bits as "0". Even if "X" bits is "1", the AK4540 ignores these bits.
*) A write to "Invalid" registers does not affect to the operation of the AK4540.
*) Lower 4 bits in 26h register are all "0" just after cold reset. When each portion is ready to normal operation, the coresponding bit becomes "1". Powerdown register is not affected by the write to reset register.
See "Mixer Registers" in AC'97 specification for the detail.

■Reset Register (Index 00h)

<Write>

When any value except for zero (0x0000) is written to the AK4540's RESET register, all registers in the AK4540 except for 26h Powerdown/Control Register are reset to default values. Note that the AK4540 ignores the write of 0x0000 to this register and that the AK4540 do nothing. The value of this register is not altered.

<Read>

All bits of this register are "0".

■ Play Master Volume Registers (Index 02h, 06h)

The following table shows the relationship between bits and the attenuation value. Attenuation step is 1.5dB.
The AK4540 does not support optional MX5 bit. The AK4540 detects when that bit is set and set all 4 LSBs to 1s.
Example: When the driver writes a "1xxxxx" the AK4540 interpret that as "011111". When this register is read, the return value is "01111".

Mute	MX5	MX4	MX3	MX2	MX1	MX0	Att.
0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	1	-1.5dB
0	0	0	0	0	1	0	-3.0dB
0	0	0	0	0	1	1	-4.5dB
0	0	1	1	1	1	0	-45.0dB
0	0	1	1	1	1	1	-46.5dB
0	1	X	X	X	X	X	-46.5dB
1	X	X	X	X	X	X	Mute

■ PC Beep Register (Index 0Ah)

The following table shows the relationship between bits and the attenuation value. Attenuation step is 3dB.
PC_BEEP of the AK4540 is mute off at default state.
The PC Beep is routed to L & R Line outputs after the rising edge of RESET signal.

Mute	PV3	PV2	PV1	PV0	Att.
0	0	0	0	0	0dB
0	0	0	0	1	-3.0dB
0	0	0	1	0	-6.0dB
0	1	1	1	1	-45.0dB
1	X	X	X	X	Mute

■ Analog Mixer Input Gain Registers (Index 0Ch-18h)

The following table shows the relationship between bits and the gain/attenuation value. Attenuation step is 1.5dB.

Mute	Gx4	Gx3	Gx2	Gx1	Gx0	Att.
0	0	0	0	0	0	+12dB
0	0	0	0	0	1	+10.5dB
0	0	1	0	0	0	0dB
0	0	1	0	0	1	-1.5dB
0	1	1	1	1	0	-33.0dB
0	1	1	1	1	1	-34.5dB
1	X	X	X	X	X	Mute

■ Record Select Control Register (Index 1Ah)

SR2	SR1	SR0	Att.
0	0	0	Mic
0	0	1	CD In (R)
0	1	0	Video In (R)
0	1	1	Aux In (R)
1	0	0	Line In (R)
1	0	1	Stereo Mix (R)
1	1	0	Mono Mix
1	1	1	Phone

SL2	SL1	SL0	Att.
0	0	0	Mic
0	0	1	CD In (L)
0	1	0	Video In (L)
0	1	1	Aux In (L)
1	0	0	Line In (L)
1	0	1	Stereo Mix (L)
1	1	0	Mono Mix
1	1	1	Phone

■ Record Gain Register (Index 1Ch)

Mute	Gx3	Gx2	Gx1	Gx0	Gain
0	0	0	0	0	0dB
0	0	0	0	1	1.5dB
0	0	0	1	0	3.0dB
0	1	1	1	1	22.5dB
1	X	X	X	X	Mute

■ General Purpose Register (Index 20h)

Bit	Function
MIX	Mono output select 0=mix, 1=mic
MS	Mic select 0=Mic1, 1 =Mic2
LPBK*	ADC/DAC loopback mode 1= loopback

*) When LPBK bit is set, slot3-valid- bit and slot4-valid-bit in the tag phase of SDATA_OUT stream must be set regardless of the audio data (slot 3 and slot4).

■ Powerdown Control/Status Register (Index 26h)

Bit	Function
REF*)	Vrefs up to normal state 0=NOT ready, 1=ready,
ANL	Analog mixers, etc ready 0=NOT ready, 1=ready
DAC	DAC section ready to accept data 0=NOT ready, 1=ready
ADC	ADC section ready to transmit data 0=NOT ready, 1=ready

Any write to this register does not affect the state of the above bits.
*) It takes 512fs (fs: sampling frequency) from the release of VREF powerdown for this bit to be ready. This means that the AK4540 does not measure the VREF value actually.

Bit	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer Powerdown (Vref still on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	Digital Interface (AC-likk) Powerdown

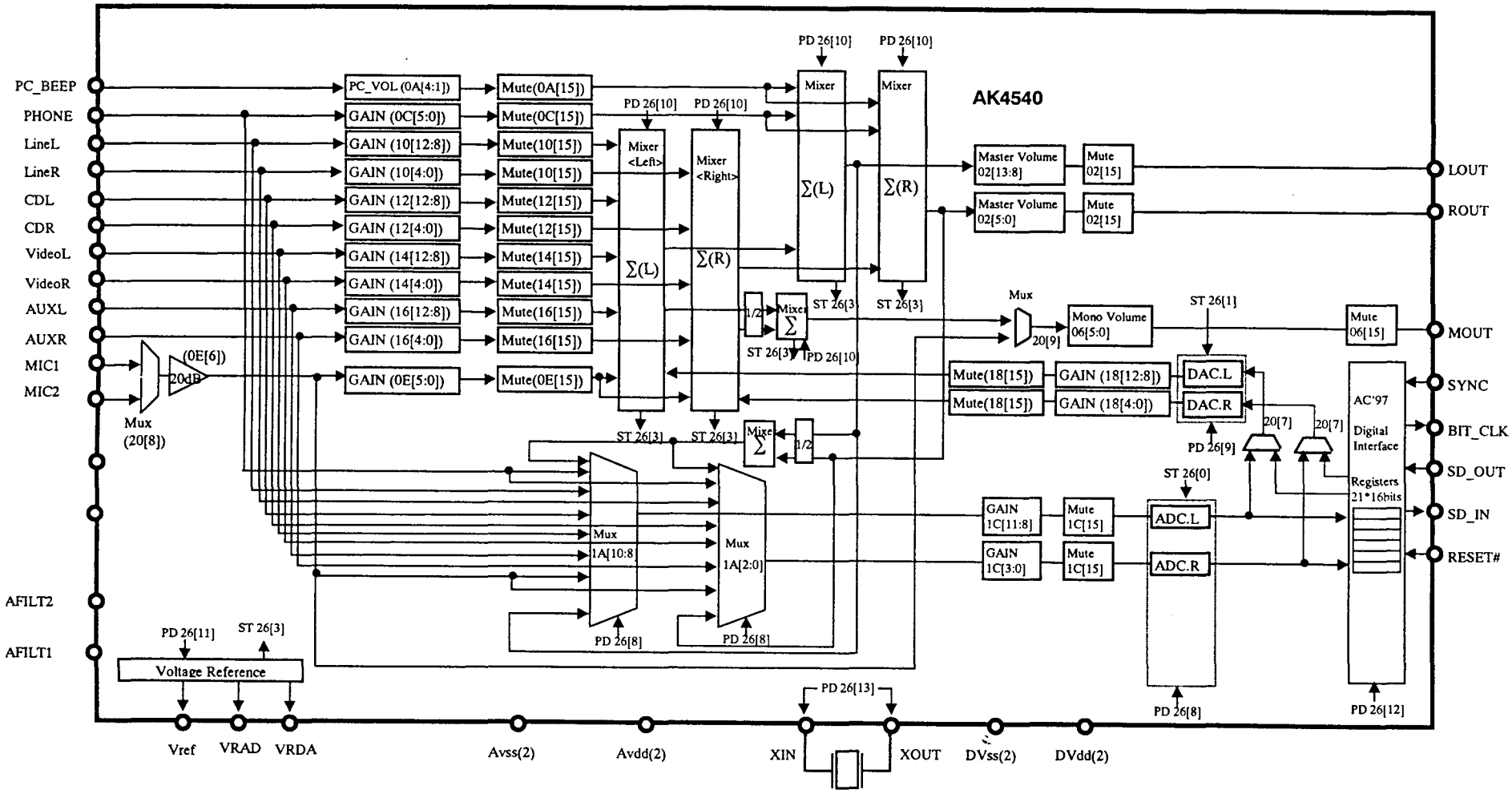
When PR3 bit is set to "1", ADC, DAC, Mixer, and VREF are powered down even if any PRx bit are "0". When PR3 bit is reset to "0", the AK4540 resumes the previous state by referencing PRx bit. In this case, the AK4540 outputs corresponding slot-x valid bits in the slot 0 as "0" until the AK4540 is power-up.

■ Vendor ID Registers (Index 7Ch, 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft Plug and Play Vendor ID code with upper byte of 7Ch register, the first character of that id, lower byte of 7Ch register, the second character and upper byte of 7Eh register the third character. These three characters are ASCII encoded. Lower byte of 7E register is for the Vendor Revision number.

AKM's vender ID is "AKM", and revision number is 0. As ASCII code "A" is 41h, "K" is 4Bh, and "M" is 4Dh, Vendor ID registers are 414Bh and 4D00h respectively.

AK4540 Block Diagram



■Low Power Modes

The AK4540 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 5 commands of separate power down. See the table below for the different modes. As the AK4540 operate at static mode, the registers will not lose their values even if the external clock is stopped. ***However, note that XTAL_IN pin does not permit floating state.***

	ADC	DAC	Mixer	VREF	ACLINK
PR0="1"	PD	don't care	don't care	don't care	don't care
PR1="1"	don't care	PD	don't care	don't care	don't care
PR2="1"	don't care	PD (TBD)	PD	don't care	don't care
PR3="1"	PD	PD	PD	PD	don't care
PR4="1"	PD	PD	don't care	don't care	don't care

PD: powerdown

Powerdown Mode Truth Table

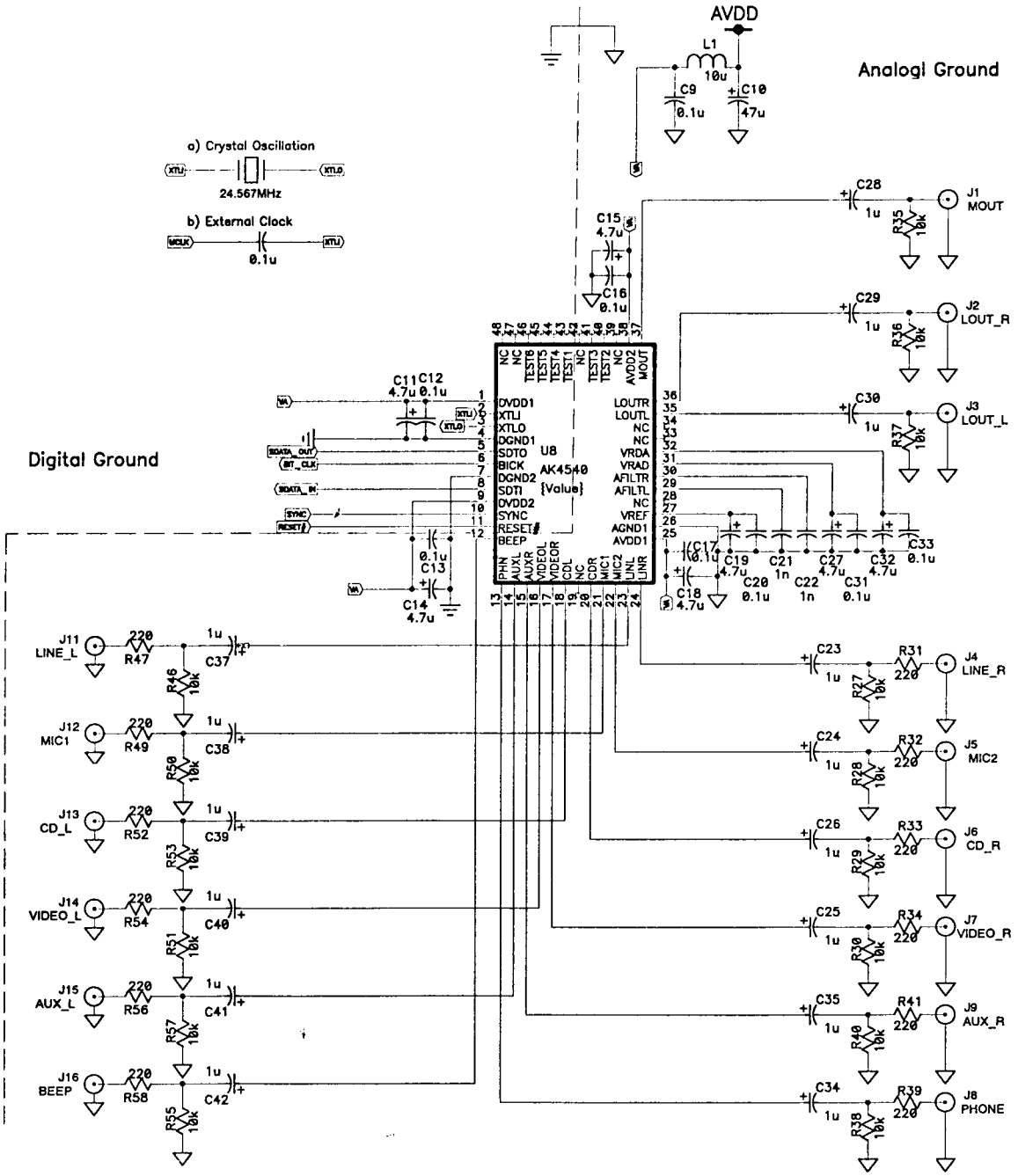
From normal operation sequential writes to the Powerdown Register are performed to power down the AK4540 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC '97 digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC '97 controller will send pulse on the sync line issuing a warm reset. This will restart the AK4540 digital interface (resetting PR4 to zero). The AK4540 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a section is powered back on the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

The above figure and the table show the transition of powerdown and powerup states.
When PR3 bit is set to "1", ADC, DAC, Mixer, and VREF are powered down even if any PRx bit are "0". When PR3 bit is reset to "0", the AK4540 resumes the previous state by referencing PRx bit. In this case, the AK4540 outputs "0" (invalid) for corresponding slot-x valid bits in the slot 0 until the corresponding block of the AK4540 is power-up.

Even if AC'97 digital controller set or clear D13 bit, which is described in AC'97 spec. as PR5 bit of the Powerdown Register, the write does not influence the operation of the AK4540 because the AK4540 ignores this bit.

System Design

The following figure shows the system connection diagram.



1. Grounding and Power Supply Decoupling

The AK4540 requires careful attention to power supply and grounding arrangements. ***Note that the voltage of digital power supply must be equal to or lower than that of analog power supply.*** If not so, the device will be damaged and may be destroyed because of latch up. To observe this rule, digital power supply, Vdd1 and Vdd2, should be supplied from analog power supply. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4540 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip Voltage Reference

The on-chip voltage reference are output on the VRAD, VRDA, Vref pins for decoupling. A electrolytic capacitor less than 10uF in parallel with a 0.1 uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VRDA, VRAD, and Vref pins. All signals, especially clocks, should be kept away from the VRAD, VRDA, and Vref pins in order to avoid unwanted coupling into modulators.

3. Master Clock

If the digital controller which operates at 3.3 volt supplies AK4540's master clock as external clock, insert AC-coupling capacitor(0.1μF) between XTAL_IN pin of the AK4540 and clock output pin of the digital controller. However, ***the digital controller must not stop the clock, or the device may be damaged*** because of the excessive current. ***Also the digital controller must not stop the clock unless XTAL_IN pin is fixed to "H" level or "L" level.*** (Floating state is not permitted)

Performance Example

The following figures show the examples of Input level vs. THD+N, Frequency Response, FFT plot of A/D, D/A respectively.

■Analog-to-Digital Performance

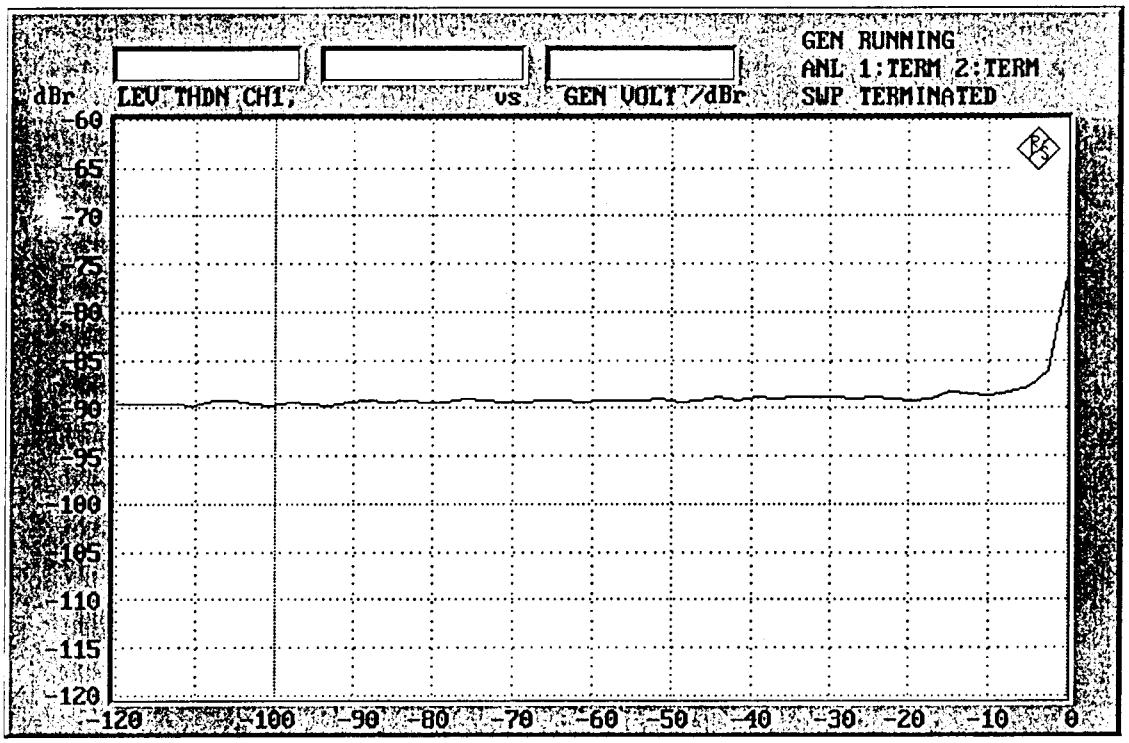


Figure 1 Input Level (@1kHz) vs. THD+N

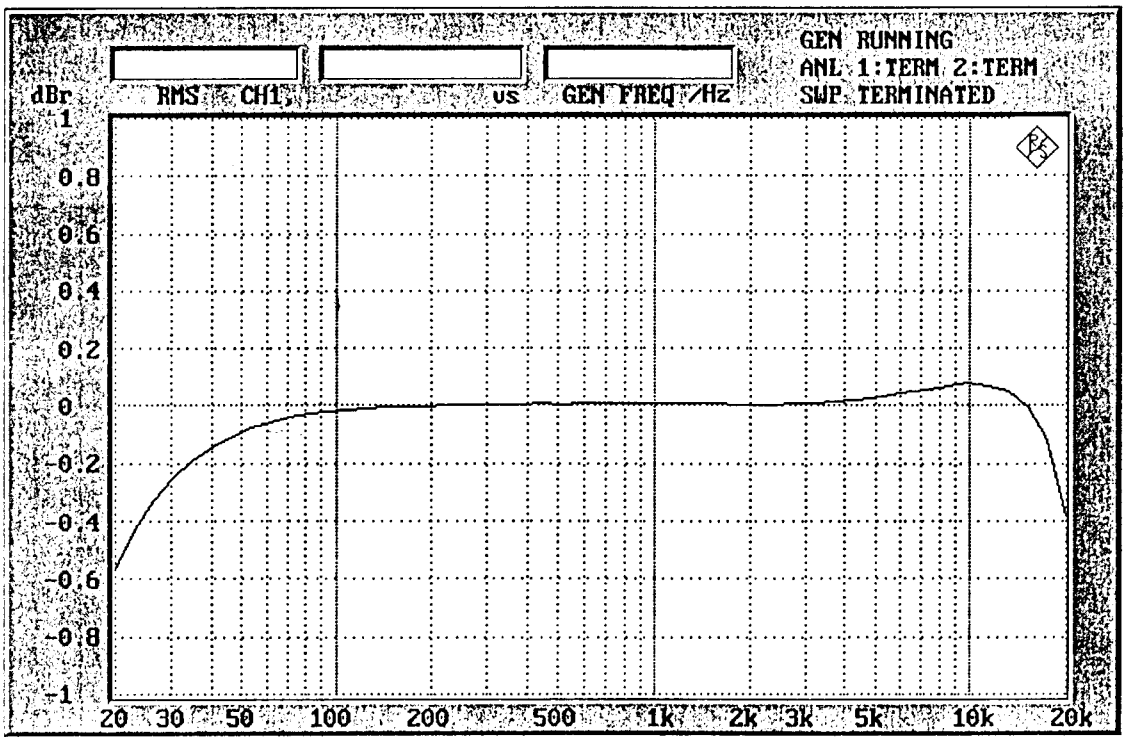


Figure 2 Frequency Response (A/D)

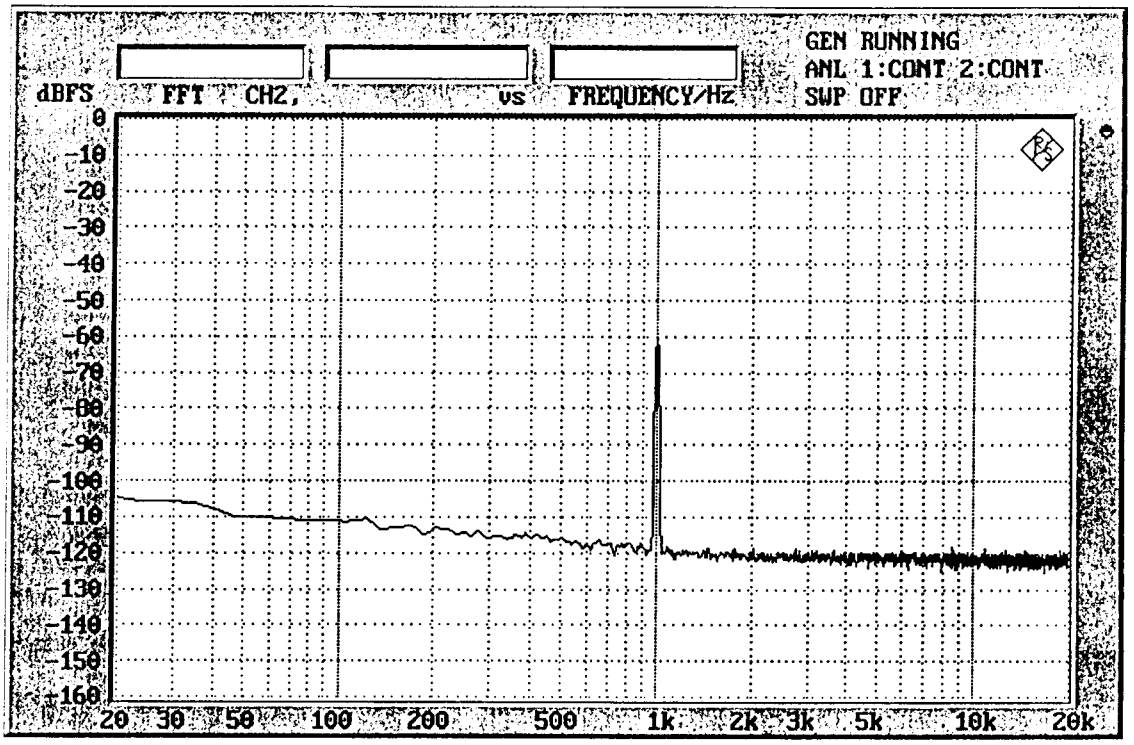


Figure 3 FFT(A/D : Input Signal 1kHz, -60dBFS, FFT Points: 8192, Averaging: 16)

■Digital-to-Analog Performance

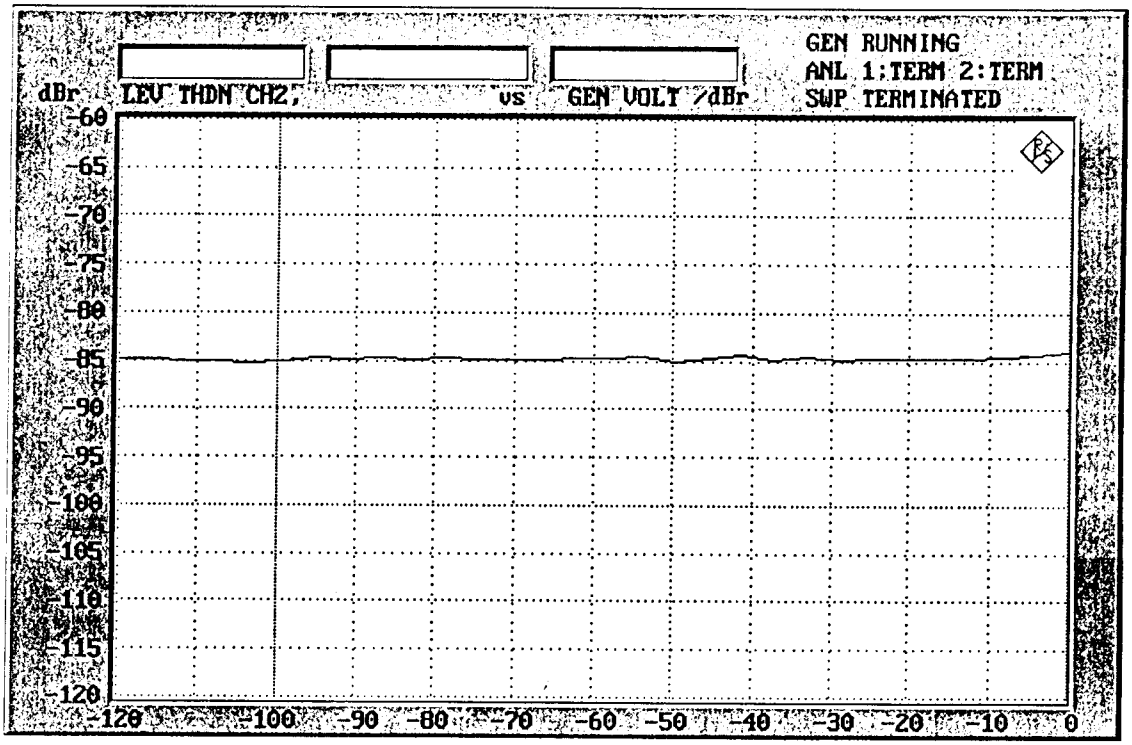


Figure 4 Input Level(@1kHz) vs THD+N

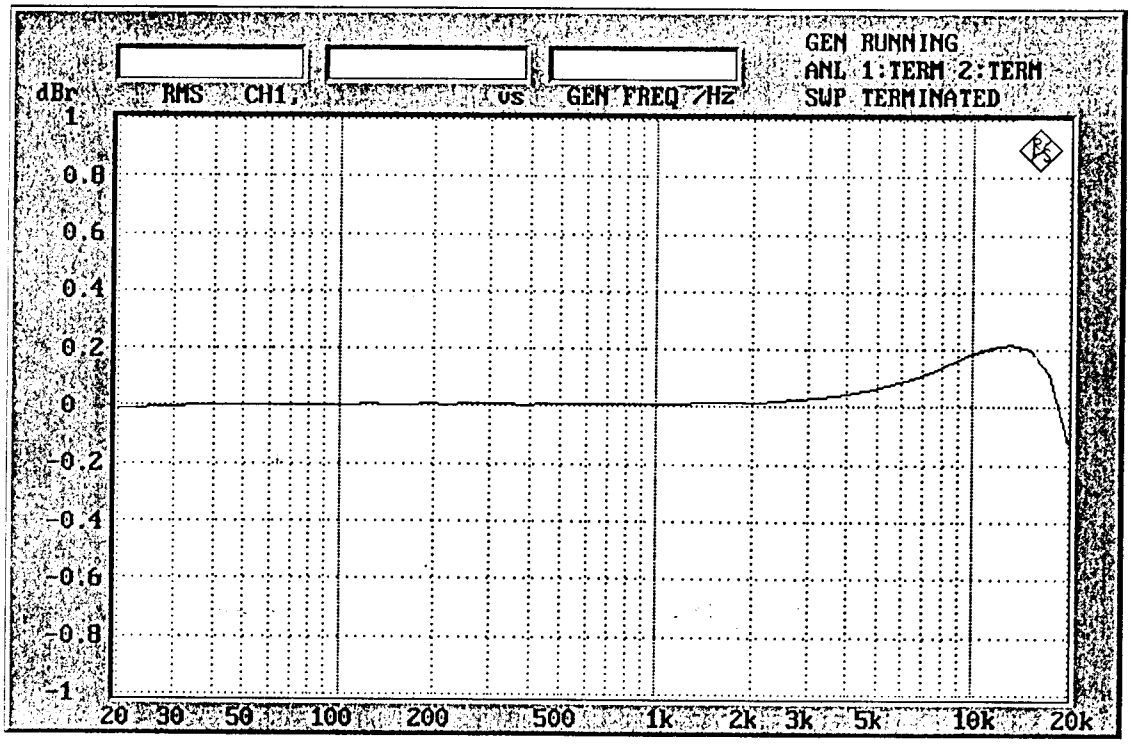


Figure 5 Frequency Response (D/A)

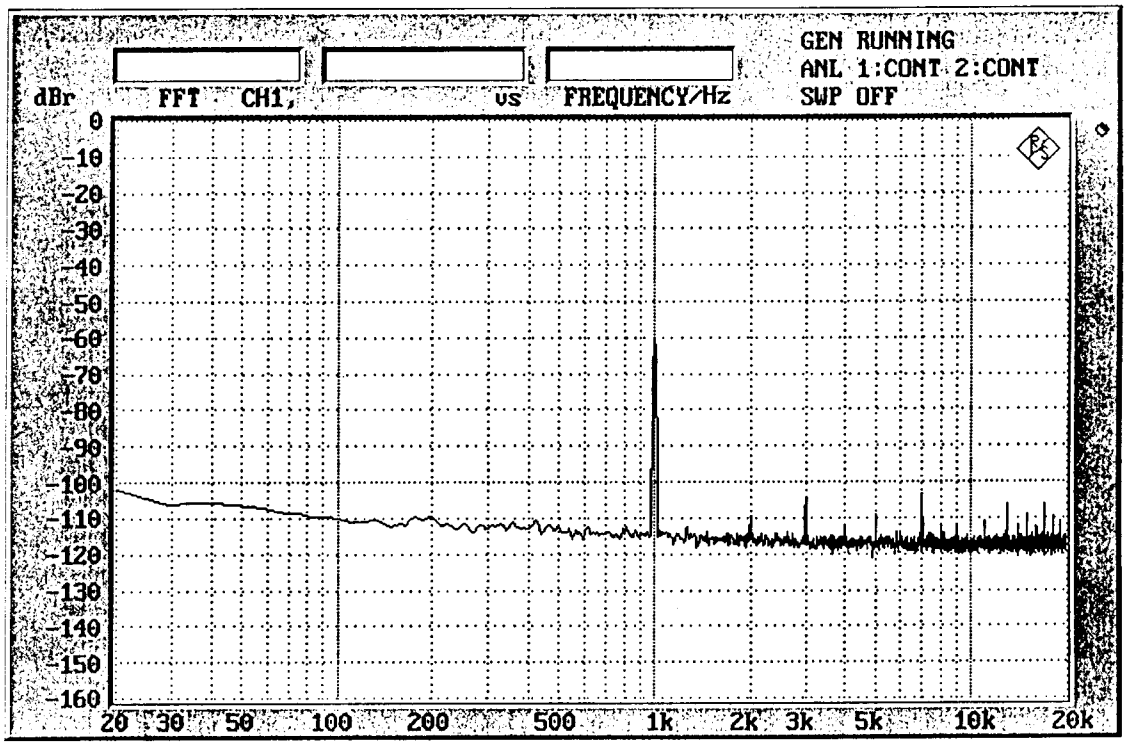


Figure 6 FFT(D/A : Input Signal 1kHz, -60dBFS, FFT Points: 8192, Averaging 16)

■Analog-to-Analog Performance

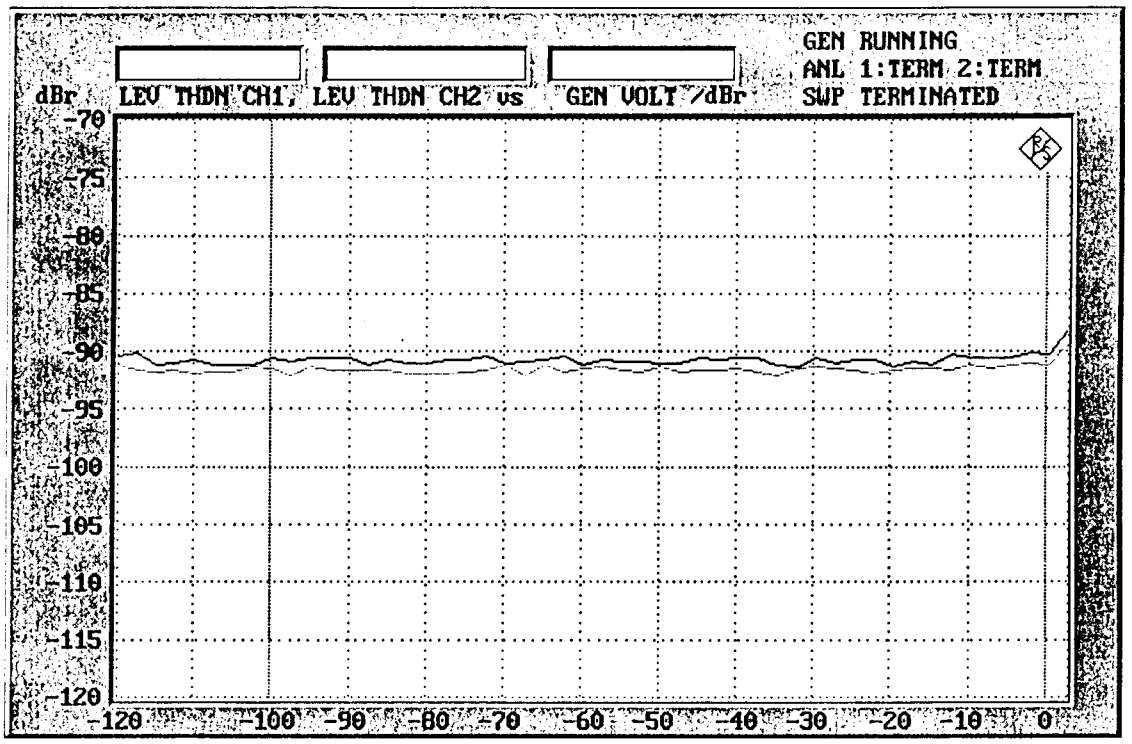
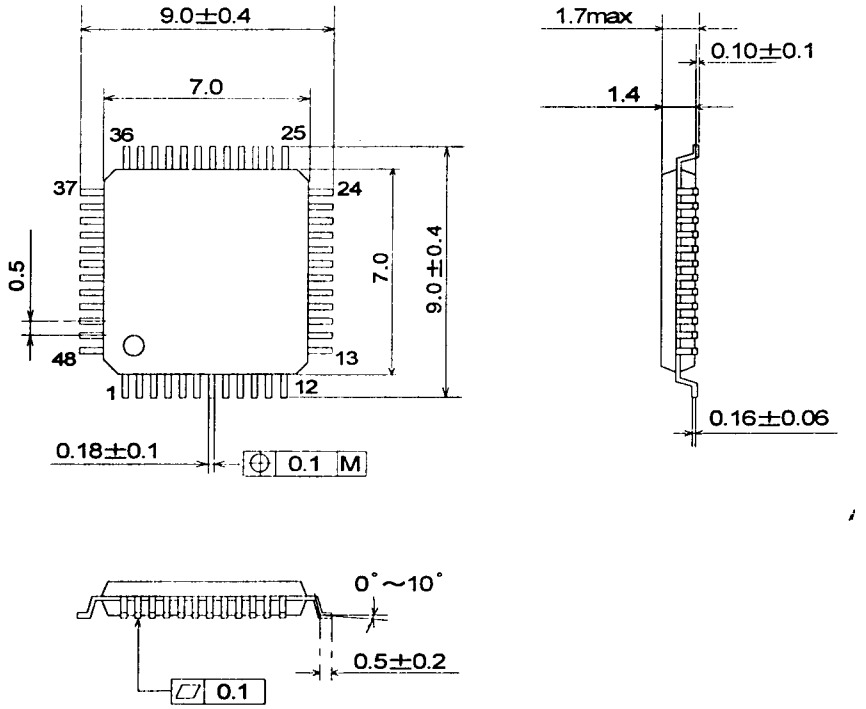


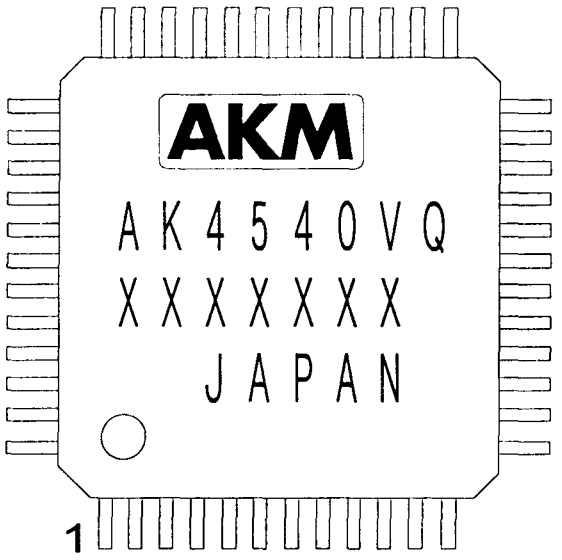
Figure 7 Input Level (@1kHz) vs THD+N

Package

48pin LQFP (Unit:mm)



Marking



1) Pin #1 indication
2) Date Code : XXXXXXX (7 digits)
3) Marketing Code : AK4540-VQ
4) Country of Origin
5) Asahi Kasei Logo

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  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.