AK4591

24bit 4ch ADC with Input selector + 24bit 6ch DAC

1.General Description

The AK4591 is a unique CODEC that combines both high performance and integration in a single chip. The uniqueness begins with the ADC input selector that can select 2 sets of stereo data from 9 sets of available stereo inputs. The 4ch ADC and 6 ch DAC offer high qualityanalog performance with 97dB (48 kHz) dynamic range on the ADC and 107dB (48 kHz) dynamic range on the DAC. This CODEC supports sampling frequencies from 8 kHz to 96 kHz and is suitable for rear seat entertainment to select and distribute 2 different sources in an automotive environment. The AK4591 is packaged in a 64-lead LQFP package offering an operational temperature range of -40°C to 85°C.

2. Features

Input selector

- **Selects 2 sets of stereo data from 9 sets of available stereo inputs**
  - **2 stereo sets of differential**
  - **7 stereo sets of single ended**

ADC: 4 Channels (2 sets of stereo ADC)

- **24-bit 64 x Over-sampling delta sigma**
- **DR, S/N : 97dBA (Fs: 48kHz Full-differential Input)**
- **S/(N+D) : 92 dB (Fs: 48kHz Full-differential Input)**
- **8kHz to 96kHz sampling rate**
- **HPF included for DC offset cancellation**

DAC: 6 Channels (3 sets of stereo DAC)

- **24-bit 128 x Over-sampling advanced multi-bit**
- **DR : 107dBA (6ch) (Fs: 48kHz)**
- **S/N: 108dBA(6ch) (Fs: 48kHz)**
- **S/(N+D) : 90 dB (6ch) (Fs: 48kHz)**
- **8kHz to 96kHz sampling rate**

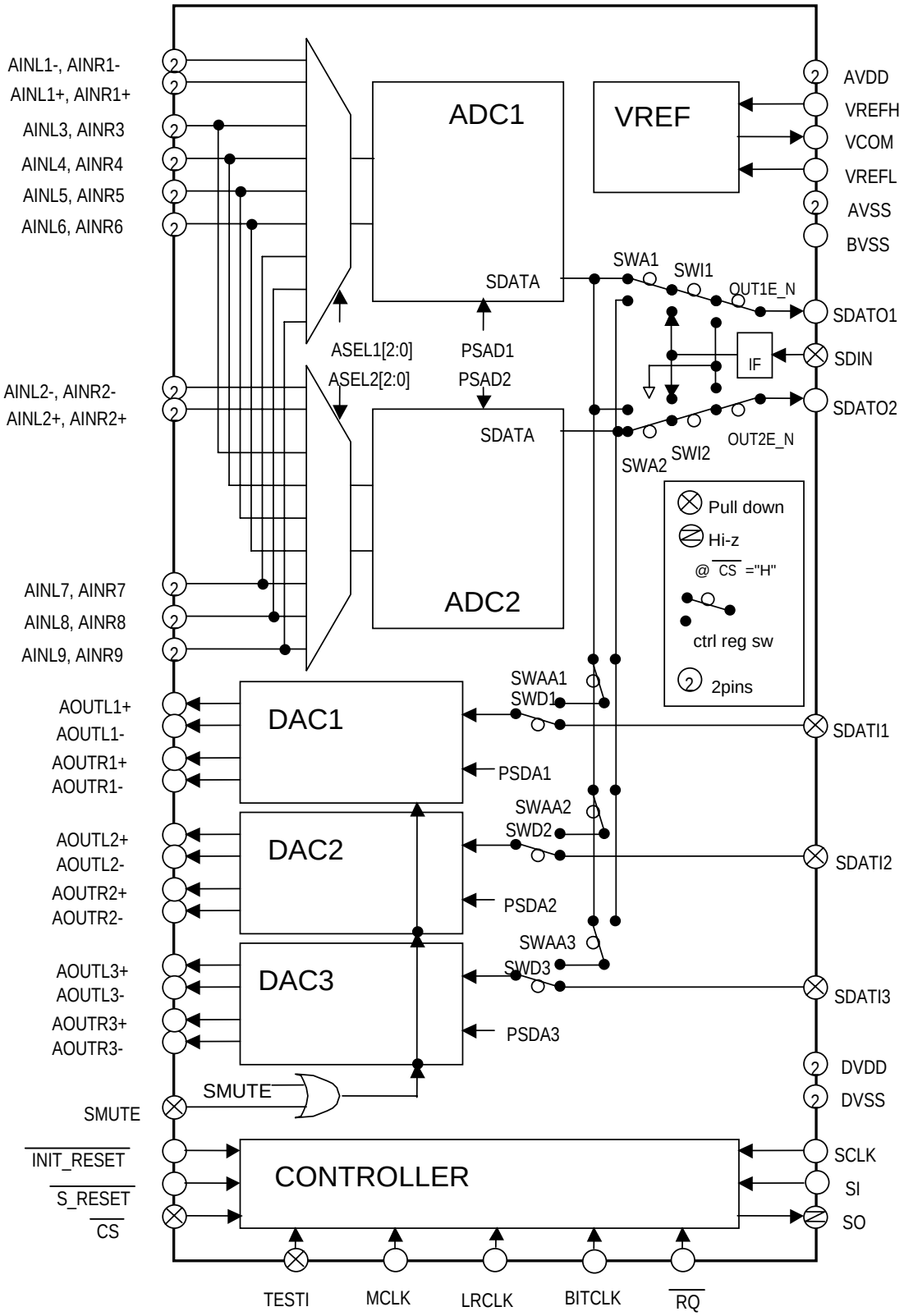
Digital Interface

- **Serial audio signal input port : 8ch**
- **Serial audio signal output port : 4ch**
- **Serial interface port for micro-controller : 1set**

Other

- **Power supply: + 3.3V ±0.3V**
- **Operating temperature range: -40°C~85°C**
- **Package : 64pin LQFP(0.5mm pitch)**

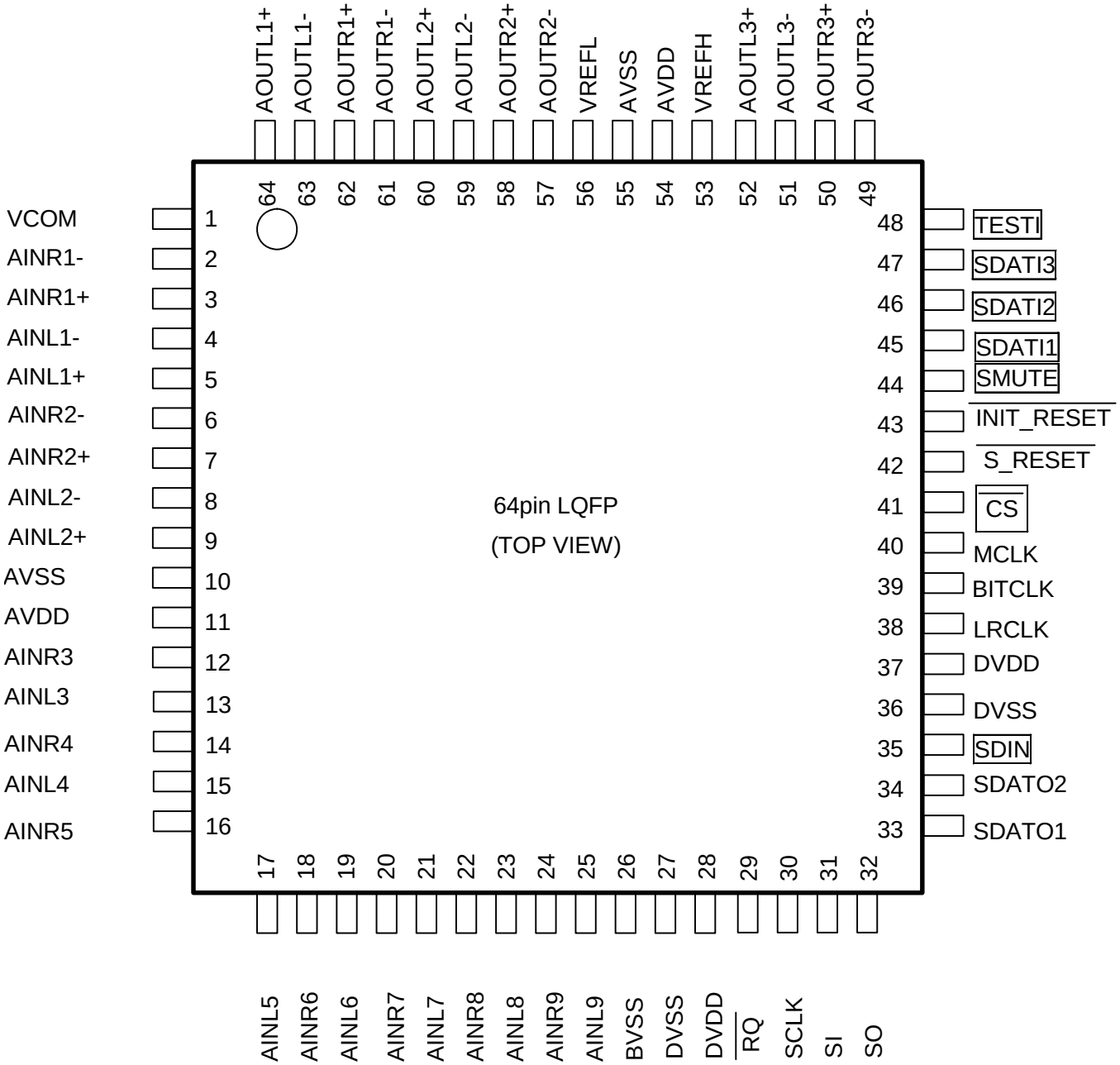
3. Block diagram



This block diagram is a simplified illustration of the AK4591; it is not a circuit diagram.

4. Description of Input/Output Pins

(1) Pin layout



Note) *** is pull-down pin.

(2) Pin function

Pin No.	Pin name	I/O	Function	Classification
1	**VCOM**	O	**Common voltage** Normally connect to 0.1μF and 10μF capacitors between this pin and AVSS. (This pin can not pull out current for an external circuit.)	Analog section
2	**AINR1-**	I	**ADC1 Rch inverted input pin**	Analog input
3	**AINR1+**	I	**ADC1 Rch non-inverted input pin**	
4	**AINL1-**	I	**ADC1 Lch inverted input pin**	
5	**AINL1+**	I	**ADC1 Lch non-inverted input pin**	
6	**AINR2-**	I	**ADC2 Rch inverted input pin**	
7	**AINR2+**	I	**ADC2 Rch non-inverted input pin**	
8	**AINL2-**	I	**ADC2 Lch inverted input pin**	
9	**AINL2+**	I	**ADC2 Lch non-inverted input pin**	
10	**AVSS**	-	**Analog ground 0V**	Analog Power supply
11	**AVDD**	-	**Power supply pin for analog section 3.3V(typ)**	
12	**AINR3**	I	**ADC1 or ADC2 Rch single ended input pin 3**	Analog input
13	**AINL3**	I	**ADC1 or ADC2 Lch single ended input pin 3**	
14	**AINR4**	I	**ADC1 or ADC2 Rch single ended input pin 4**	
15	**AINL4**	I	**ADC1 or ADC2 Lch single ended input pin 4**	
16	**AINR5**	I	**ADC1 or ADC2 Rch single ended input pin 5**	
17	**AINL5**	I	**ADC1 or ADC2 Lch single ended input pin 5**	
18	**AINR6**	I	**ADC1 or ADC2 Rch single ended input pin 6**	
19	**AINL6**	I	**ADC1 or ADC2 Lch single ended input pin 6**	
20	**AINR7**	I	**ADC1 or ADC2 Rch single ended input pin 7**	
21	**AINL7**	I	**ADC1 or ADC2 Lch single ended input pin 7**	
22	**AINR8**	I	**ADC1 or ADC2 Rch single ended input pin 8**	
23	**AINL8**	I	**ADC1 or ADC2 Lch single ended input pin 8**	
24	**AINR9**	I	**ADC1 or ADC2 Rch single ended input pin 9**	
25	**AINL9**	I	**ADC1 or ADC2 Lch single ended input pin 9**	
26	**BVSS**	-	**Analog ground 0V**	Analog Power
27	**DVSS**	-	**Ground pin for digital section 0V**	Digital Power
28	**DVDD**	-	**Power supply pin for digital section 3.3V(typ)**	
29	**$\overline{\text{RQ}}$**	I	**Microcomputer interface write request pin** When $\overline{\text{RQ}}$ ="L" and $\overline{\text{CS}}$ ="L" the interface is enable.	Microcomputer interface
30	**SCLK**	I	**Microcomputer interface serial data clock pin** When SCLK is not used, leave SCLK="H"	
31	**SI**	I	**Microcomputer interface serial data input pin** When the AK4591 does not access to μP I/F , leave SI="L",SCLK="H" and $\overline{\text{RQ}}$ ="H".	
32	**SO**	O	**Serial data output pin for Microcomputer interfaces** When $\overline{\text{CS}}$ ="H", SO is Hi-Z.	
33	**SDATO1**	O	**ADC1 serial data output pin** Outputs MSB justified, I^2S , LSB justified 24bit and 16bit.	Audio interface
34	**SDATO2**	O	**ADC2 serial data output pin** Outputs MSB justified, I^2S , LSB justified 24bit and 16bit.	
35	**SDIN**	I	**Digital serial data input pin (with pull down)** Through, I^2S, MSB justified, LSB justified 24bit and 16bit.	

Pin No.	Pin name	I/O	Function	Classification
36	**DVSS**	-	**Ground pin for digital section 0.0V**	Digital power supply
37	**DVDD**	-	**Power supply pin for digital section 3.3V(typ)**	
38	**LRCLK**	I	**LR channel select clock pin** Input the fs clock	System clock
39	**BITCLK**	I	**Serial bit clock pin** Inputs 64fs. (32 and 48fs are available with conditions attached).	
40	**MCLK**	I	**Master clock input pin**	
41	**$\overline{\text{CS}}$**	I	**Chip select pin for Microcomputer. (with pull down)** $\overline{\text{CS}}$ ="H": SI data cannot be input. SO becomes Hi-z. If $\overline{\text{CS}}$ is not used, connect to DVSS.	Microcomputer Interface
42	**$\overline{\text{S_RESET}}$**	I	**System Reset pin**	Reset
43	**$\overline{\text{INIT_RESET}}$**	I	**Reset pin (for initialization)** Used for initialization of the AK4591.	
44	**SMUTE**	I	**Soft mute pin (with pull down)** Digital Soft mute for DAC. SMUTE="H": Soft mute enabled. SMUTE="L": Soft mute disabled. (Soft mute also can be controlled by a control register.)	Control
45	**SDATI1**	I	**DAC1 Serial data input pin (with pull down)** Compatible with MSB/LSB justified 24,16bits and I^2S.	Digital section Serial input data
46	**SDATI2**	I	**DAC2 Serial data input pin (with pull down)** Compatible with MSB/LSB justified 24,16bits and I^2S.	
47	**SDATI3**	I	**DAC3 Serial data input pin (with pull down)** Compatible with MSB/LSB justified 24,16bits and I^2S.	
48	**TESTI**	I	**Test pin (with pull down)** Connect to DVSS.	Control
49	**AOUTR3-**	O	**DAC3 Rch analog inverted output pin.**	Analog output
50	**AOUTR3+**	O	**DAC3 Rch analog non-inverted output pin.**	
51	**AOUTL3-**	O	**DAC3 Lch analog inverted output pin.**	
52	**AOUTL3+**	O	**DAC3 Lch analog non-inverted output pin.**	
53	**VREFH**	I	**Analog Reference voltage input pin** Normally, connect to AVDD (54pin) with 0.1μF and 10μF capacitors between this pin and AVSS.	Analog section
54	**AVDD**	-	**Power supply pin for analog section 3.3V(typ)**	Power supply
55	**AVSS**	-	**Analog ground 0.0V**	
56	**VREFL**	I	**Analog low level Reference voltage input pin** Normally, connect to AVSS (55pin).	Analog section
57	**AOUTR2-**	O	**DAC2 Rch analog inverted output pin.**	Analog output
58	**AOUTR2+**	O	**DAC2 Rch analog non-inverted output pin.**	
59	**AOUTL2-**	O	**DAC2 Lch analog inverted output pin.**	
60	**AOUTL2+**	O	**DAC2 Lch analog non-inverted output pin.**	
61	**AOUTR1-**	O	**DAC1 Rch analog inverted output pin.**	
62	**AOUTR1+**	O	**DAC1 Rch analog non-inverted output pin.**	
63	**AOUTL1-**	O	**DAC1 Lch analog inverted output pin.**	
64	**AOUTL1+**	O	**DAC1 Lch analog non-inverted output pin.**	

Note) Don't leave Digital input pin (29, 30, 31, 35, 38~48pin) open except for pull down pins.
Pull down pins indicated as (with pull down).
(When pull down pin does not use, then leave open or connect to DVSS)
(We recommend connecting TESTI (48pin) with DVSS.)

5. Absolute maximum rating

(AVSS,BVSS,DVSS=0V: All voltage indicated are relative to the ground.)

Item Symbol		min	max	Unit
Power supply voltage				
Analog(AVDD)	VA	-0.3	4.6	V
Digital(DVDD)	VD	-0.3	4.6	V
|AVSS(BVSS)-DVSS| Note 1)	ΔGND		0.3	V
Input current (except for power supply)	IIN	-	±10	mA
Analog input voltage AINL1+,AINL1-,AINR1+,AINR1-, AINL2+,AINL2-,AINR2+,AINR2-, AINL3~9,AINR3~9,VREFH,VREFL		-0.3	VA+0.3	V
Digital input voltage	VIND	-0.3	VD+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note 1) AVSS(BVSS) should be same level as DVSS.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

6. Recommended operating conditions

Power supply

(AVSS,DVSS,BVSS=0.0V : All voltages indicated are relative to the ground)

Items Symbol		min	typ	max	Unit
Power supply voltage					
AVDD	VA	3.0	3.3	3.6	V
DVDD	VD	3.0	3.3	3.6	V
Reference voltage					
VREFH Note 1)	VRH		VA		V
VREFL Note 2)	VRL		0.0		V

Note 1) VREFH normally connect with AVDD.

Note 2) VREFL normally connect with AVSS

Note The analog input voltage and output voltage are proportional to the VREFH – VREFL voltages.

7. Electric characteristics

(1) Analog characteristics

(Unless otherwise specified,Ta=25 °C; AVDD=DVDD=3 .3V;VREFH=AVDD;VREFL=AVSS;BITCLK=64fs; Signal frequency 1kHz; Measuring frequency =20 Hz~20kHz(@48kHz); 20Hz~40kHz(@96kHz); MCLK=12.288MHz (256fs@48kHz); 24.576MHz (256fs@96kHz); ADC with all differential inputs except for LSB justified 16bit and BITCLK 32fs mode)

Parameter		min	typ	max	Unit
ADC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dBFS) (Note 1)	82 92		dB	
	fs = 96kHz (-1dBFS) (Note 1)		88		dB
	Dynamic range fs=48kHz (A filter) (Note1,2)	87 97		dB	
	fs=96kHz (Note1,2)		93		dB
	S/N fs = 48kHz (A filter) (Note 1)	87 97		dB	
	fs = 96kHz (Note 1)		93		dB
	Inter-channel isolation (f=1kHz) (Note 3)	90	115		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Analog input				
	Input voltage (differential) (Note 4)	±1.85	±2.00	±2.15	Vp-p
	Input voltage (single-ended) (Note 5)	1.85	2.00	2.15	Vp-p
	Input impedance (Note 6)	22	33		kΩ
DAC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (0dBFS)	80 90		dB	
	fs = 96kHz (0dBFS)		88		dB
	Dynamic range fs = 48kHz (A filter) (Note 2)	97 107		dB	
	fs = 96kHz (Note 2)		102		dB
	S/N fs = 48kHz (A filter)	97 108		dB	
	fs = 96kHz		103		dB
	Inter-channel isolation (f=1kHz) (Note 7)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching		0.2	0.5	dB
	Analog output				
	Output voltage (AOUT+)-(AOUT-) (Note 8)	3.36	3.66	3.96	Vp-p
	Load resistance	5			kΩ
	Load capacitance			20	pF

Note

1. In case of the using single-ended input, this value is not guaranteed.
2. Indicates S/ (N+D) when -60 dB signal is applied.
3. Specified for L and R of each input selector.
4. This applies to AINL1+, AINL1-, AINR1+, AINR1-, AINL2+, AINL2-, AINR2+ and AINR2- pins. The full-scale (ΔAIN = (AIN+) – (AIN-)) can represented by (±FS = ±(VREFH-VREFL) ×(2.0/3.3)).
5. This applies to AINL3~L9 and AINR3~R9. The full-scale of single-ended input is (FS= (VREFH-AVSS) ×(2.0/3.3).
6. This applies to AINL1+, AINL1-, AINR1+, AINR1-, AINL2+, AINL2-, AINR2+, AINR2-, AINL3~L9 and AINR3~R9.
7. Specified for L and R of each DAC in case of input 0dBFS signals.
8. The full-scale output voltage when VREFH=AVDD, VREFL=AVSS.

(2) DC characteristics

VDD=AVDD=DVDD=3.0~3.6V(typ=3.3V),Ta=-45°C~85°C

Parameter Symbol		min	typ	max	Unit
High level input voltage	VIH	80%VDD			V
Low level input voltage	VIL			20%VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current (pull down) Note 2)	Iid		22		μA

Note:

1. The pull-down pins are not included.
2. The pull-down resistor value is 150kΩ. The pull-down pins are the following:

   SDIN, $\overline{CS}$,SMUTE,SDATI1,SDATI2,SDATI3,TESTI

Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus, (serial/parallel) such as registers.

(3) Current consumption

AVDD=DVDD=3.0~3.6V(typ=3.3V,max=3.6V),Ta=25°C;MCLK=24.576MHz=256fs[fs=96kHz];

Parameter min		typ	max	Unit
Power supply current				
1) In active mode				
a) AVDD		78		mA
b) DVDD	27			mA
c) Total(a+b)		105	150	mA

(4) Digital filter characteristics

Values described below are design values cited as references.

4-1) ADC Section

(Ta=25°C; AVDD,DVDD=3.0~3.6V; fs=48kHz;HPF=off)

Parameter Symbol		min	typ	max	Unit
Pass band ±0.005dB	PB 0			21.5	kHz
(-6.0dB)		-	24.00	-	kHz
Stop band (Note 1)	SB	26.5			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Note 3)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts=1/fs)	GD		29.3		Ts

Note : HPF response is not including.
Note 1) : The stop band is from 26.5kHz to 3.0455MHz when fs=48kHz.
Note 2) : The pass band is from DC to 21.5kHz when fs=48kHz.
Note 3) : When fs=48kHz, the analog modulator samples analog input at 3.072MHz.
The input signal is not attenuated by the digital filter in the multiple bands
(n x 3.072MHz ± 21.99kHz; n=0,1,2,3…..) of the sampling frequency.

4-2) DAC section

4-2-1) DAF=0 (CONT5 D4) : fs = 48kHz

(Ta=25°C; AVDD,DVDD=3.0~3.6V; fs=48kHz)

Parameter Symbol		min	Typ	max	Unit
Digital filter					
Pass band ±0.08dB	PB	0		21.2	kHz
(-0.28dB) (Note 1)		-	21.7	-	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 1)	SB	26.5			kHz
Pass band ripple	PR			±0.04	dB
Stop band attenuation	SA	47			dB
Group delay(Ts=1/fs) (Note 2)	GD	-	15.0		Ts
Digital filter + SCF					
Amplitude characteristics (0~20.0kHz)			±0.5	dB	

Note 1): The pass band and stop band frequencies are proportional to system sampling rate, and represents PB=0.4535fs(@-0.28dB) and SB=0.5519fs.

Note 2): This calculated delay time which occurs in the digital filter is from setting the 24-bit data of both channels on input register to the output of analog signal.

4-2-2) DAF=1 (CONT5 D4) : fs = 48kHz

(Ta=25°C; AVDD,DVDD=3.0~3.6V; fs=48kHz)

Parameter Symbol		min	Typ	max	Unit
Digital filter					
Pass band ±0.02dB	PB	0		20.6	kHz
(-0.48dB) (Note 1)		-	21.7	-	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 1)	SB	27.4			kHz
Pass band ripple	PR			±0.01	dB
Stop band attenuation	SA	59			dB
Group delay(Ts=1/fs) (Note 2)	GD	-	15.0		Ts
Digital filter + SCF					
Amplitude characteristics (0~20.0kHz)			±0.5	dB	

Note 1): The pass band and stop band frequencies are proportional to system sampling rate, and represents PB=0.4535fs (@-0.48dB) and SB=0.5704fs.

Note 2): This calculated delay time which occurs in the digital filter is from setting the 24-bit data of both channels on input register to the output of analog signal.

(5) Switching characteristics

5-1) System clock

(AVDD=DVDD=3.0~3.6V,Ta=-40°C~85°C)

Parameter	Symbol	min	typ	max	Unit
MCLK					
Duty factor		40	50	60	%
CKS=0 (Note 1)	fMCLK				
DFS[1:0]=0h		2.0	12.288	12.8	MHz
DFS[1:0]=1h		8.0	8.192	12.8	MHz
DFS[1:0]=2h		20.48	24.576	25.0	MHz
CKS=1 (Note 1)	fMCLK				
DFS[1:0]=0h		3.5	18.432	19.2	MHz
DFS[1:0]=1h		12.0	12.288	19.2	MHz
Clock rise time	tCR			6	ns
Clock fall time	tCF			6	ns
LRCLK : frequency (Note 1)	fs		1	-	fs
DFS[1:0]=0h		8		48	kHz
DFS[1:0]=1h		8		12	kHz
DFS[1:0]=2h		80		96	kHz
Clock rise time	tLR			6	ns
Clock fall time	tLF			6	ns
BITCLK : frequency (Note 2)	fBCLK (32)			64	fs
High level width	tBCLKH	72		ns	
Low level width	tBCLKL	72			ns
Clock rise time	tBR			6	ns
Clock fall time	tBF			6	ns

Note 1) CKS,CKS1,DFS[1:0] are setting values for control register.

Note 2) BITCLK can use normally 64fs. 48fs and 32fs are also available. However, 32fs and 48fs mode have some limitation.

5-2) Reset

(AVDD=DVDD=3.0~3.6V,Ta=-40°C~85°C)

Parameter Sy		mbol	min	typ	max	Unit
$\overline{\text{INIT_RESET}}$	Note 1	tRST 400				ns
$\overline{\text{S_RESET}}$	Note 1	tRST 400				ns

Note 1) "L" is acceptable when power is turned on, but afer stable power level it must keep at least "min" time.

5-3) Audio interface

(AVDD=DVDD=3.0~3.6V,Ta=-40°C~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Delay from BITCLK"↑" to LRCLK (Note 1)	tBLRD	40			ns
Delay from LRCLK to BITCLK"↑" (Note 1)	tLRBD	40			ns
Delay from LRCLK to serial data output	tLRD			40	ns
Delay from BITCLK to serial data output	tBSOD			40	ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay from SDIN to SDATO1 or SDATO2 (In the case of "Through" mode)	tSISO			45	ns

Note 1) This feature is to avoid LRCLK edge and BITCLK "↑" edge.

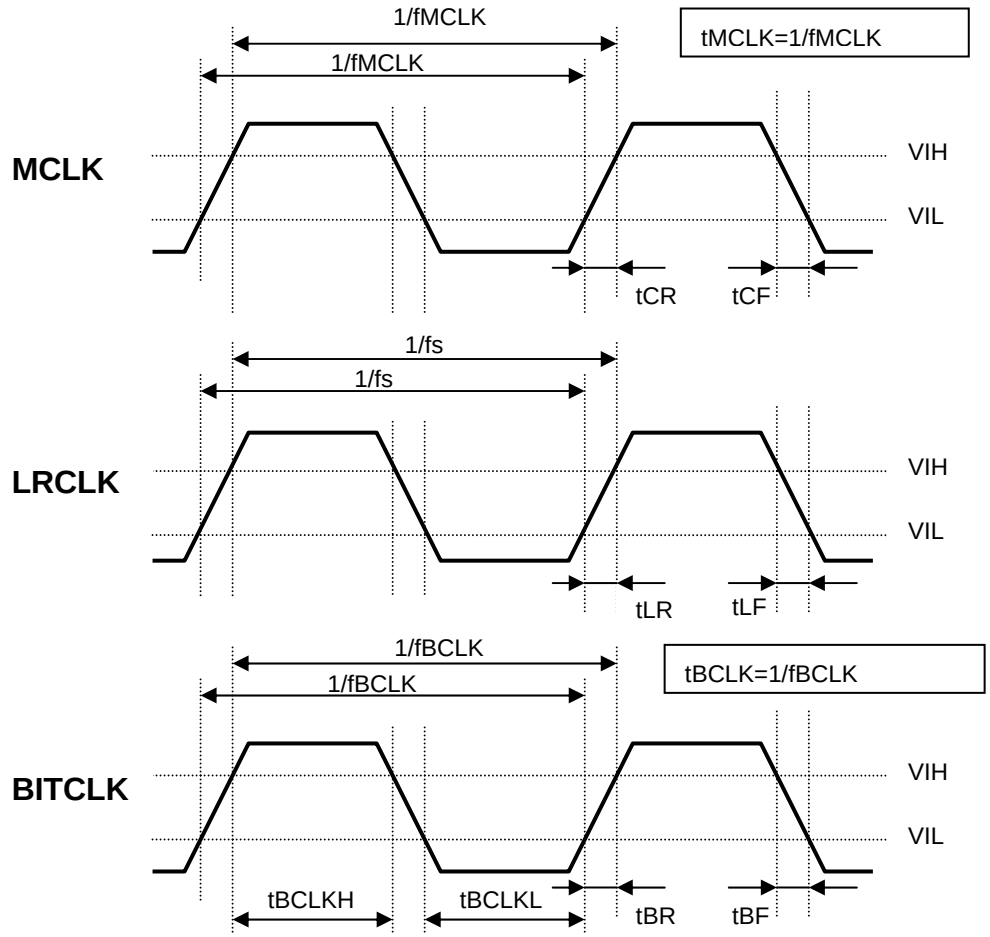
5-4) Microcomputer interface

(AVDD=DVDD=3.0~3.6V,Ta=-40°C~85°C,CL=20pF)

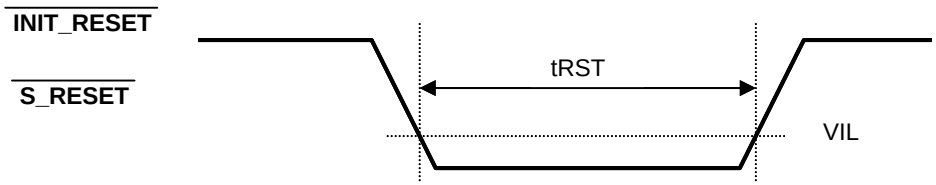
Parameter	Symbol	min	typ	max	Unit
Microcomputer interface signal					
$\overline{RQ}$ Fall time	tWRF			8	ns
$\overline{RQ}$ Rise time	tWRR			8	ns
SCLK fall time	tSF			8	ns
SCLK rise time	tSR			8	ns
SCLK low level width	tSCLKL	100			ns
SCLK high level width	tSCLKH	100			ns
Microcomputer to AK4591					
Time from $\overline{S_RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
Time from $\overline{RQ}$ "↑" to $\overline{S_RESET}$ "↑"	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	200			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
Delay from SCLK "↓" to SO output	tSOD			100	ns
$\overline{CS}$					
$\overline{CS}$ Fall time	tCSF			8	ns
$\overline{CS}$ Rise time	tCSR			8	ns
Time from $\overline{S_RESET}$ "↓" to $\overline{CS}$ "↓"	tWRCS	400			ns
Time from $\overline{CS}$ "↑" to $\overline{S_RESET}$ "↑"	tWCSR	400			ns
$\overline{CS}$ high level width	tWCSH	800			ns
Time from $\overline{CS}$ "↓" to $\overline{RQ}$ "↓"	tWCSRQ	400			ns
Time from $\overline{RQ}$ "↑" to $\overline{CS}$ "↑"	tWRQCS	400			ns
$\overline{CS}$ "↓" to Hi-Z release of SO (RL=10kΩ)	tCSHR			600	ns
$\overline{CS}$ "↑" to Hi-Z setting of SO (RL=10kΩ)	tCSHS			600	ns

(6) Timing waveform

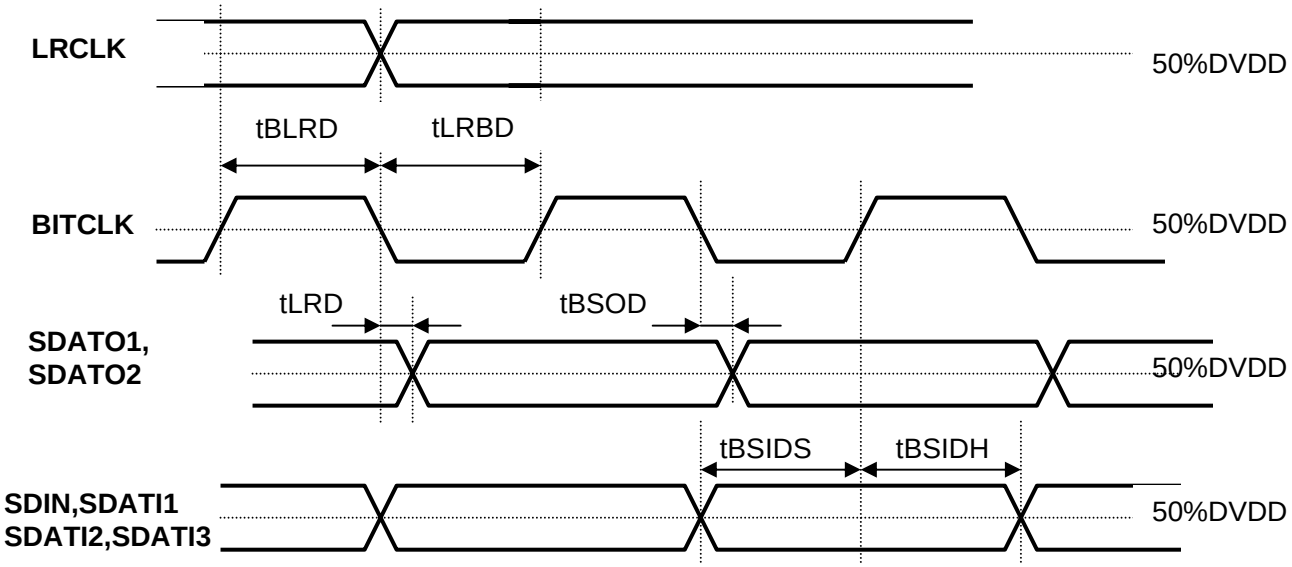
6-1) System clock



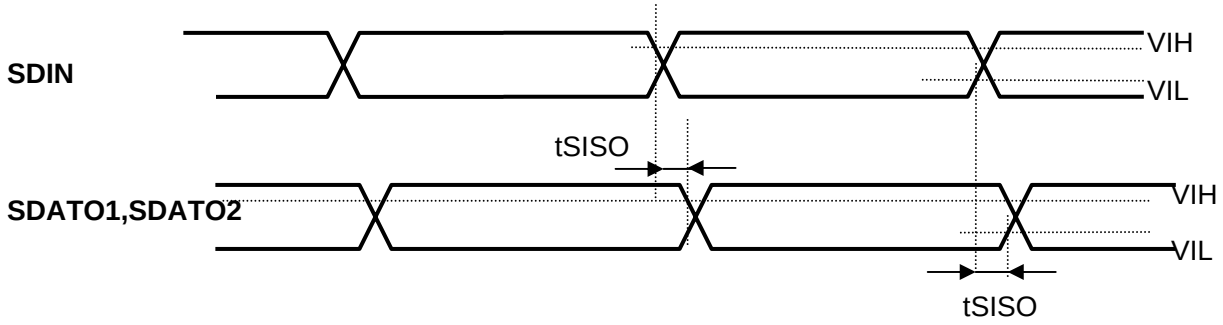
6-2) RESET



6-3) Audio interface

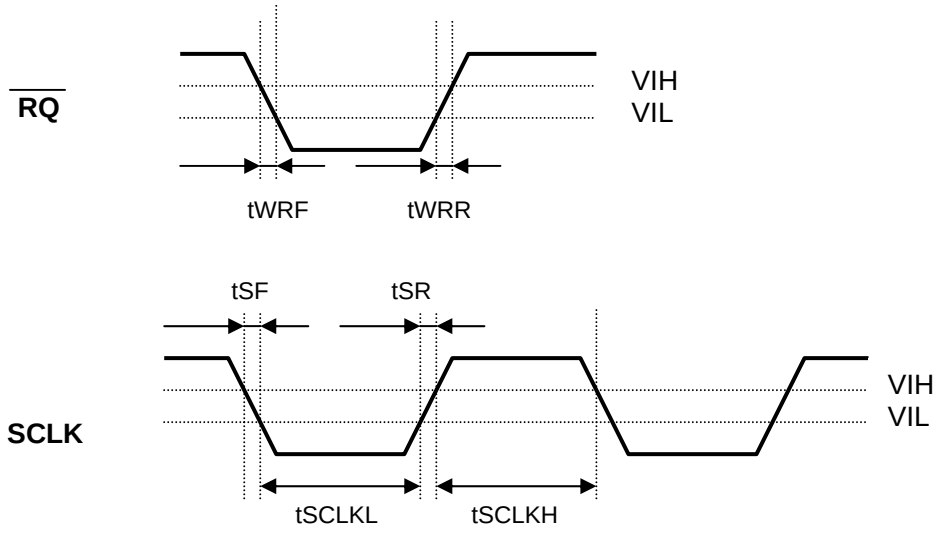


Note) SDIN Through selected (see. CONT2 setting)

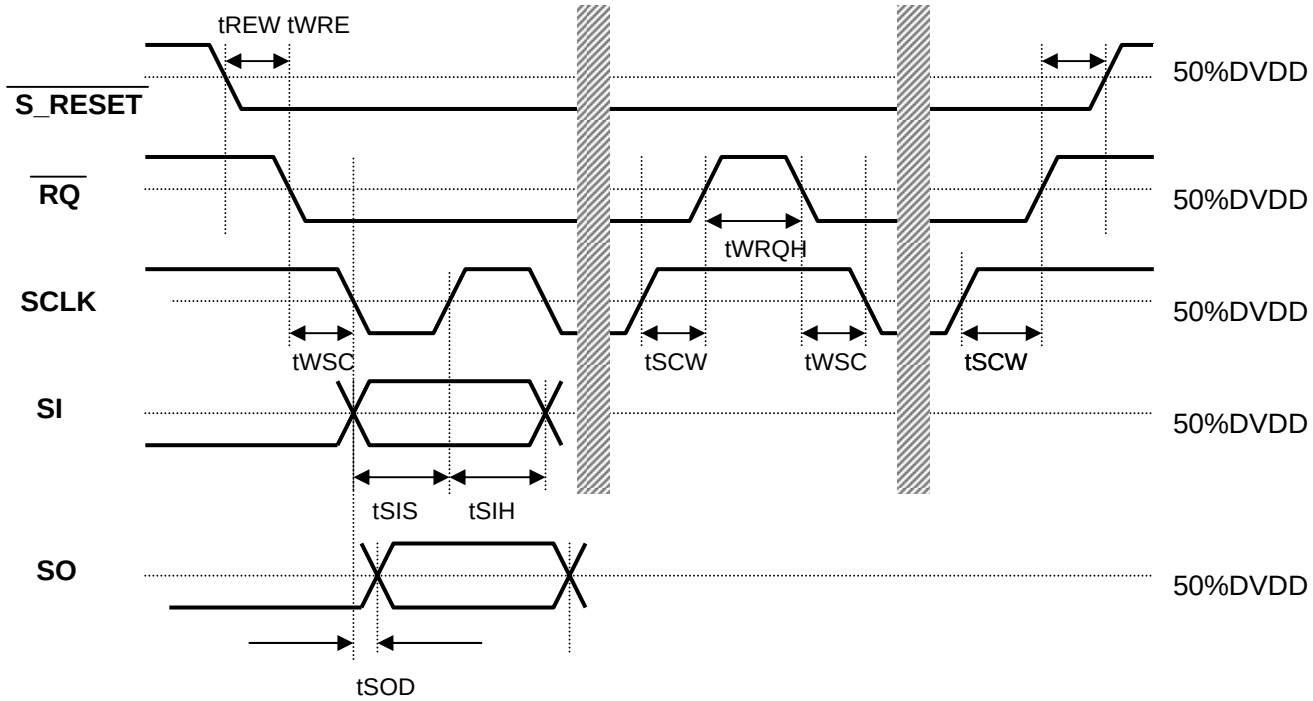


6-4) Microcomputer interface

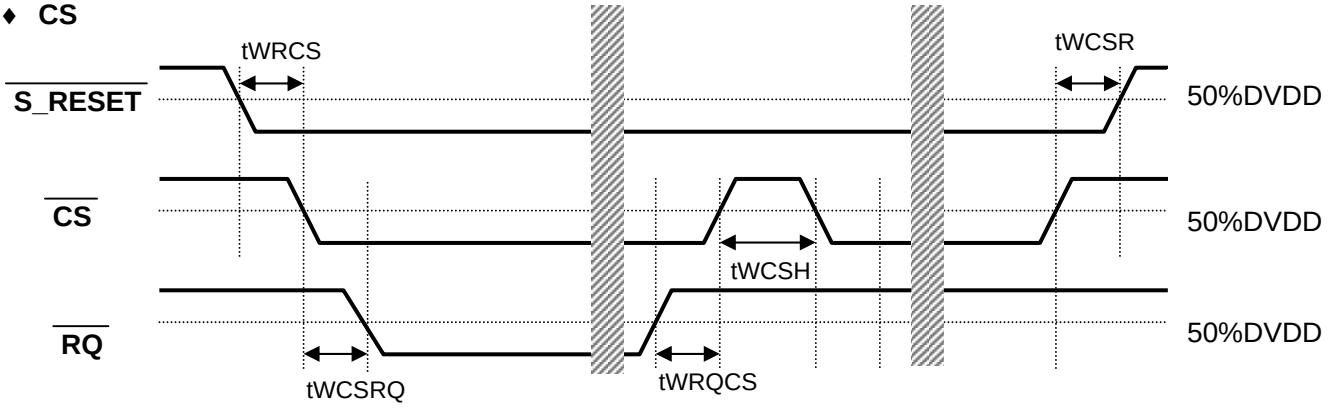
♦ Microcomputer interface



♦ AK4591 ↔ Microcomputer



♦ $\overline{CS}$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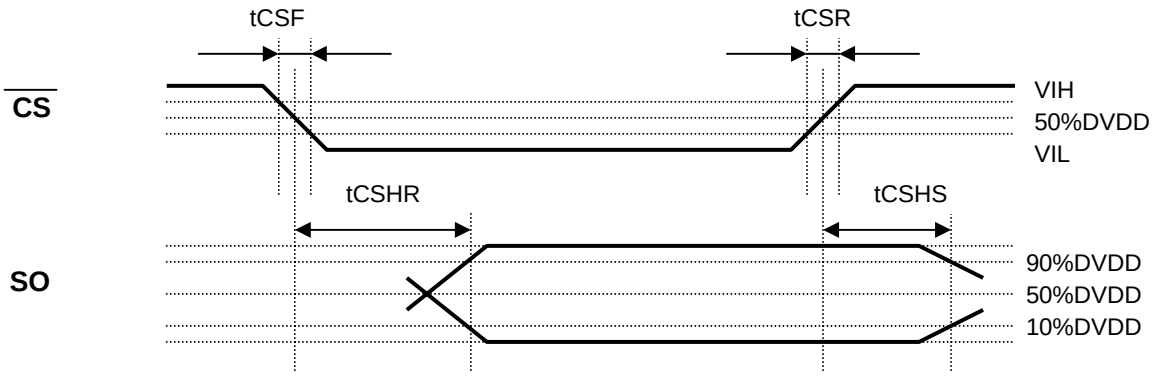
tWCSR
S_RESET
50%DVDD
CS
50%DVDD
tWCSH
RQ
50%DVDD
tWCSRQ
tWRQCS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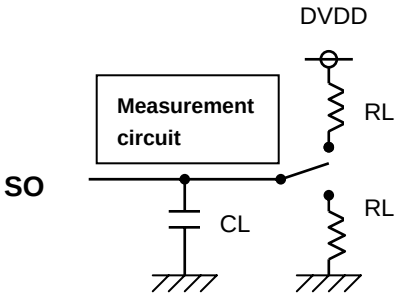
tCSR
CS
VIH
50%DVDD
VIL
tCSHR
tCSHS
SO
90%DVDD
50%DVDD
10%DVDD


DVDD
Measurement circuit
RL
SO
CL
RL

8. Function Description

(1) Control registers setting

The control registers can be set via the micro controller interface in addition to the control pins. The 7 control registers consist of 7-bit data however; SCLK always needs 16bit clock (Command Code 8bit, Data 8bit). Each register is set after the last D0 data is written. For the value to be written in the control registers see the description of the interface with micro controller. The following describes the control register map.

All 7 control registers are initialized by $\overline{\text{INIT_RESET}}$ ="L" to default sate, but they are NOT initialized by $\overline{\text{S_RESET}}$ ="L".

CONT0,CONT1 and CONT7 can only be set at system reset ($\overline{\text{S_RESET}}$ ="L") in order to avoid a possible error. Some other register bits also prohibit being written to except for system reset. We recommend to set other registers during a system reset phase ($\overline{\text{S_RESET}}$ ="L") as well but it is not required. Setting control register on the fly may cause click noise.

The register parameter setting is as following.

T,TEST:TESTmode (Input 0,D0:It ignores input data, but should input 0)

Command Code		Name	D7	D6	D5	D4			D3	D2	D1	D0	Default
Write	Read												
20h	30h	CONT0	**DFS[1]**		**DFS[0]**		**DIFS**	**A2IF[1]**	**A2IF[0]**	**A1IF[1]**	**A1IF[0]**	0	0000 0000
22h	32h	CONT1	**D3IF[1]**	**D3IF[0]**	**D2IF[1]**			**D2IF[0]**	**D1IF[1]**	**D1IF[0]**	**CKS**	0	0000 0000
24h	34h	CONT2	**ISIF[1]**	**ISIF[0]**			**OSIF[1]**	**OSIF[0]**	OUT2E_N	OUT1E_N	**CKSH**	0	0000 0000
26h	36h	CONT3	ASEL1 [2]		ASEL1 [1]		ASEL1 [0]	SWA1	SWI1	PSAD1	**TEST**	0	0000 0000
28h	38h	CONT4	ASEL2 [2]		ASEL2 [1]		ASEL2 [0]	SWA2	SWI2	PSAD2	**TEST**	0	0000 0000
2Ah	3Ah	CONT5	SMUTE		**SF1**	**SF0**		**DAF**	PSDA3	PSDA2	PSDA1	0	0000 0000
2Ch	3Ch	CONT6	SWAA3		SWD3		SWAA2	SWD2	SWAA1	SWD1	**TEST**	0	0000 0000
2Eh	**3Eh**	**CONT7**	**TEST**	**TEST**	**TEST**			**TEST**	**TEST**	**TEST**	**TEST**	0	0000 0000

The bold type registers can be set only at system reset state and are not allowed to be change at any other state.

The LSB bit of the Read and Write code is ignored, however it should write specified "Command Code".

1. **To avoid error action, CONT0 and CONT1 can not beset except for system reset state ($\overline{\text{S_RESET}}$ ="L") CONT7 can not be written to becauseit is for TEST use only. It is not necessary to read CONT7, however the result is 00h if read.**
2. **The following registers on CONT2~CONT6 are forbidden to change except for system reset state. CONT2:D7,D6,D5,D4,D1,CONT3:D1,CONT4:D1,CONT5:D6,D5,D4 and CONT6 :D1. These register should not change when you set CONT2~CONT6 at run time (after release system reset.).**
3. **If TEST registers are included for setting, it should be set to 0.**
4. **All registers are available to be read at run time.**
5. **Default setting means initialized value by $\overline{\text{INIT_RESET}}$ ="L".**
6. **The digital paths set by OUT2E_N,OUT1E_N,SWA1,SWI1,SWA2, SWI2, SWAA3, SWD3, SWAA2, SWD2,SWAA1 and SWD1 are changed at the starting edge of the Left channel of LRCLK after 8LRCLK(max) from rising edge of $\overline{\text{S_RESET}}$. When it changes at run time, it can change in 3LRCLK(max) after registers setting.**

1) CONT0: Sampling rate and ADC interface selection

This register is enable only at system reset state ($\overline{\text{S_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
20h	30h	CONT0	**DFS[1]**	**DFS[0]**	**DIFS**	**A2IF[1]**	**A2IF[0]**	**A1IF[1]**	**A1IF[0]**	0	0000 0000

① D7, D6: DFS [1:0] Sampling rate setting

DFS Mode	DFS[1]	DFS[0]	fs (kHz)	MCLK CKS(CONT1:D1)	
				CKS=0	CKS=1
0	0	0	256fs(fs=48kHz~8kHz)	256fs	384fs
1	0	1	1024fs(fs=12kHz~8kHz)	1024fs	1536fs
2	1	0	256fs(fs=96kHz)	256fs	N/A
3	1	1	N/A TEST		

Note) Recommend DFS mode 1 at fs:12kHz~8kHz (It should set DFS mode 1, except for special case providing only 256fs or 384fs clock.)

② D5:DIFS Audio interface selection

0: AKM method
It should be set to 0, in case of BITCLK48fs and BITCLK32fs.
1: I^2S compatible (24bit)
(In this case, all input / output pins are I^2S compatible. Except SDIN)

③ D4,D3:A2IF[1:0] ADC2 output selection

A2IF Mode	A2IF[1]	A2IF[0]	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified 24bit
2	1	0	N/A
3	1	1	LSB justified 16bit

Note) When DIFS=1, the state is compatible independent of mode setting,
However A2IF mode should be set to 0.
In case of BITCLK48fs or BITCLK32fs then A2IFmode should be set to 0.

④ D2,D1:A1IF[1:0] ADC1 output selection

A1IF Mode	A1IF[1]	A1IF[0]	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified 24bit
2	1	0	N/A
3	1	1	LSB justified 16bit

Note) When DIFS=1, the state is compatible independent of mode setting,
However A1IF mode should be set to 0.
In case of BITCLK48fs or BITCLK32fs then A1IF mode should be set to 0.

⑤ D0: Input always 0

Note) Underlines of the setting of "_" mean default setting.

2) CONT1:DAC interface selection

This register is enable only at system reset state ($\overline{\text{S_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
22h	32h	CONT1	**D3IF[1]**	**D3IF[0]**	**D2IF[1]**	**D2IF[0]**	**D1IF[1]**	**D1IF[0]**	**CKS**	0	0000 0000

① D7,D6:D3IF[1:0] DAC3 Input mode selection

D3IF Mode	D3IF[1]	D3IF[0]	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified 24bit
2	1	0	N/A
3	1	1	LSB justified 16bit

Note) When DIFS=1, the state is I^2S compatible independently of mode setting,
however D3IF mode should be set to 0. In case of BITCLK48fs then D3IF mode should be set to 0.
BITCLK32fs then D3IFmode should be set to 3.

② D5,D4:D2IF[1:0] DAC2 Input mode selection

D2IF Mode	D2IF[1]	D2IF[0]	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified 24bit
2	1	0	N/A
3	1	1	LSB justified 16bit

Note) When DIFS=1, the state is I^2S compatible independently of mode setting,
however D2IF mode should be set to 0. In case of BITCLK48fs then D2IF mode should be set to 0.
BITCLK32fs then D2IFmode should be set to 3.

③ D3,D2:D1IF[1:0] DAC1 Input mode selection

D1IF Mode	D1IF[1]	D1IF[0]	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified 24bit
2	1	0	N/A
3	1	1	LSB justified 16bit

Note) When DIFS=1, the state is I^2S compatible independently of mode setting,
however D1IF mode should be set to 0. In case of BITCLK48fs then D1IF mode should be set to 0.
BITCLK32fs then D1IFmode should be set to 3.

④ D1:CKS Input clock selection

MCLK		Fs	DFS	DFS[1]	DFS[0]
CKS=0	CKS=1		Mode		
256fs	384fs	8kHz~48kHz	0	0	0
1024fs	1536fs	8kHz~12kHz	1	0	1
256fs	N/A	80kHz~96kHz	2	1	0

When fs:12kHz~8kHz, recommend 1024fs,1536fs.
See system clock section.

⑤ D0: Input always 0

Note) Underlines of the setting of "_" mean default setting.

3) CONT2: SDIN Interface selection and others

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
24h	34h	CONT2	**ISIF[1]**	**ISIF[0]**	**OSIF[1]**	**OSIF[0]**	OUT2E_N	OUT1E_N	**CKSH**	0	0000 0000

① D7,D6:ISIF[1:0] SDIN Input selection

ISIF Mode	ISIF[1]	ISIF[0]	DIFS=0(CONT0 D5)	DIFS=1(CONT0 D5)
0	0	0	Through	Through
1	0	1	MSB justified (24bit)	I^2S compatible
2	1	0	LSB justified 24bit	NOT available
3	1	1	LSB justified 16bit	NOT available

Note) When "Through" is selected at OSIF setting, ISIF settig is also "Through".

This setting can be changed only at system reset state ($\overline{\text{S_RESET}}$ ="L").

When BITCLK is 48fs mode, ISIF mode 2 and 3 can not be used.
When BITCLK is 32fs mode, ISIF mode 1 and 2 can not be used.

② D5,D4:OSIF[1:0] SDIN conversion

OSIF Mode	OSIF[1]	OSIF[0]	DIFS=0(CONT0 D5)	DIFS=1(CONT0 D5)
0	0	0	Through	Through
1	0	1	MSB justified (24bit)	I^2S compatible
2	1	0	LSB justified 24bit	NOT available
3	1	1	LSB justified 16bit	NOT available

Note) When "Through" is selected at ISIF setting, OSIF setting is also "Through".
The conversion time is 1 LRCLK, when mode 1,2 or 3 is selected.
Pay attention to "Delay time (tSISO)", when it use SDATO1 or SDATO2 at "Through" selected.
This setting can be changed only at system reset state ($\overline{\text{S_RESET}}$ ="L").
When BITCLK is 48fs mode, OSIF mode 2 and 3 can not be used.
When BITCLK is 32fs mode, OSIF mode 1 and 2 can not be used

③ D3:OUT2E_N SDATO2 output selection

0: SDATO2 normal output
1: "L" level output
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

④ D2:OUT1E_N SDATO1 output selection

0: SDATO1 normal output
1: "L" level output
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

⑤ D1:CKSH Input clock selection

0: Normal operation
1: Use 1/2 divided MCLK
When CKSH=1 selected, input clock is as following.
This setting can be changed only at system reset state ($\overline{\text{S_RESET}}$ ="L")

DFS mode	DFS[1]	DFS[0]	Fs	MCLK	
				CKS=0	CKS=1
0	0	0	fs=48kHz~8kHz	512fs	768fs
1	0	1	fs=12kHz~8kHz	2048fs	3072fs

In detail, see (4) system clock explanation.

⑥ D0: Input always 0

Note) Underlined settings of ①~⑤ = default setting.

4) CONT3:ADC1 control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
26h	36h	CONT3	ASEL1[2]	ASEL1[1]	ASEL1[0]	SWA1	SWI1	PSAD1	**TEST**	0	0000 0000

① D7,D6,D5: ASEL1[2:0] ADC1 Input selector setting

ASEL1[2]	ASEL1[1]	ASEL1[0]	Analog input pin
0	0	0	AINL1-,AINL1+,AINR1-,AINR1+
0	0	1	AINL3,AINR3
0	1	0	AINL4,AINR4
0	1	1	AINL5,AINR5
1	0	0	AINL6,AINR6
1	0	1	AINL7,AINR7
1	1	0	AINL8,AINR8
1	1	1	AINL9,AINR9

② D4: SWA1 ADC SDATA output selection (see [3. Block diagram])

0: Select SDATA output of ADC1
1: Select SDATA output of ADC2
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

③ D3: SWI1 ADC SDATA output selection (see [3.Block diagram])

0: Normal operation (select SDATA selected by SWA1)
1: Select SDIN
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

④ D2:PSAD1 ADC1 power save

0:Normal operation
1:ADC1 power saves

In the case of not using ADC1, set this value to "1" and ADC1 will be in RESET.
This is useful for reducing power consumption.
(The digital output signals of ADC1 will be 000000h.)
When changing to normal operation, set this value to "0" at system reset.

⑤ D1:TEST

0: Normal operation
1: TEST mode (Do not use this mode)

⑥ D0: Input always 0

Note) Underlined settings of ①~⑤ = default setting.

5) CONT4:ADC2 control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
28h	38h	CONT4	ASEL2[2]	ASEL2[1]	ASEL2[0]	SWA2	SWI2	PSAD2	**TEST**	0	0000 0000

① D7,D6,D5: ASEL2[2:0] ADC2 Input selector setting

ASEL2[2]	ASEL2[1]	ASEL2[0]	Analog input pin
0	0	0	AINL2-,AINL2+,AINR2-,AINR2+
0	0	1	AINL3,AINR3
0	1	0	AINL4,AINR4
0	1	1	AINL5,AINR5
1	0	0	AINL6,AINR6
1	0	1	AINL7,AINR7
1	1	0	AINL8,AINR8
1	1	1	AINL9,AINR9

② D4:SWA2 ADC SDATA output selection (see [3. Block diagram])

0: Select SDATA output of ADC2
1: Select SDATA output of ADC1
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

③ D3:SWI2 ADC SDATA output selection (see [3. Block diagram])

0: Normal operation (select SDATA selected by SWA2)
1: Select SDIN
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

④ D2:PSAD2 ADC2 power save

0:Normal operation
1:ADC2 power save

In the case of not using ADC2, set this value to "1" and ADC2 will be in RESET.
This is useful for reducing power consumption.
(The digital output signals of ADC2 will be 000000h.)
When changing to normal operation, set this value to "0" at system reset.

⑤ D1:TEST

0: Normal operation
1: TEST mode (Do not use this mode)

⑥ D0: Input always 0

Note) Underlined settings of ①~⑤ = default setting.

6) CONT5:DAC control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
2Ah	3Ah	CONT5	SMUTE	**SF1**	**SF0**	**DAF**	PSDA3	PSDA2	PSDA1	0	0000 0000

① D7:SMUTE SMUTE selection

0: Normal operation

1: SMUTE

This register works same as SMUTE pin.

When using this register for soft mute control, the SMUTE pin should be set to "L".

When using the SMUTE pin for soft mute control, this register(D7) should be set to 0.

② D6,D5:SF1,SF0 soft mute cycle time setting

SF mode	SF1	SF0	
0	0	0	1008 LRCLK cycles
1	0	1	4032 LRCLK cycles
2	1	0	504 LRCLK cycles
3	1	1	2016 LRCLK cycles

This setting can be changed only at system reset state ($\overline{\text{S_RESET}}$ ="L").

③ D4: DAF DAC section digital filter selection (See [7. 4-2) Digital filter characteristics])

0: Normal operation

1: Change DA Digital Filter

When DFS mode select 1 consist of CONT0: D7 and D6, this register should set 1.

This setting can be changed only at system reset state ($\overline{\text{S_RESET}}$ ="L").

④ D3:PSDA3 DAC3 power save

0:Normal operation

1:DAC3 power save

In the case of not using DAC3, set this value to "1" and DAC3 will RESET.

This can be useful for reducing power consumption.

When changing to normal operation, set this value to "0" at system reset.

⑤ D2:PSDA2 DAC2 power save

0:Normal operation

1:DAC2 power save

In the case of not using DAC2, set this value to "1" and DAC2 will RESET.

This can be useful for reducing power consumption.

When changing to normal operation, set this value to "0" at system reset.

⑥ D1:PSDA1 DAC1 power save

0:Normal operation

1:DAC1 power save

In the case of not using DAC1, set this value to "1" and DAC1 will RESET.

This can be useful for reducing power consumption.

When changing to normal operation, set this value to "0" at system reset.

⑦ D0: Input always 0

Note) Underlined settings of ①~⑥ = default setting.

7) CONT6 : Internal path setting (see [3. Block diagram])

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
2Ch	3Ch	CONT6	SWAA3	SWD3	SWAA2	SWD2	SWAA1	SWD1	**TEST**	0	0000 0000

① D7:SWAA3

0: Select SDATA of ADC1
1: Select SDATA of ADC2
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

② D6:SWD3

0: Normal operation (Select SDATAI3)
1: Select SDATA of ADC that selected by SWAA3
(DAC input and ADC output format should be selected correct setting.)
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

③ D5:SWAA2

0: Select SDATA of ADC1
1: Select SDATA of ADC2
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

④ D4:SWD2

0: Normal operation (Select SDATAI2)
1: Select SDATA of ADC that selected by SWAA2
(DAC input and ADC output format should be selected correct setting.)
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

⑤ D3:SWAA1

0: Select SDATA of ADC1
1: Select SDATA of ADC2
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

⑥ D2:SWD1

0: Normal operation (Select SDATAI1)
1: Select SDATA of ADC that selected by SWAA1
(DAC input and ADC output format should be selected correct setting.)
This register is changed at rising edge of the LRCLK (falling edge at I^2S mode.).

⑦ D1:0 TEST

0: Normal operation
1: TEST mode (Do not use this mode)

⑧ D0: Input always 0

Note) Underlined settings of ①~⑦ = default setting.

(2) Power supply startup sequence

When it starts power supply for the AK4591, its setting should be $\overline{\text{INIT_RESET}}$ = "L" and $\overline{\text{S_RESET}}$ = "L" (initial reset). Then all control registers are initialized to default values by $\overline{\text{INIT_RESET}}$ ="L". The VREF (Analog reference level) of the AK4591 is set by setting the $\overline{\text{INIT_RESET}}$ rise to "H".

Normally, $\overline{\text{INIT_RESET}}$ sequence is executed when power is applied to the device.

By the time of the $\overline{\text{S_RESET}}$ sets "H" (release system reset), the AK4591 requires stable the system clocks (MCLK, LRCLK and BITCLK).

However, CLKO(, CLKO1, CLKO2), BITCLK(_O) and LRCLK(_O) of the AK7750 or the AK7730 can connects AK4591 and control $\overline{\text{S_RESET}}$ in common with them. (After release of $\overline{\text{S_RESET}}$, all output clock enable is required.). Except for the slave mode of the AK7730, these 3 clocks (CLKO(,CLKO1, CLKO2), BITCLK(_O) and LRCLK(_O)) do not rise up stably by the release of $\overline{\text{S_RESET}}$. It is no problem because internal reset of the AK4591 is done after these clocks are stably supplied. After operation has begun, do not stop supplying clock except during reset state.

Also, VREF needs to rise up stably before $\overline{\text{S_RESET}}$ sets to "H". The stable time of the VREF depends on the capacitors attached with VCOM. In case of using 0.1μF and 10μF capacitors, it takes about 10ms.

The AK4591 does not need system clocks (MCLK, LRCLK and BITCLK) at reading or writing its control registers.

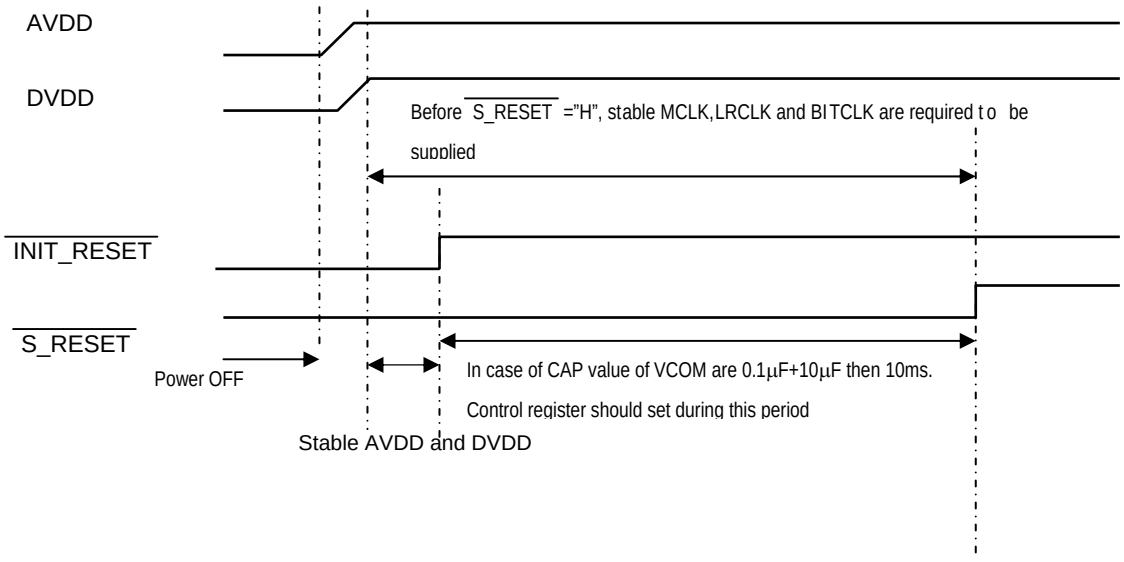
However, we can not recommend writing or reading during states that system clocks are changing to avoid influences of noise.

The control registers should be changed in the stable system clock state.

The initial setting of the control registers should be in system reset state ($\overline{\text{INIT_RESET}}$ ="H" and $\overline{\text{S_RESET}}$ ="L"). Some registers can be set at run time, it comes out click noise in some case.

Note Do not stop the system clock (MCLK, LRCLK, BITCLK) except when $\overline{\text{INIT_RESET}}$ ="H" and $\overline{\text{S_RESET}}$ = "L". If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result. In case of changing the system clock, this action is also required.

SMUTE function of the AK4591 is not effective at following state (power up, power down, initial reset, release of initial reset, system reset and system reset release); therefore an external mute circuit in this case is necessary to avoid any click noise.



(3) Resetting

The AK4591 has two reset pins : $\overline{\text{INIT_RESET}}$ and $\overline{\text{S_RESET}}$.

The $\overline{\text{INIT_RESET}}$ pin is used to initialize and set up reference level as shown in " (2) Power supply startup sequence" section.

The system reset state is $\overline{\text{S_RESET}}$ ="L" and $\overline{\text{INIT_RESET}}$ ="H". Normally the control registers set in this state.

During the system reset phase, the ADC and DAC sections are also reset. However, reference levels are active.

The system reset is released by setting $\overline{\text{S_RESET}}$ to "H", and this will activate the internal counter.

When the system reset is released, internal timing will be activated in synchronization with rising edge "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. Therefore LRCLK, BITCLK should stabilize before the system reset release. At run time, fewer than 2 clocks of the phase difference between LRCLK and internal clock (the limit checks both rising and falling phase) can keep normal functions. If the phase difference exceeds the above range, the phase isadjusted by synchronizing the "↑" of LRCLK (when the standard input format is used). This prevents synchronization failure with the external circuit. For some time after returning to the normal state after loss of synchronization, normal data will not be valid.

If the phase difference in LRCLK and internal timing is over the limit, the operation is performed with internal timing remaining unchanged. This is an assist function so that it can not use for clock phase adjustor frequency changing.

It needs system reset $\overline{\text{S_RESET}}$ ="L"(& $\overline{\text{INIT_RESET}}$ ="H") or initial reset $\overline{\text{INIT_RESET}}$ ="L"(& $\overline{\text{S_RESET}}$ ="L"), when it changes regarding clock state. (Ex. master clock, sampling frequency or phase change of MCLK , BITCLK or LRCLK.)

The ADC section can output 530-LRCLK (max) after its internal counter started.

The AK4591 performs normal operation when $\overline{\text{S_RESET}}$ is set to "H".

When initial reset ($\overline{\text{INIT_RESET}}$) and system reset ($\overline{\text{S_RESET}}$) change, the status of DAC section also changes to Power down or Release mode, and may cause a click noise on the output. In this case SMUTE function is not effective, an external mute circuit (in this case) is necessary to avoid any click noise. (It is same case as select power save mode by control register setting.) The digital output from ADC may require also require this same attention.

(4) System clock

The required system clock is MCLK (256fs or 384fs @48kHz), LRCLK (fs) and BITCLK (64fs or 48fs, 32fs (with conditions attached)). The master clock (MCLK) and LRCLK must be synchronized, but the phase is not critical. LRCLK corresponds to the standard digital audio rate (8 kHz ~ 96 kHz).

■ CKSH=0 (CKSH:CONT2 D1)

Fs	MCLK (Master clock)				BITCLK
256fs		384fs	1024fs	1536fs	64fs
	CKS=0	CKS=1	CKS=0	CKS=1	
8kHz	(2.048MHz)	(3.072MHz)	8.192MHz	12.288MHz	512kHz
12kHz	(3.072MHz)	(4.608MHz)	12.288MHz	18.432MHz	768kHz
16kHz	4.096MHz	6.144MHz	-	-	1.024MHz
24kHz	6.144MHz	9.216MHz	-	-	1.536MHz
32kHz	8.192MHz	12.288MHz	-	-	2.048MHz
44.1kHz	11.2896MHz	16.9344MHz	-	-	2.8224MHz
48kHz	12.288MHz	18.432MHz	-	-	3.072MHz
96kHz	24.576MHz	-	-	-	6.144MHz

Note) - : invalid

When Fs mode is 8kHz or 12kHz, 1024fs or 1536fs is recommended.

■ CKSH=1 (CKSH:CONT2 D1)

Fs	MCLK (Master clock)				BITCLK
	512fs	768fs	2048fs	3072fs	64fs
	CKS=0	CKS=1	CKS=0	CKS=1	
8kHz	(4.096MHz)	(6.144MHz)	16.384MHz	24.576MHz	512kHz
12kHz	(6.144MHz)	(9.216MHz)	24.576MHz	-	768kHz
16kHz	8.192MHz	12.288MHz	-	-	1.024MHz
24kHz	12.288MHz	18.432MHz	-	-	1.536MHz
32kHz	16.384MHz	24.576MHz	-	-	2.048MHz
44.1kHz	22.5792MHz	-	-	-	2.8224MHz
48kHz	24.576MHz	-	-	-	3.072MHz
96kHz	-	-	-	-	-

Note) - : invalid

When Fs mode is 8kHz, 2048fs or 3072fs is recommended. When Fs mode is 12kHz, 2048fs is recommended.

(5) Audio data interface

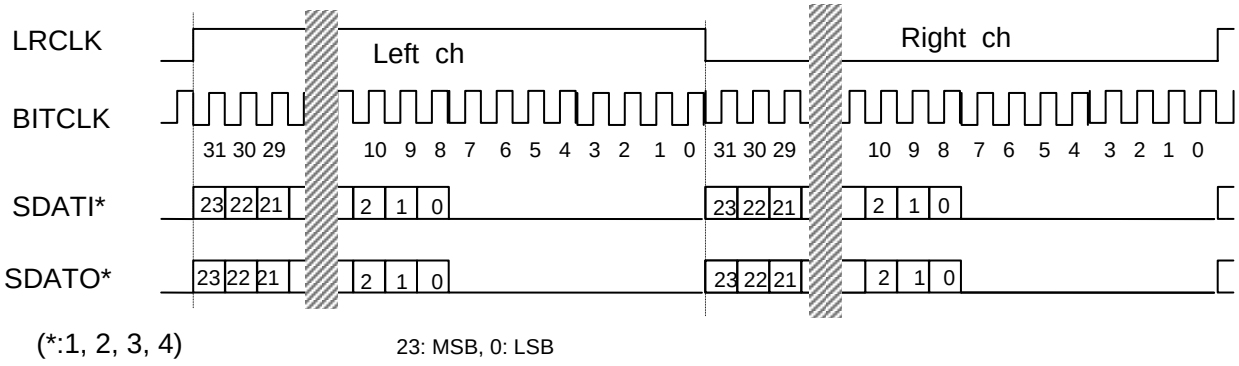
5-1) SDATI1,SDATI2,SDATI3,SDATO1,SDATO2 (BITCLK64fs)

The serial audio data pins SDATI1, SDATI2, SDATI3, SDATO1 and SDATO2 are interfaced with the external system, using LRCLK and BITCLK. The data format is MSB-first 2's complement.

5-1-a) AKM Standard format (CONT0 : DIFS=0)

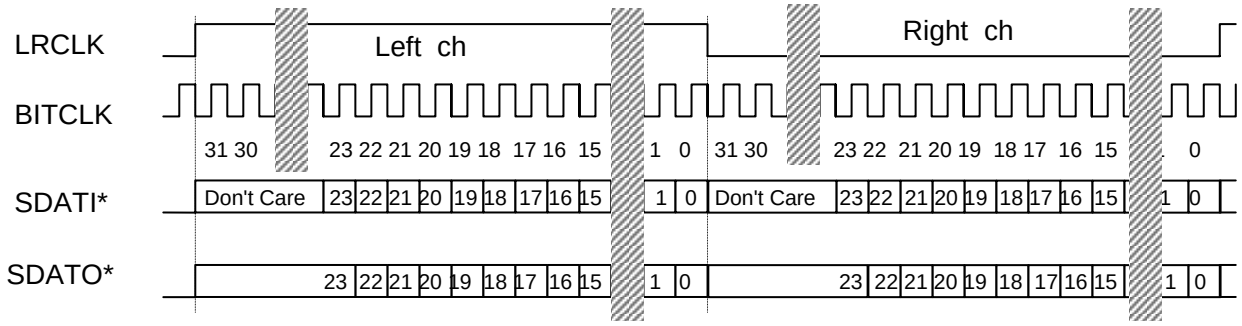
The input and output format of the AK4591 can be seteach port independently by control register settings when BITCLK is 64fs. Default setting is MSB justified(24bit). It can correspond to LSB justified 24bit and 16bit.
(See [8. (1) control register setting] section in detail.)
If BITCLK=48fs, interface format should be set to MSB justified 24bit.

(1) Mode 0 MSB justified 24bit



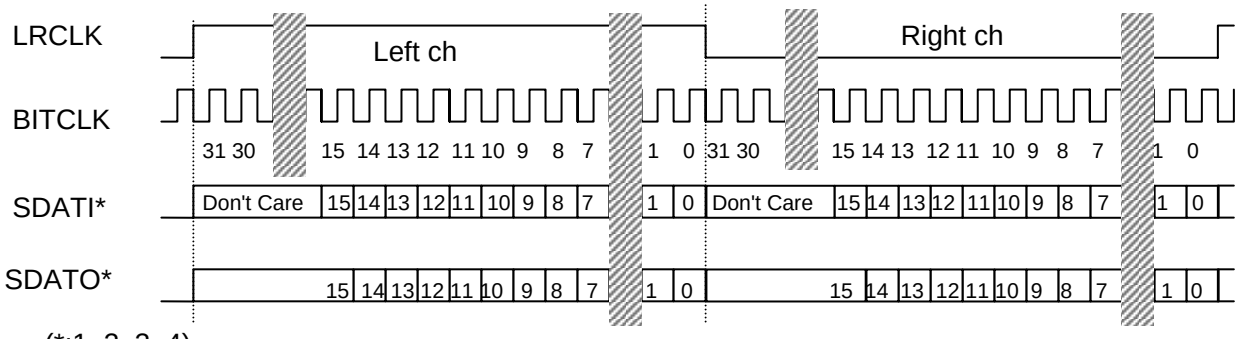
(*:1, 2, 3, 4) 23: MSB, 0: LSB

(2) Mode 1 LSB justified 24bit



(*:1, 2, 3, 4) 23: MSB, 0: LSB

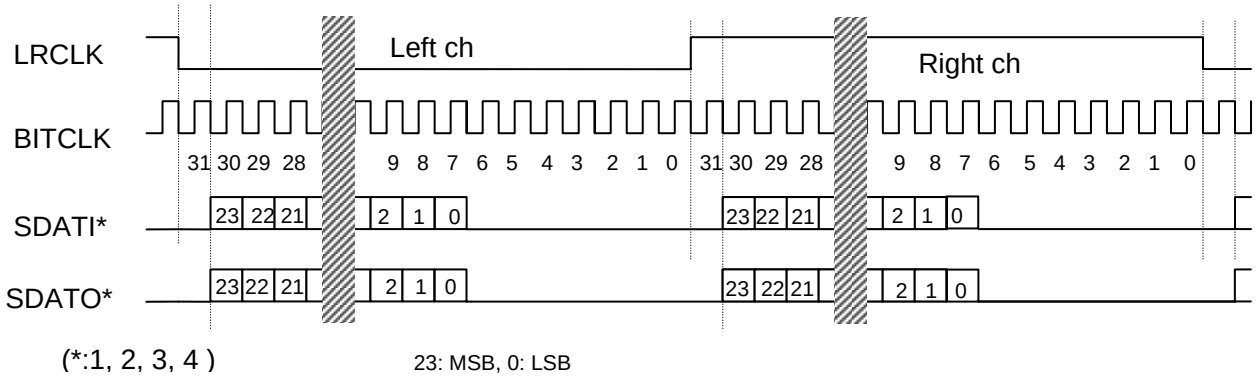
(3) Mode 3 LSB justified 16bit



(*:1, 2, 3, 4) 15: MSB, 0: LSB

5-1-b) I²S compatible (CONT0 : DIFS=1)

The data format is MSB-first 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to I²S compatible mode by setting the control register "CONT0 DIFS (D5) to 1". (In this case, all input/output audio data pin interface are in I²S compatible mode.)



5-2) SDIN (BITCLK64fs)

The serial audio pin (SDIN) can be used when SDATO1 or SDATO2 are not used as output ofthe ADC serial data. (See [3.Block diagram] or [8. Fuction description (1) control registers setting].)

By setting of the control registers, input data of the SDIN can output to SD ATO1 or SD ATO2 through or w ith serial data conversion. When it uses serial data conversion, it takes 1/fs (μs).

5-3) BITCLK48fs,BITCLK32fs

AK4591 can use 48fs and 32fs BITCLK, however, all audio interface should be set to 48fs or 32fs.
So, the control register should set as following.

5-3-a) BITCLK48fs

CONT0 D5:DIFS=0, D4,D3:A2IF[1:0]=00 D2,D1:A1IF[1:0]=00
CONT1 D7,D6:D3IF[1:0]=00, D5,D4:D2IF[1:0]=00, D3,D2:D1IF[1:0]=00,
CONT2 (D7,D6:ISIF[1:0]=00,D5,D4:OSIF[1:0]=00) or (D7,D6:ISIF[1:0]=01,D5,D4:OSIF[1:0]=01)

5-3-b) BITCLK32fs

CONT0 D5:DIFS=0, D4,D3:A2IF[1:0]=00 D2,D1:A1IF[1:0]=00
CONT1 D7,D6:D3IF[1:0]=11, D5,D4:D2IF[1:0]=11, D3,D2:D1IF[1:0]=11,
CONT2 (D7,D6:ISIF[1:0]=00,D5,D4:OSIF[1:0]=00) or (D7,D6:ISIF[1:0]=11,D5,D4:OSIF[1:0]=01)

(6) Interface with microcomputer

The microcomputer interface uses 4 control pins; $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input CLocK), SI (Serial data Input) and SO (Serial data Output). $\overline{CS}$ (ChipSelect Bar) can use if required.

When the AK4591 needs to transfer data to the micro controller, it starts by $\overline{RQ}$ going "L". The AK4591 reads SI data at the rising point of SCLK, and outputs to SO at the falling point of SCLK.
The AK4591 accepts first data as command then sets register when writing mode. When reading mode, at first sends a command data then send 8-bit of zero data on SI and read at SO line.

When $\overline{RQ}$ changes to "H", one command has finished. New command requests must set $\overline{RQ}$ to "L" again.

The command code of the AK4591 is assigned from 20h to 3Fh.

When $\overline{CS}$ ="H", SI is not active and SO becomes Hi-z. (When $\overline{CS}$ ="L" and $\overline{RQ}$ ="H", SI is not active but SO is not Hi-z.)

The initial setting of the control registers should be done at system reset state ($\overline{S_RESET}$ ="L" and $\overline{INIT_RESET}$ ="H"). It does not need sy stem clock (MCLK , LRCLK and BITCLK) for reading and w riting its control registers.

However, do not read or write during unstable system clock state to avoid influence of noise. It should be done in stable system clock state. Some register can be changed at run time, but may cause a click noise in some cases.

To avoid outer noise effects during no communications with micro controller, the interface pins should be set to the following states, $\overline{RQ}$ ="H",SCLK="H" and SI="L". (Regarding $\overline{CS}$, use properly case by case.)

6-1) WRITE(Control register setting)

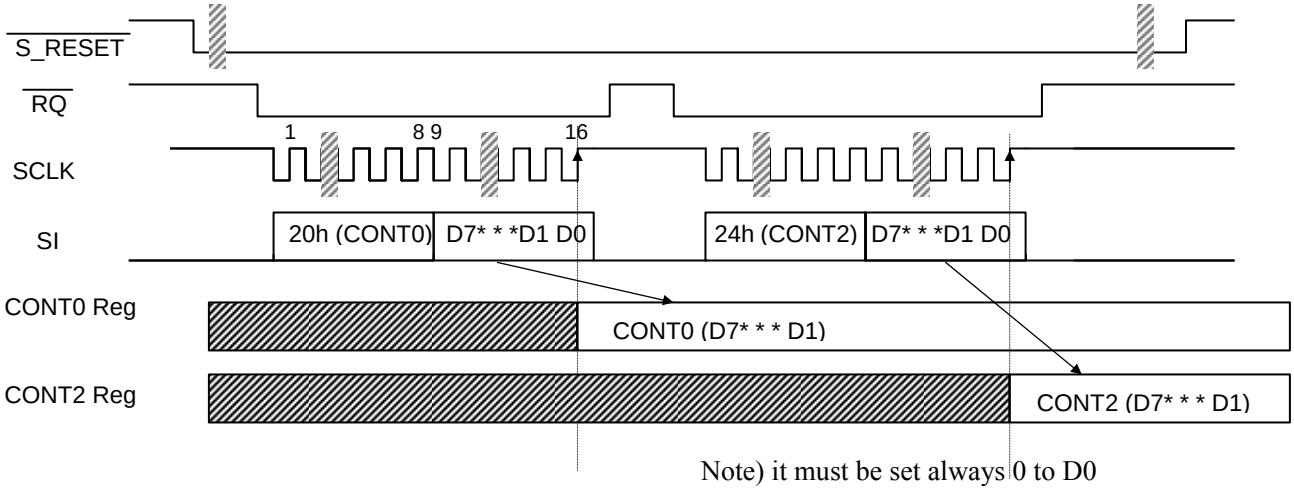
The data is comprised of 2 bytes (16bit) used to perform control register write operations. When all data has been entered, the new data is sent at the rising edge of the 16th count of SCLK.

Data transfer procedure

① Command code 20h,22h,24h,26h,28h,2Ah,2Ch(,2Eh)
② Control data (D7 D6 D5 D4 D3 D2 D1 D0)

Note) 2Eh is TEST use only.

For the function of each bit, see the description of Control registers, (see [8. Function description (1) control registers setting]).



Control Registers write operation (example)

During RUN phase the timing is same as upper except for $\overline{\text{S_RESET}}$ ="H".

6-2) READ (check the control registers)

To read data written into the control registers, input the command code and 16 bits of SCLK. After the input command code, the data of D 7 to D 1 outputs from SO is synchronized with the falling edge of SCLK. D0 bit is invalid, so please ignore this bit.

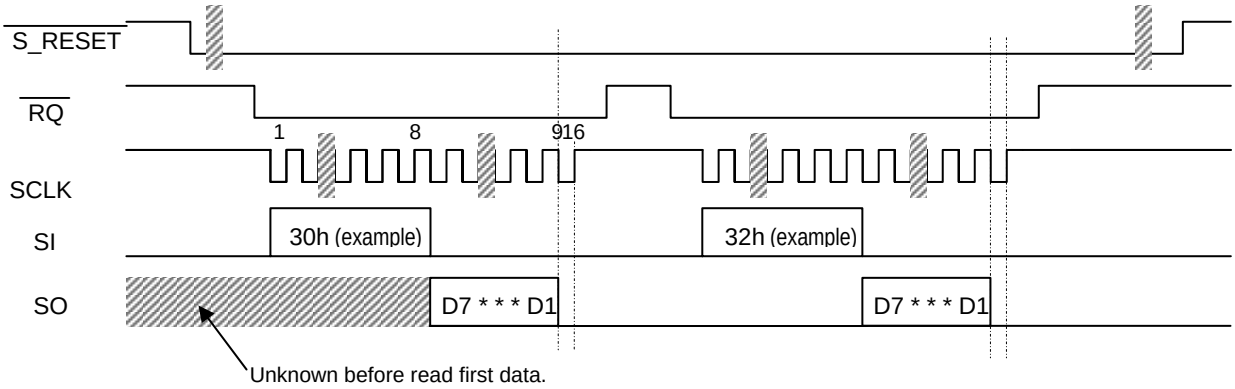
All register can read even in RUN phase ($\overline{\text{S_RESET}}$ ="H").

Data transfer procedure

① Command code	30h,32h,34h,36h,38h,3Ah,3Ch(,3Eh)
②	(0 0 0 0 0 0 0 0)

Note) 3Eh is TEST use only.

For the function of each bit, see the description of Control registers,
(see [8. Function description (1) control register setting]).



Control Register data read operation. When RUN phase $\overline{\text{S_RESET}}$ ="H"

(7) ADC section high-pass filter

The AK4591 incorporates a digital high-pass filter (HPF) for canceling DC offset in the ADC section. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

96kHz		48kHz	44.1kHz 32k	Hz	8kHz
Cut-off frequency	1.86Hz	0.93Hz	0.86Hz	0.62Hz	0.16Hz

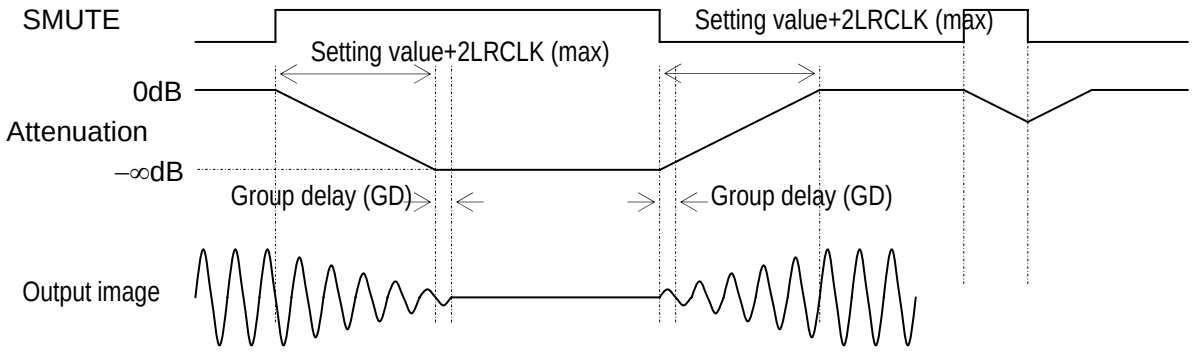
(8) Soft mute operation of DAC section

Soft mute operation is performed in the digital domain of DAC1, DAC2 and DAC3. When SMUTE pin goes to "H" or sets SMUTE=1 of the control register CONT5, the signal is attenuated to -∞dB during the time that is set by control registers SF1 and SF0 of CONT5 + 2LRCLK (max) cycles. (When SF1=0 and SF0=0, attenuation time is 1008(min) to 1010(max) LRCLK.)
When SMUTE is returned to "L", the mute is cancelled and output attenuation gradually changes to 0dB during the time that is set by control registers. If the soft mute is cancelled within the setting time after starting the operation, the attenuation is discontinued and returned to 0dB.
(SMUTE function can set both the SMUTE pin and control register setting. See block diagram.)
The soft mute is enable at $\overline{\text{S_RESET}}$ is "H". (DAC section during RUN phase)

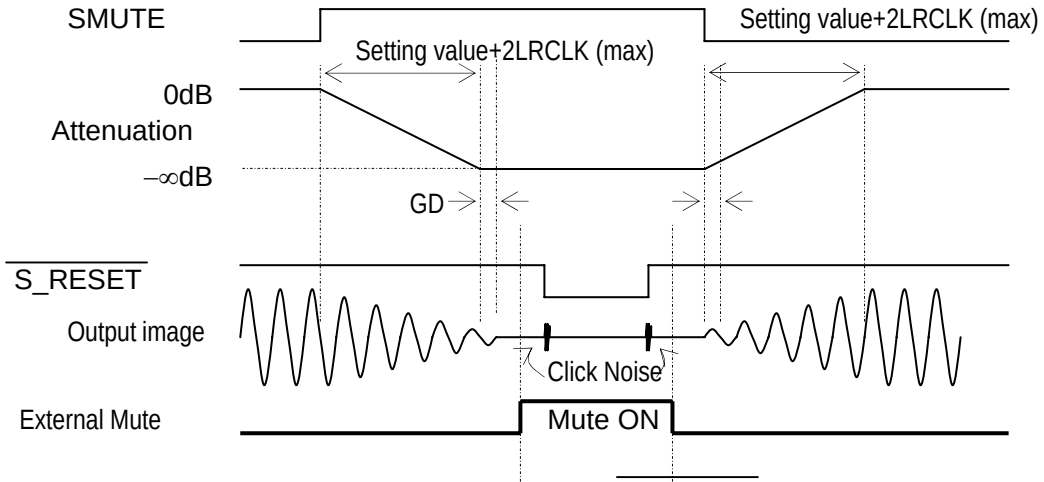
After attenuated to - ∞dB(0), it may make a click noise when the release operation of system reset ($\overline{\text{S_RESET}}$ ="L").

Because of the DAC sections change to reset phase. However, the attenuation value does not initialize by $\overline{\text{S_RESET}}$.

Only $\overline{\text{INIT_RESET}}$ set to "L" can initialize this value.



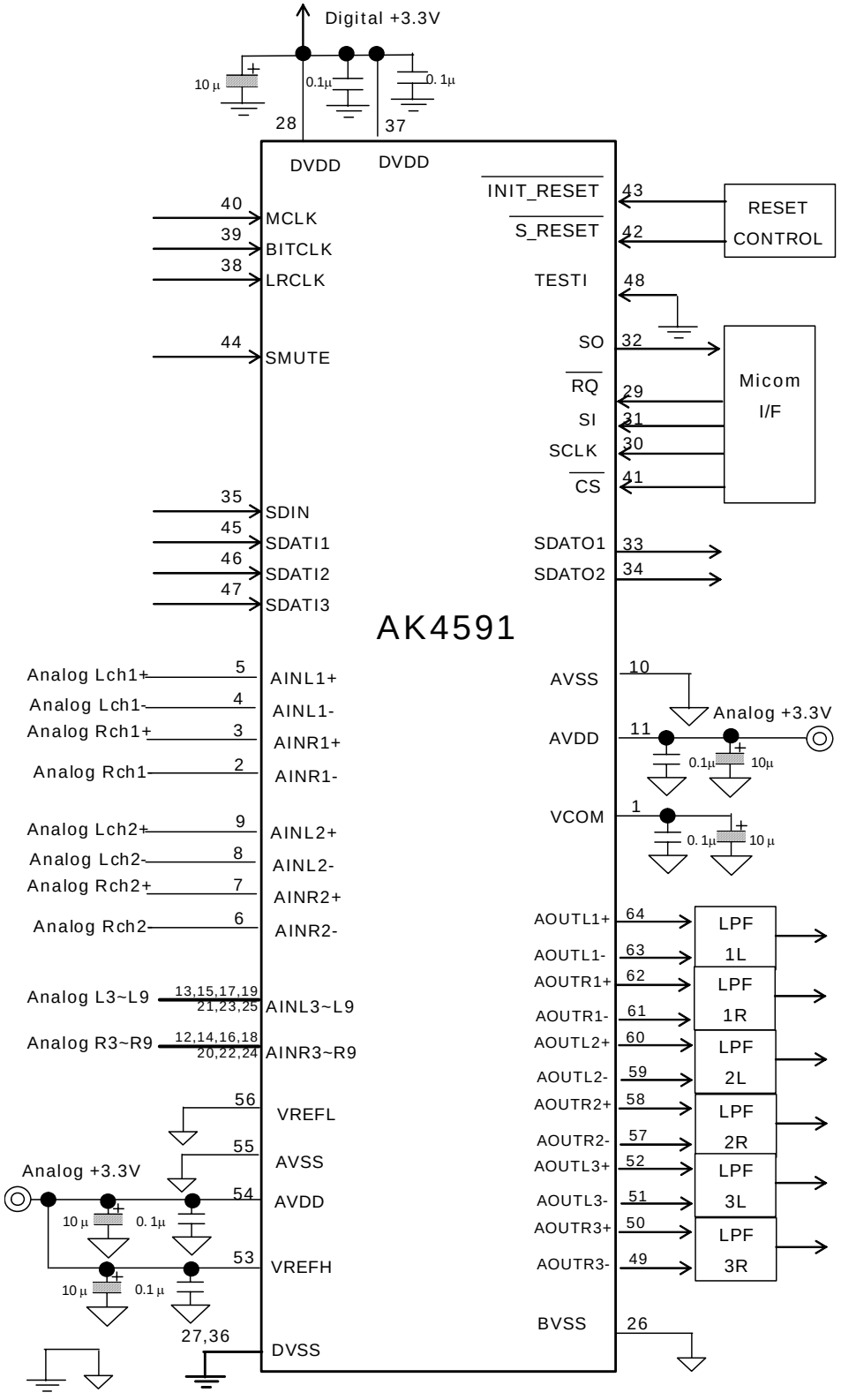
Soft mute function (SMUTE pin)



Soft mute example during $\overline{\text{S_RESET}}$ ="L"

9. System Design

(1) Connection example



(2) Peripheral circuit

2-1) Ground and power supply

To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK4591. System analog power is supplied to AVDD. Generally, the power supply and ground wires must be connected separately for the analog and digital sections. Connect them at a position close to the power source on the PC board. Decoupling capacitors and small ceramic capacitors should be connected as close as possible to the AK4591.

2-2) Reference voltage

The input voltage difference between the VREFH pin and the VREFL pin determines the full scale of analog input and analog output. Normally, connect VREFH to AVDD and connect VREFL to AVSS. To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between VREFH and AVSS. The ceramic capacitor in particular should be connected as close as possible to the pin. To avoid coupling to the AK4591, digital signals and clock signals should be kept away as far as possible from the VREFH and the VREFL pin.

VCOM is used as the common voltage of the analog signal. To reduce high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor should be connected as close as possible to the pin. Do not draw current from the VCOM pin.

2-3) Analog input

Analog input signals are applied to the modulator through the differential input pins or single-ended pins of each channel selected by the input selector. When using the differential inputs, this voltage is equal to the differential voltage between AIN+ and A IN- (ΔVAIN= (AIN+)-(AIN-)), and the input range is ±FS= ± (VREFH-AVSS) × (2.0/3.3). When VREFH = 3.3V and AVSS = 0V, the input range is within ±2.0Vpp. When using single-ended inputs, this input range is FS = (VREFH-AVSS) × (2.0/3.3). When VREFH = 3.3V and AVSS = 0V, the input range is within 2.0Vpp the output code format is given in terms of 2's complements.

The analog source voltage to the AK4591 is +3.3V (Typ.). Voltage of AVDD+0.3V or more, voltage of AVSS-0.3V or less, and current of 10 mA or more must not be applied to analog input pins (AINL1+,AINL1-,AINR1+,AINR1-,AINL2+,AINL2-,AINR2+,AINR2-AINL3~L9,AINR3~R9,VREFH,VREFL) Excessive current will damage the internal protection circuit and will cause latch-up, thereby damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15 V, the analog input pins must be protected from high-voltage signals.

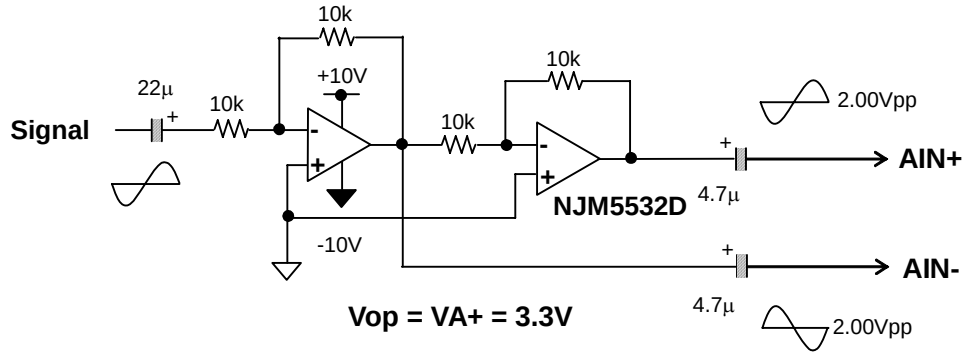


Fig. 1 Example of input buffer circuit (differential input)

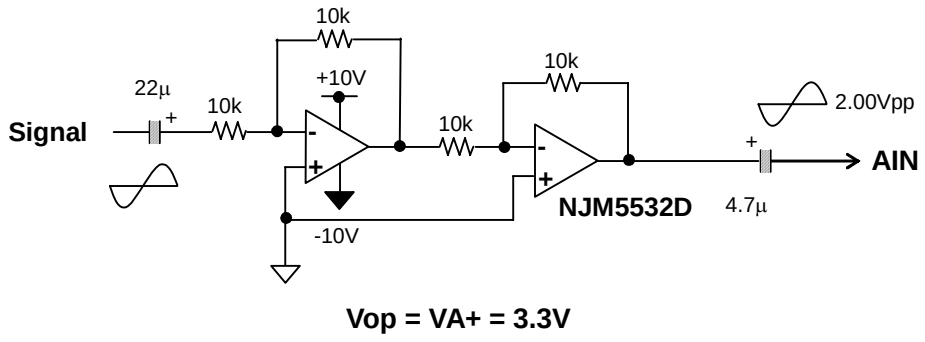


Fig. 2 Example of input buffer circuit (single ended input)

After release of the $\overline{\text{INIT_RESET}}$ pin, the AK4591 makes internal center level as AVDD/2 for the ADC, so do NOT input AC signal to the analog input pins of the AK4591 during the initial reset state (AINL1+, AINL1-, AINR1+, AINR1-, AINL2+, AINL2-, AINR2+, AINR2-, AINL3~L9 ,AINR3~R9) in case of removing DC level as upper example.

2-4) Analog output

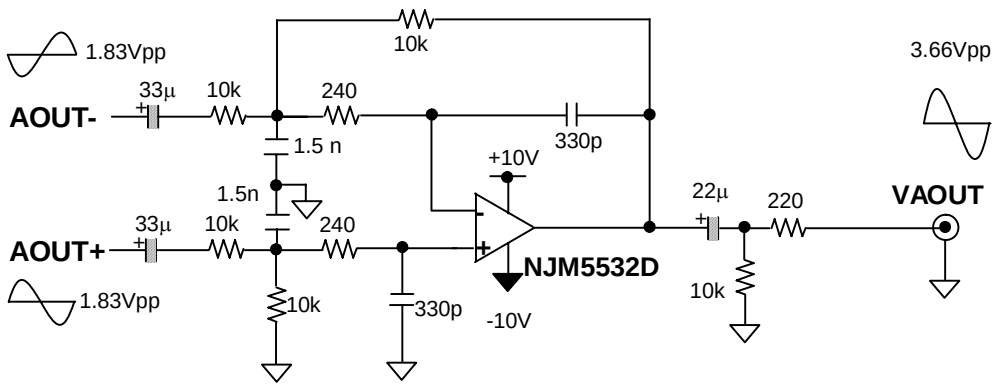


Fig.3 Example of output LPF circuit

The analog outputs are full differential outputs and nominally ±1.83Vpp (typ @ VRDAH=3.3V) centered in the internal com mon voltage about (AVDD/2). The di fferential outputs are sum med externally, VAOUT= (AOUT+)-(AOUT-) between AOUT+ and AOUT-.

If the summing gain is 1, the output range is VAOUT = 3 .66Vpp (typ@ VRDAH=3.3V). The bias voltage of external summing circuit is supplied externally.

The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal AOUT is 0V for 000000H (@24bit).

The internal switched-capacitor filter and external LPF a ttenuate the noise generated by the delta-sigma modulator beyond the audio pass band.

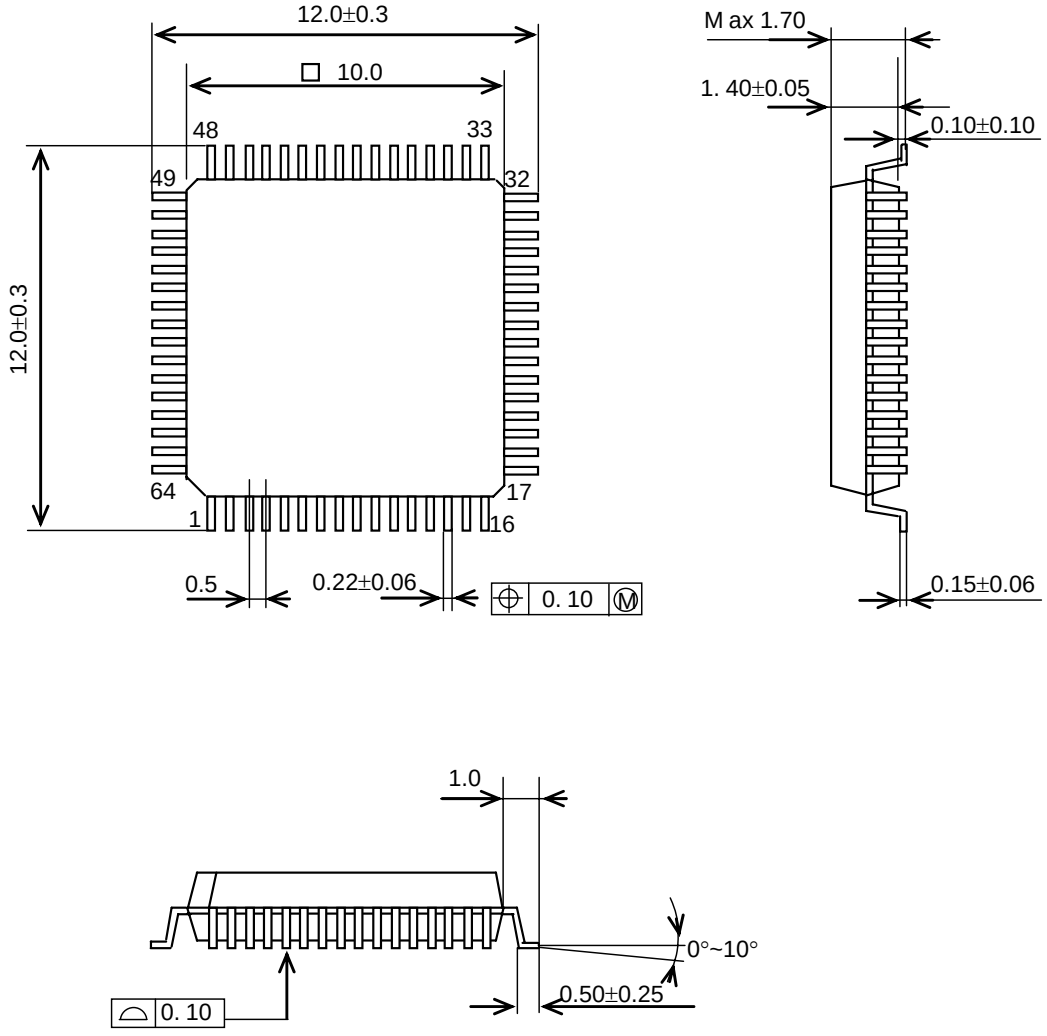
Differential outputs can eliminate few mV+AVDD/2 DC offset on analog outputs with capacitors.
Fig.3 shows the example of external op-amp circuit summing the differential outputs.

2-5) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect low voltage logic to the digital output. The applicable logic family includes the 74LV, 74LV-A, 74ALVC and 74AVC series.

10. Package

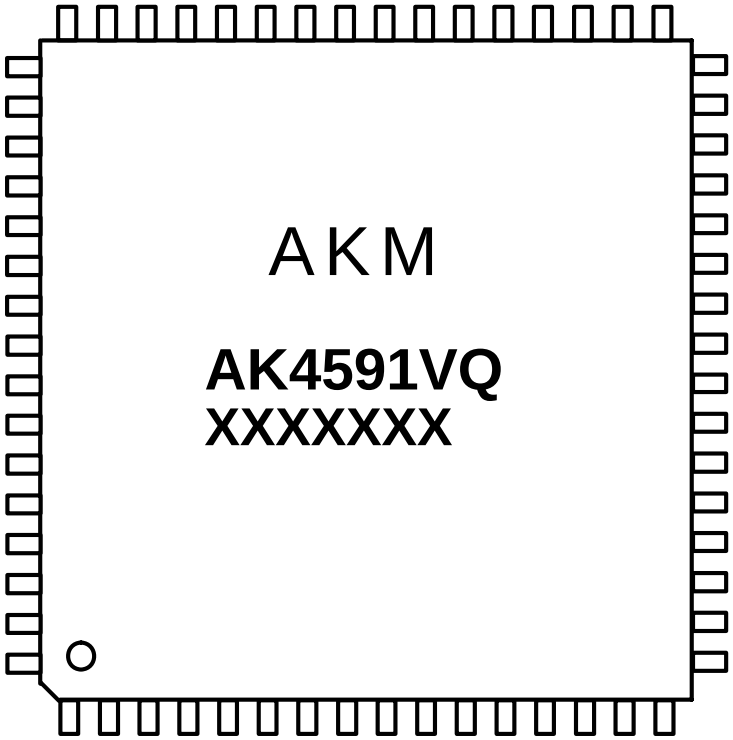
64-pin LQFP (Unit: mm)



- Material & Lead finish

Package:		Epoxy
Lead-fram	e:	Copper
Lead-finish		Soldering (Pb free) plate

11. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4591VQ
4) Asahi Kasei Logo

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
04/03/17 00		First Edition		
12/12/19 01		Specification Change	39 PACKAGE	Package dimensions were changed.

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