AK4616

24bit 3ch/5ch Audio CODEC with Mic Amplifier

GENERAL DESCRIPTION

The AK4616 is a single chip audio CODEC that includes three channel ADCs and five channel DACs. The analog inputs support differential/single-ended with 4:1 stereo selector in front of 2-channel 99dB ADC, and monaural ADC for guidance sound. The high performance 5-channel DAC integrates full-range digital volume control and achieves 105dB dynamic range. A car audio system can be easily designed with an audio DSP and the AK4616. The AK4616 is housed in a space saving 48-pin LQFP package.

FEATURES

- ☐ **2ch ADC**
  - **Sampling Frequency: 8kHz~48kHz**
  - **4 System in / 1 out (Diffrentialx3, single endx1)**
  - **ADC S/N: 99dB, S/ (N+D): 88dB**
  - **I/F format: MSB justified, I^2S or TDM**
- ☐ **1ch ADC for Monaural Audio Input**
  - **Sampling Frequency: 8kHz~48kHz**
  - **ADC S/N: 97dB, S/ (N+D): 87dB**
  - **I/F format: MSB justified, I^2S or TDM**
- ☐ **4ch DAC**
  - **Sampling Frequency: 8kHz~48kHz**
  - **DAC S/N: 105dB, S/ (N+D): 95dB**
  - **I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S or TDM**
- ☐ **Monaural DAC**
  - **Sampling Frequency: 8kHz~48kHz**
  - **DAC S/N: 107dB, S/ (N+D): 100dB**
  - **I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S or TDM**
- ☐ **Microphone Interface**
  - **Differential**
  - **Programmable Gain (+33dB ~ +15dB and 0dB, 3dB step)**
  - **Low Noise Microphone Bias**
- ☐ **Digital Processing**
  - **Individual Channel Independent Digital Volume for DAC (0dB ~ -127dB, 0.5dB step)**
  - **Monaural Audio Input Mixing and Individual Channel Digital Volume for ADC (0dB~-127dB, 0.5dB step)**
  - **Soft mute**
- ☐ **Master Clock**
  - **256fs, 384fs, 512fs**
- ☐ **µP I/F: I^2C-slave**
- ☐ **Power Supply**
  - **Analog Power Supply: A3V31,A3V32 = 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital Power Supply1: D3V3 = 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital Power Supply2: D1V8 = 1.7 ~ 1.9V (typ.1.8V)**
- ☐ **Operating temperature range: -40°C ~ 85°C**
- ☐ **Package: 48-pin LQFP**

■ Block Diagram

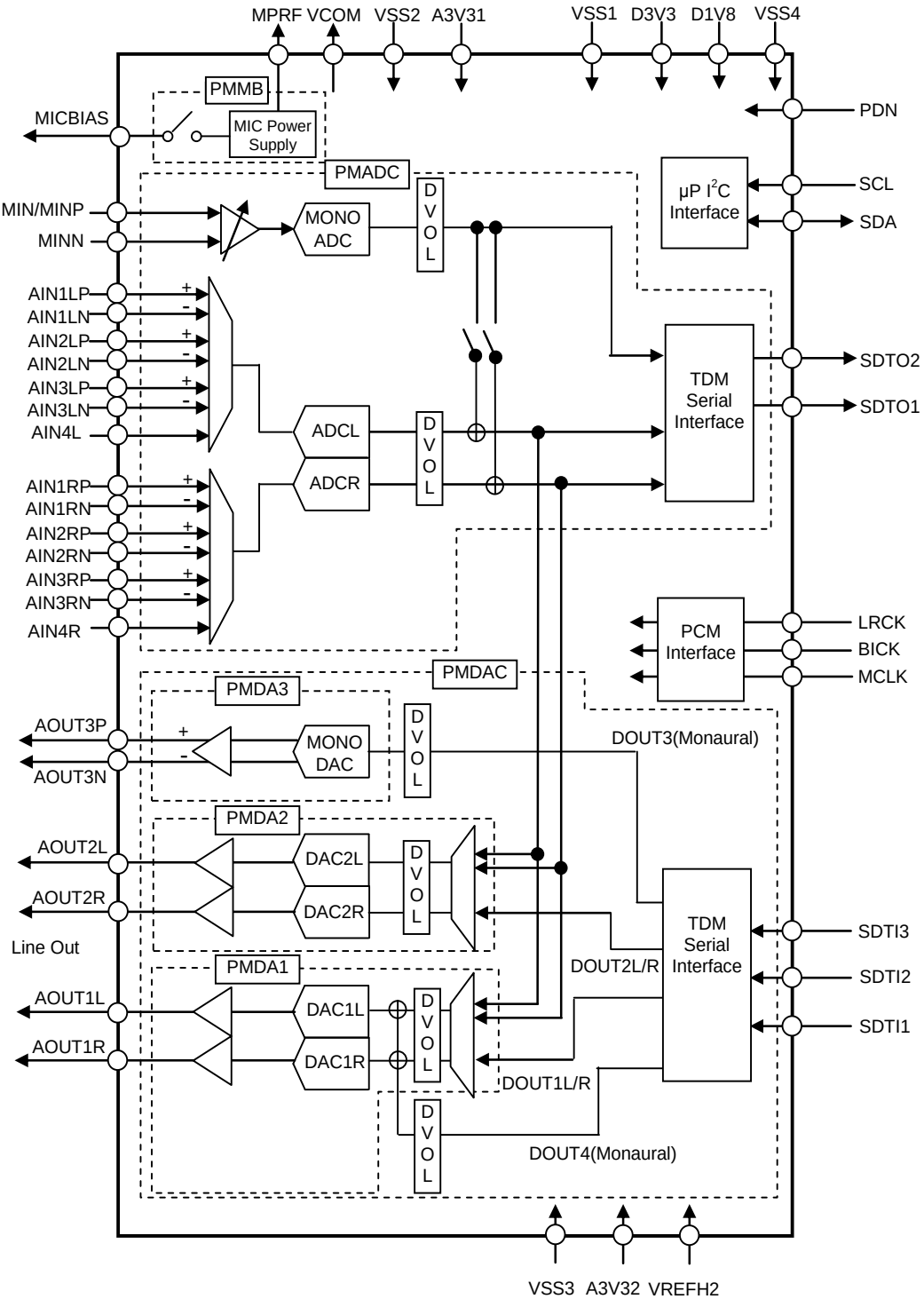
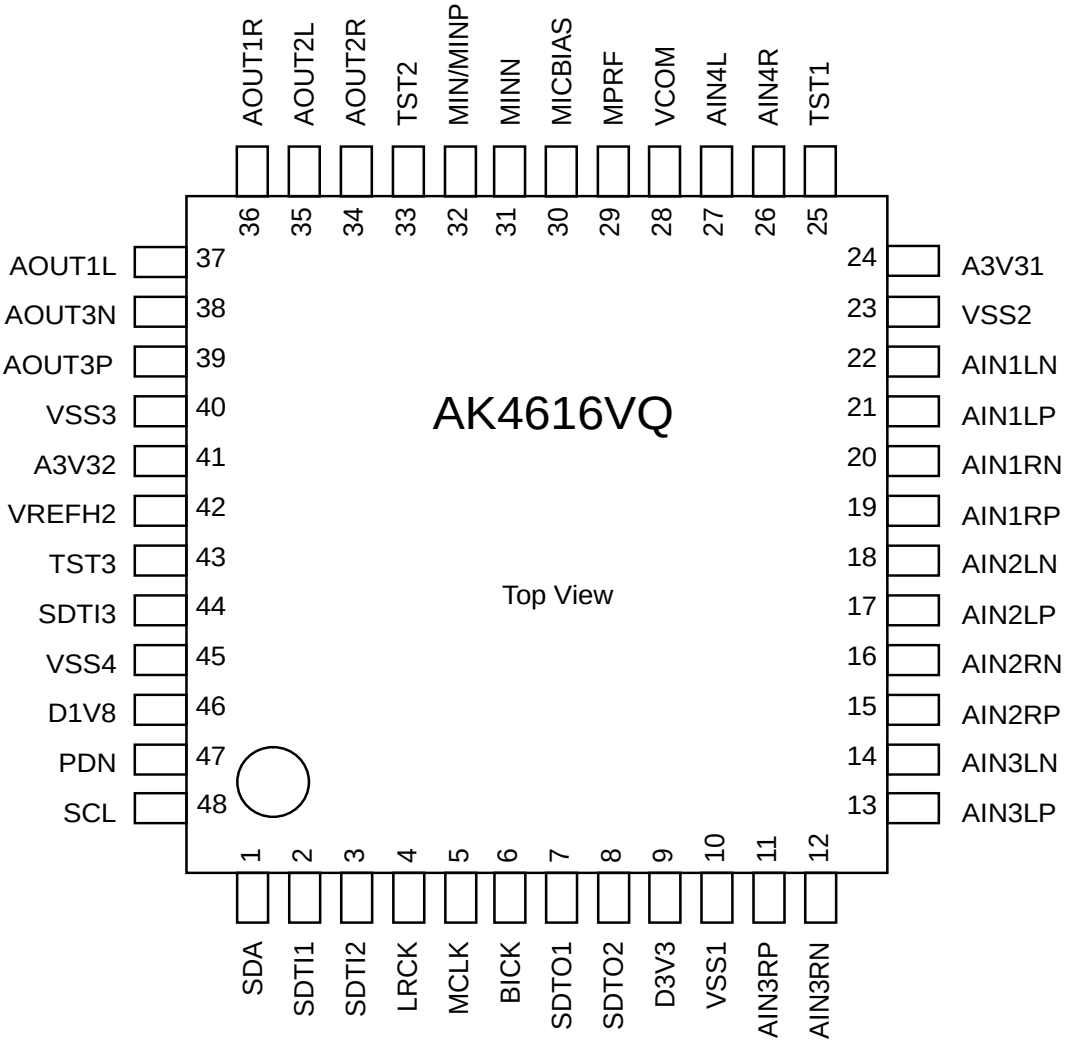


Figure 1. Block Diagram

■ Ordering Guide

AK4616VQ	–40 ~ +85°C	48pin LQFP (0.5mm pitch)
AKD4616	Evaluation Board for AK4616	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDA	I/O	Control Data Input Pin
2	SDTI1	I	Audio Serial Data Input 1 Pin
3	SDTI2	I	Audio Serial Data Input 2 Pin
4	LRCK	I	Input Channel Clock Pin
5	MCLK	I	External Master Clock Input Pin
6	BICK	I	Audio Serial Data Clock Pin
7	SDTO1	O	Audio Serial Data Output 1 Pin
8	SDTO2	O	Audio Serial Data Output 2 Pin
9	D3V3	-	Digital Power Supply Pin, 3.0V~3.6V
10	VSS1	-	Ground Pin, 0V
11	AIN3RP	I	Rch Analog Positive Input 3 Pin
12	AIN3RN	I	Rch Analog Negative Input 3 Pin
13	AIN3LP	I	Lch Analog Positive Input 3 Pin
14	AIN3LN	I	Lch Analog Negative Input 3 Pin
15	AIN2RP	I	Rch Analog Positive Input 2 Pin
16	AIN2RN	I	Rch Analog Negative Input 2 Pin
17	AIN2LP	I	Lch Analog Positive Input 2 Pin
18	AIN2LN	I	Lch Analog Negative Input 2 Pin
19	AIN1RP	I	Rch Analog Positive Input 1 Pin
20	AIN1RN	I	Rch Analog Negative Input 1 Pin
21	AIN1LP	I	Lch Analog Positive Input 1 Pin
22	AIN1LN	I	Lch Analog Negative Input 1 Pin
23	VSS2	-	Ground Pin, 0V
24	A3V31	-	Analog Power Supply Pin, 3.0V~3.6V
25	TST1	-	This pin must be connected to A3V31 pin.
26	AIN4R	I	Rch Analog Input 4 Pin
27	AIN4L	I	Lch Analog Input 4 Pin
28	VCOM	O	Common Voltage Output Pin, A3V31x1/2 Large external capacitor around 1μF is used to reduce power-supply noise.
29	MPRF	O	Output Pin for Ripple Filter of MICBIAS Circuit Connect 1.0μF capacitor to VSS2. Outputs A3V31 during initial reset.
30	MICBIAS	O	Microphone bias. Outputs Hi-Z during initial reset.
31	MINN	I	Microphone Negative input pin (MDIF bit = "1")
32	MIN	I	Single-ended Analog Input pin (MDIF bit = "0")
	MINP	I	Microphone Positive input pin (MDIF bit = "1")
33	TST2	-	This pin must be connected to VSS3 pin.
34	AOUT2R	O	Rch Analog Output 2 Pin
35	AOUT2L	O	Lch Analog Output 2 Pin
36	AOUT1R	O	Rch Analog Output 1 Pin
37	AOUT1L	O	Lch Analog Output 1 Pin
38	AOUT3N	O	Analog Negative Output 3 Pin
39	AOUT3P	O	Analog Positive Output 3 Pin
40	VSS3	-	Ground Pin, 0V
41	A3V32	-	Analog Power Supply Pin, 3.0V~3.6V
42	VREFH2	I	Positive Voltage Reference Input Pin, AVDD2
43	TST3	-	This pin must be connected to VSS4 pin.
44	SDTI3	I	Audio Serial Data Input 3 Pin
45	VSS4	-	Ground Pin, 0V
46	D1V8	-	Digital Power Supply Pin, 1.7V~1.9V
47	PDN	I	Power-Down & Reset Pin When "L", the AK4616 is powered-down and the control registers are reset to default state.
48	SCL	I	Control Data Clock Pin

Note 1. All digital input pins must not be allowed to float.

■Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AIN3RP, AIN3RN, AIN3LP, AIN3LN, AIN2RP, AIN2RN, AIN2LP, AIN2LN, AIN1RP, AIN1RN, AIN1LP, AIN1LN, AIN4R, AIN4L, MINN, MIN/MINP,	Open
	MPRF, MICBIAS, AOUT2R, AOUT2L, AOUT1R, AOUT1L, AOUT3N, AOUT3P	Open
Digital	SDA, SDTI1, SDTI2, SDTI3, SCL	Connect to VSS1
	SDTO1, SDTO2,	Open

ABSOLUTE MAXIMUM RATINGS

(VSS1 ~ 4 = 0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog Digital1 Digital2	A3V31, A3V32 D3V3 D1V8	-0.3 -0.3 -0.3	6.0 6.0 2.5	V V V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	A3V31+0.3	V
Digital Input Voltage (MCLK, LRCK, BICK, SDTI1-3, PDN, SCL, and SDA pins)		VIND	-0.3	D3V3+0.3	V
Ambient Temperature (power applied)(Note 3)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS1 ~ 4 must be connected to the same analog ground plane.
Note 3. In case that PCB wiring density is 100%.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1 ~ 4 = 0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 4)	Analog	A3V31, A3V32	3.0	3.3	3.6	V
	Digital1	D3V3	3.0	3.3	3.6	V
	Digital2	D1V8	1.7	1.8	1.9	V
	Difference	A3V31, A3V32 – D3V3	-0.1	0	+0.1	V

Note 4. The power up sequence between A3V31, A3V32, D3V3 and D1V8 is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4616 under the condition that a surrounding device is powered on and the I2C bus is in use. A3V31 and A3V32 must be connected with the same power supply.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25ºC; A3V31, A3V32=D3V3=3.3V, D1V8=1.8V, VSS1 ~ 4 =0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz; Unless otherwise specified.)

			min	typ	max	Unit
MIC AMP						
Input Resistance			40			kΩ
Gain	MGAIN[2:0]bits=0h			0		dB
	MGAIN[2:0]bits=1h			15		dB
	MGAIN[2:0]bits=2h			18		dB
	MGAIN[2:0]bits=3h			21		dB
	MGAIN[2:0]bits=4h			24		dB
	MGAIN[2:0]bits=5h			27		dB
	MGAIN[2:0]bits=6h			30		dB
	MGAIN[2:0]bits=7h			33		dB
MIC BIAS						
Bias Output Voltage	Load current = 0mA			2.46		V
	Load current = 1mA			2.32		V
Load Resistance			2			kΩ
Load Capacitance					30	pF
Stereo ADC Analog Input Characteristics						
Resolution					24	Bits
S/(N+D)	(-1dBFS, Differential inputs)		80	88		dB
DR	(-60dBFS with A-weighted, Differential inputs)		89	99		dB
S/N	(A-weighted, Differential inputs)		89	99		dB
Interchannel Isolation				110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Input Voltage	Single-ended (AIN=0.81x AVDD1)		2.40	2.67	2.94	Vpp
	Differential (AIN=±0.81x AVDD1)		±2.40	±2.67	2.94	Vpp
Input Resistance			40			kΩ
Power Supply Rejection	(Note 5)			70		dB
Monaural ADC Analog Input Characteristics (Single-ended inputs)						
Resolution					24	Bits
S/(N+D)	(-1dBFS)	MGAIN[2:0]bits=0h(0dB)		87		dB
		MGAIN[2:0]bits=3h(+21dB)		80		dB
DR (-60dBFS with A-weighted)		MGAIN[2:0]bits=0h(0dB)		97		dB
		MGAIN[2:0]bits=3h(+21dB)		85		dB
S/N	(A-weighted)	MGAIN[2:0]bits=0h(0dB)		97		dB
		MGAIN[2:0]bits=3h(+21dB)		85		dB
Gain Drift				20	-	ppm/°C
Input Voltage	Single-ended (AIN=0.81x AVDD1)			2.67		Vpp
	Differential (AIN=±0.81x AVDD1)			±2.67		Vpp
Power Supply Rejection	(Note 5)			70		dB
DAC1, 2 Analog Output Characteristics (Single-ended outputs)						
Resolution					24	Bits
S/(N+D)	(0dBFS)		85	95		dB
DR	(-60dBFS with A-weighted)		100	105		dB
S/N	(A-weighted) (Note 6)		100	105		dB
Interchannel Isolation				100		dB
Interchannel Gain Mismatch (Note 7)				0	0.7	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.61x VREFH2		1.80	2.00	2.20	Vpp
Load Resistance	(AC Load)		5			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 5)				70		dB

DAC3 Analog Output Characteristics (Differential outputs)					
Resolution				24	Bits
S/(N+D) (0dBFS)			100		dB
DR (-60dBFS with A-weighted)			107		dB
S/N (A-weighted)		100	107		dB
Gain Drift			20	-	ppm/°C
Output Voltage	AOUT=0.62x VREFH2		±2.06		Vpp
Load Resistance (AC Load)		5			kΩ
Load Capacitance				30	pF
Power Supply Rejection (Note 5)			70		dB

Note 5. PSR is applied to A3V31, A3V32 and D3V3 with 1kHz, 50mVpp. VREFH2 pin is held a constant voltage +3.3V.
Note 6. CCIR468-Un-weighted data is 102.2dB(typ) at 22Hz~22kHz. σ = 0.42dB.
Note 7. Channel gain mismatch between all output channels (AOUT1L/R, AOUT2L/R).

Parameter	min	typ	max	Unit
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H")				
A3V31+A3V32		22	33	mA
D3V3		1	2	mA
D1V8		3	6	mA
Power-down mode				
(PDN pin = "L") (Note 8)				
A3V31+A3V32+D3V3+D1V8		10	200	μA

Note 8. In the power-down mode, all digital input pins including clock pins are held VSS1.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= -40 ~ +85°C; A3V31, A3V32= D3V3=3.0~ 3.6V, D1V8 =1.7~ 1.9V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	±0.16dB	PB	0	-	18.8	kHz
	−0.66dB		-	21.1	-	kHz
	−1.1dB		-	21.7	-	kHz
	−6.9dB		-	24.1	-	kHz
Stopband (Note 9)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 10)		GD	-	18.4	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	−3.0dB	FR	-	3.7	-	Hz
	−0.5dB		-	10.9	-	Hz
	−0.1dB		-	24.0	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 9)	±0.06dB	PB	0	-	21.8	kHz
	−6.0dB		-	24.0	-	kHz
Stopband (Note 9)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 10)		GD	-	23	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 11)	20kHz	FR	-	-0.1	-	dB

Note 9. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (−1.0dB) = 0.454 x fs, DAC: Passband (±0.06dB) = 0.45412 x fs (@ fs=48kHz).

Note 10. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.

Note 11. The reference frequency is 1kHz.

DC CHARACTERISTICS

(Ta=-40°C~+85°C; A3V31, A3V32= D3V3=3.0~ 3.6V;D1V8 =1.7~1.9V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-3, PDN, SCL, SDA pins)	VIH	70% D3V3	-	-	V
Low-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-3, PDN, SCL, SDA pins)	VIL	-	-	30% D3V3	V
High-Level Output Voltage (SDTO1-2 pins: Iout=-100μA)	VOH	D3V3-0.5	-	-	V
Low-Level Output Voltage (SDTO1-2 pins: Iout= 100μA)	VOL		-	0.5	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-40~+85°C; A3V31, A3V32= D3V3=3.0~ 3.6V; D1V8=1.7~ 1.9V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
External Clock					
256fs:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fs:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fs:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
LRCK Timing (Slave mode)					
Stereo mode (TDM bit = "0")					
LRCK frequency	fs	8		48	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM bit = "1")					
LRCK frequency	fs	8		48	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
Audio Interface Timing (Slave mode)					
Stereo mode (TDM bit = "0")					
BICK Period	tBCK	324			ns
BICK Pulse Width Low	tBCKL	130			ns
Pulse Width High	tBCKH	130			ns
LRCK Edge to BICK "↑" (Note 12)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 12)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^2S mode)	tLRS			80	ns
BICK "↓" to SDTO	tBSD			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
TDM256 mode (TDM bit = "1")					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 12)	tLRB	23			ns
BICK "↑" to LRCK Edge (Note 12)	tBLR	23			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Note 12. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 13)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 14)	tPD	150			ns
PDN "↑" to SDTO valid (Note 15)	tPDV		1059		1/fs

Note 13. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 14. The AK4616 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150ns for a certain reset. The AK4616 is not reset by the "L" pulse less than 30ns.

Note 15. These cycles are the number of LRCK risings after internal power-down is released. Internal power-down is released after Dummy Command Input.

Note 16. I^2C is a trademark of NXP B.V.

■ Timing Diagram

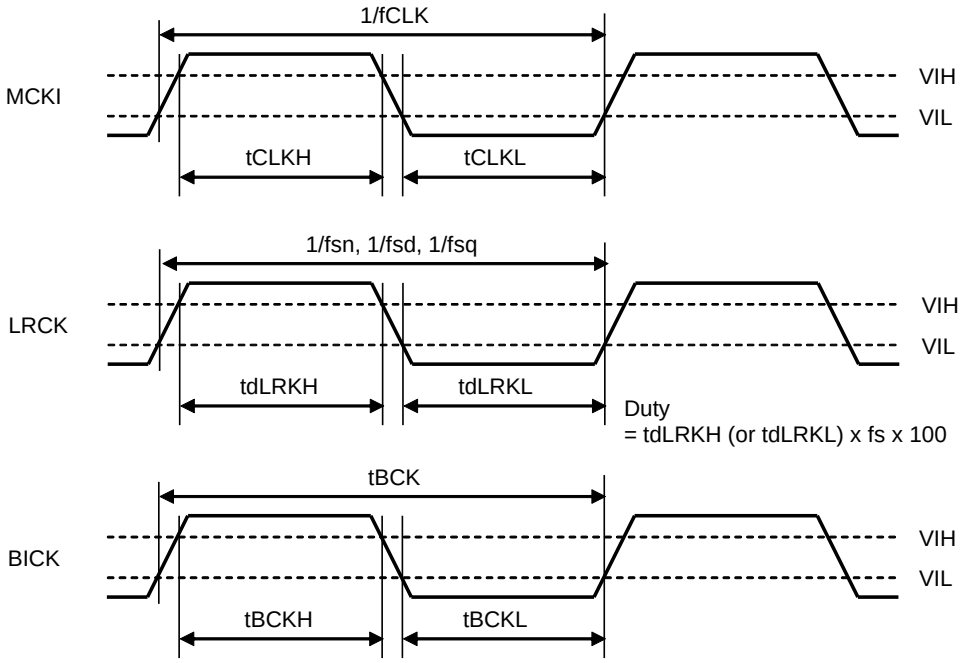


Figure 2. Clock Timing (TDM bit = "0" & Slave mode)

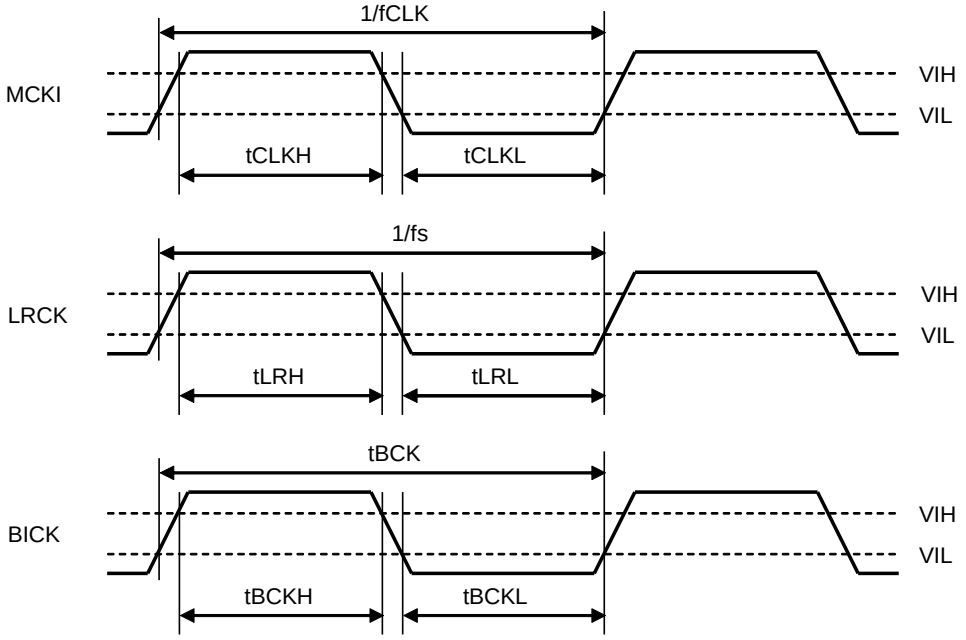


Figure 3. Clock Timing (Except TDM bit = "0" & Slave mode)

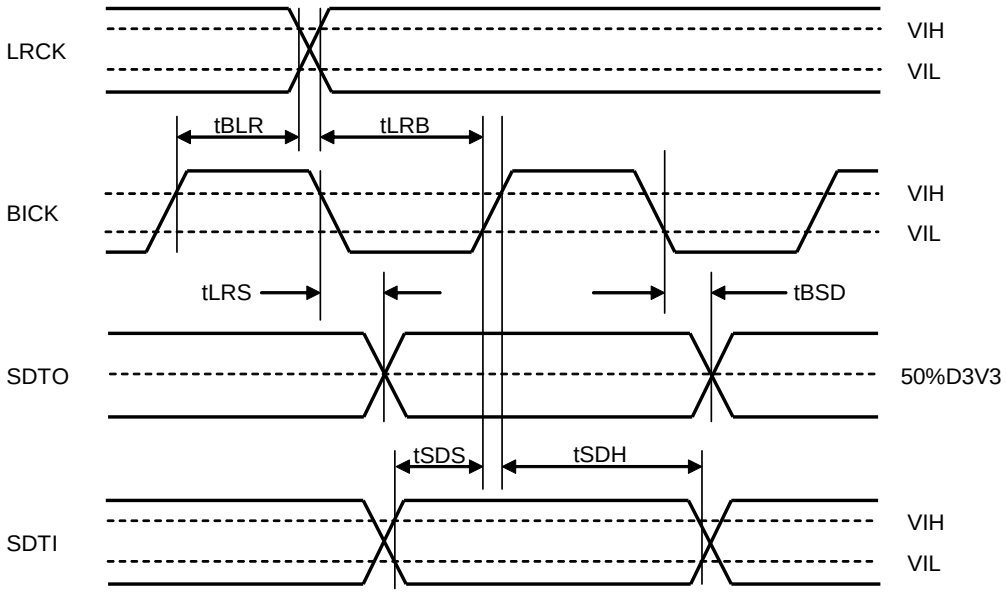


Figure 4. Audio Interface Timing (TDM bit = "0" & Slave mode)

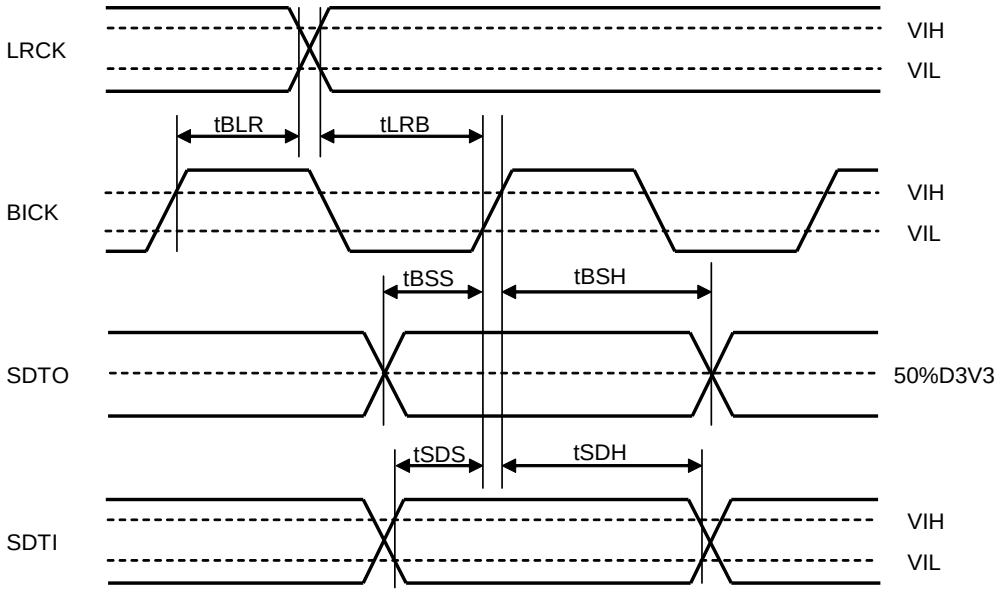


Figure 5. Audio Interface Timing (Except TDM bit = "0" & Slave mode)

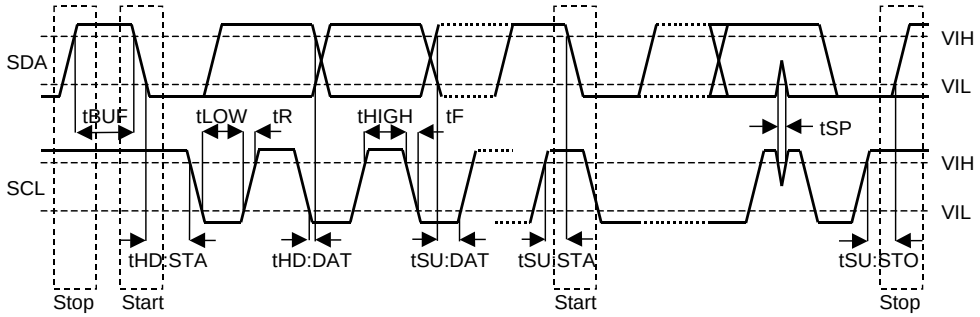


Figure 6. I^{2}C Bus mode Timing

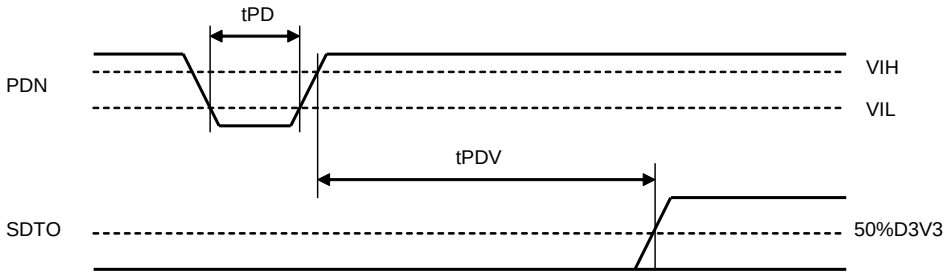


Figure 7. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4616 in slave mode are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK but the phase is not critical. After exiting reset at power-up in slave mode, the AK4616 is in power-down mode until MCLK, LRCK and BICK are input. If the clock is changed, reset the AK4616 by setting the PDN pin = "L".

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
8.0kHz	2.0480	3.0720	4.0960	0.5120
16.0kHz	4.0960	6.1440	8.1920	1.0240
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 1. System Clock Example

■ Input Selector

The AK4616 includes a 4ch stereo input selector for ADC, a monaural ADC mixing switch and an input selector for DAC1 and DAC2. The input selector for ADC is 4 to 1 selector and set by AIN1-0 bits (Table 2). The mixing switch for ADC and monaural ADC is set by MOMIX bit (Table 3). The output is clipped at full scale if the mixing result of ADC and monaural ADC outputs was more than 0dB. Adjust ADC volume or monaural ADC volume to prevent this clipping. The input selector for DAC1 and DAC2 is set by DACIN bit (Table 4).

AIN1 bit	AIN0 bit	Input Selector	
0	0	AIN1L /AIN1R	(default)
0	1	AIN2L /AIN2R	
1	0	AIN3L /AIN3R	
1	1	AIN4L /AIN4R	

Table 2. Input Selector for ADC

MOMIX bit	Monaural ADC mixing	
0	Off	(default)
1	On	

Table 3, Mixing Switch for ADC and Monaural ADC

DACIN bit	Input Selector	
0	ADC	(default)
1	DOUT L/R	

Table 4. Input Selector for DAC1 and DAC2

* When DACIN bit = "0", the digital ADC output is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-2 is ignored. The audio format of SDTO at loopback mode becomes mode 3 at mode 0, 1, 2, and 3, and mode 4 at mode 4, respectively. DACIN bit should be set "1" in TDM mode.

[Selector Switching Sequence]

The input selector for ADC should be changed after enabling a mute function, set by SADATL/R7-0 bits, to avoid the switching noise of the input selector (Figure 8).

1. Enable mute before changing channel.
2. Change channel.
3. Disable mute.

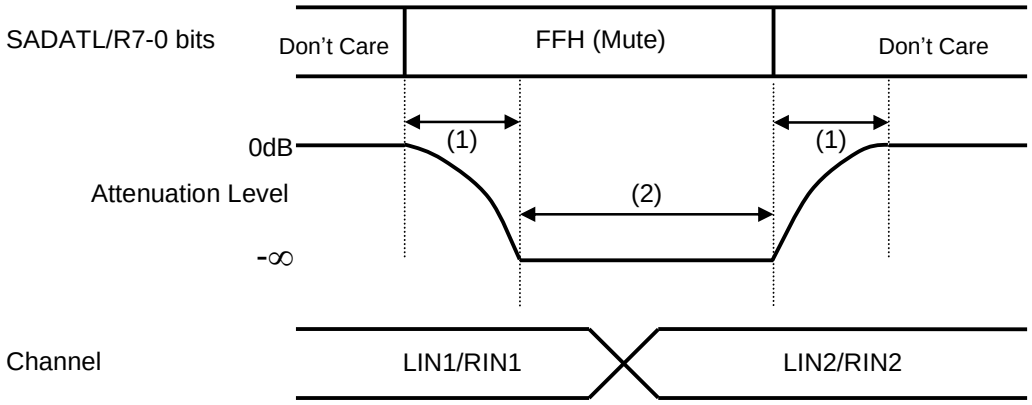


Figure 8. Input channel switching sequence example

Note:
(1) The output signal is attenuated to −∞ in the cycle set by ADATS1-0 bits (Table 11).
(2) When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels.

The mixing switch for ADC and monaural ADC should be changed after muting output of monaural ADC, set by MADAT7-0 bits, to avoid the switching noise of the mixing switch (Figure 9).

1. Enable mute before changing channel.
2. Mixing monaural ADC
3. Disable mute.

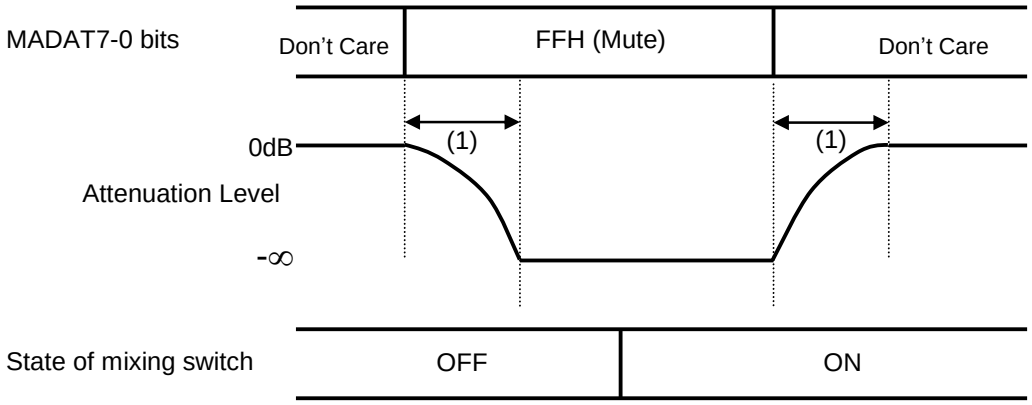


Figure 9. Input channel switching sequence example

Note:
(1) The output signal is attenuated to −∞ in the cycle set by ADATS1-0 bits (Table 11).

The input selector for DAC1 and DAC2 should be changed after enabling soft mute function, set by DAATS1-0 bits, to avoid the switching noise of the input selector (Figure 10).

1. Enable soft mute before changing channel.
2. Change channel.
3. Disable soft mute.

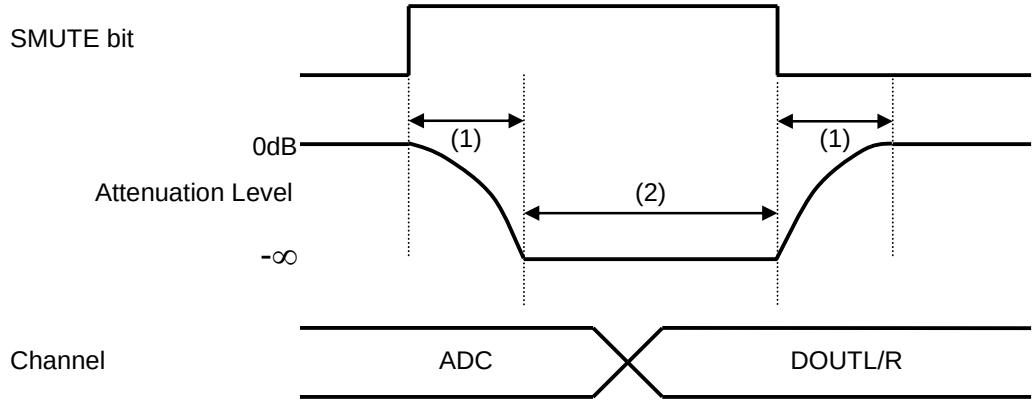


Figure 10. Input channel switching sequence example

Note:

(1) The output signal is attenuated to −∞ in the cycle set by DAATS1-0 bits (Table 10).

(2) When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels.

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 3.7Hz at fs=48kHz and scales with the sampling rate (fs).

■ Audio Serial Interface Format

(1) Stereo Mode

When TDM bits = "0", ten modes can be selected by the DIF2-0 bits as shown in Table 5. In all modes the serial data is MSB-first, 2's compliment format. The data SDTO1-2 is clocked out on the falling edge of BICK and the SDTI1-3 is latched on the rising edge of BICK.

Mode 2/3/4/7/8/9 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

Mode	TDM	DIF2	DIF1	DIF0	SDTO1-2	SDTI1-3	LRCK		BICK		
								I/O		I/O	
0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	I	≥ 32fs	I	
1	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	I	≥ 48fs	I	
2	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	I	≥ 48fs	I	
3	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	I	≥ 48fs	I	
4	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	I	≥ 48fs	I	(default)

Table 5. Audio Data Formats (Stereo mode)

(2) TDM Mode

The audio serial interface format is set in TDM mode by the TDM bit = "1". Five modes can be selected by the DIF2-0 bits. In all modes the serial data is MSB-first, 2's compliment format. The SDTO1 is clocked out on the rising edge of BICK and the SDTI1/2 are latched on the rising edge of BICK.

TDM256 mode can be set by TDM bit = "1"as show in Table 6. In the TDM256 mode, the serial data of all ADC (three channels) is output to the SDTO1 pin. The SDTO2 pin = "L". And the serial data of DAC (six channels; L1, R1, L2, R2, L3, R3) is input to the SDTI1 pin. The input data to SDTI2-3 pins are ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be 1/256fs at least.

Mode	TDM	DIF2	DIF1	DIF0	SDTO1-2	SDTI1-3	LRCK		BICK	
								I/O		I/O
5	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	256fs	I
6	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	256fs	I
7	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	256fs	I
8	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	256fs	I
9	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	256fs	I

Table 6. Audio data formats (TDM256 mode)

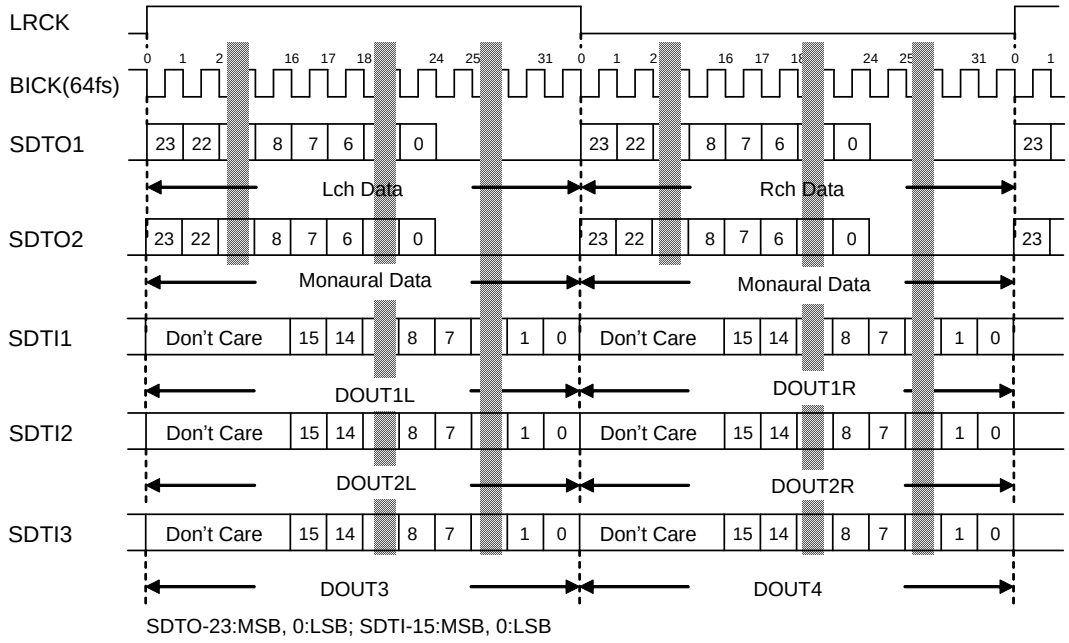


Figure 11. Mode 0 Timing (Stereo Mode)

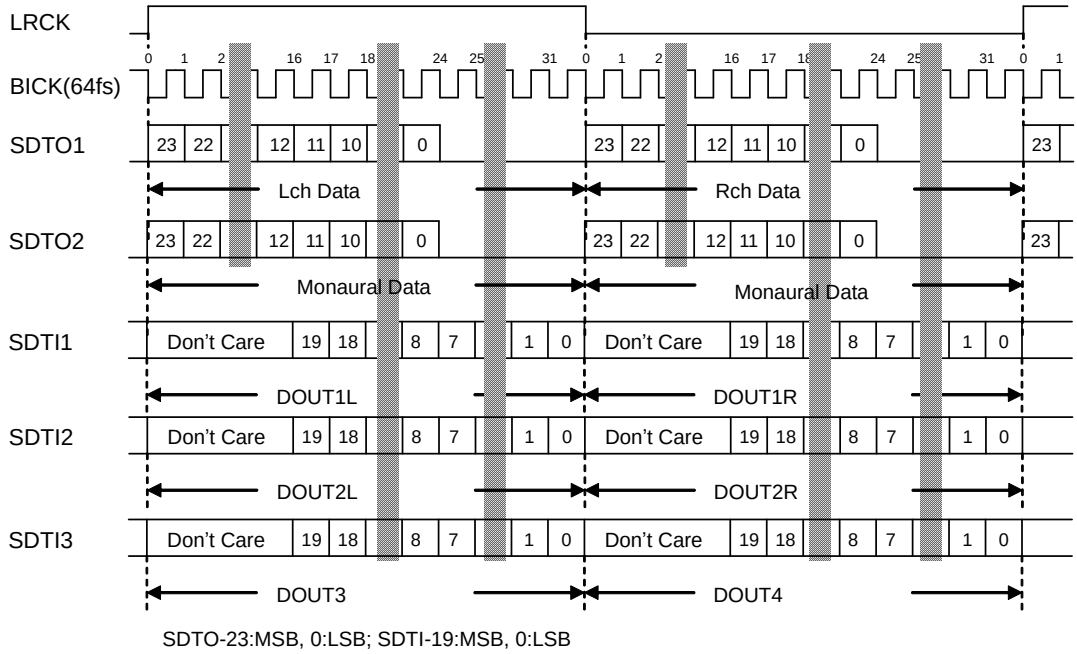


Figure 12. Mode 1 Timing (Stereo Mode)

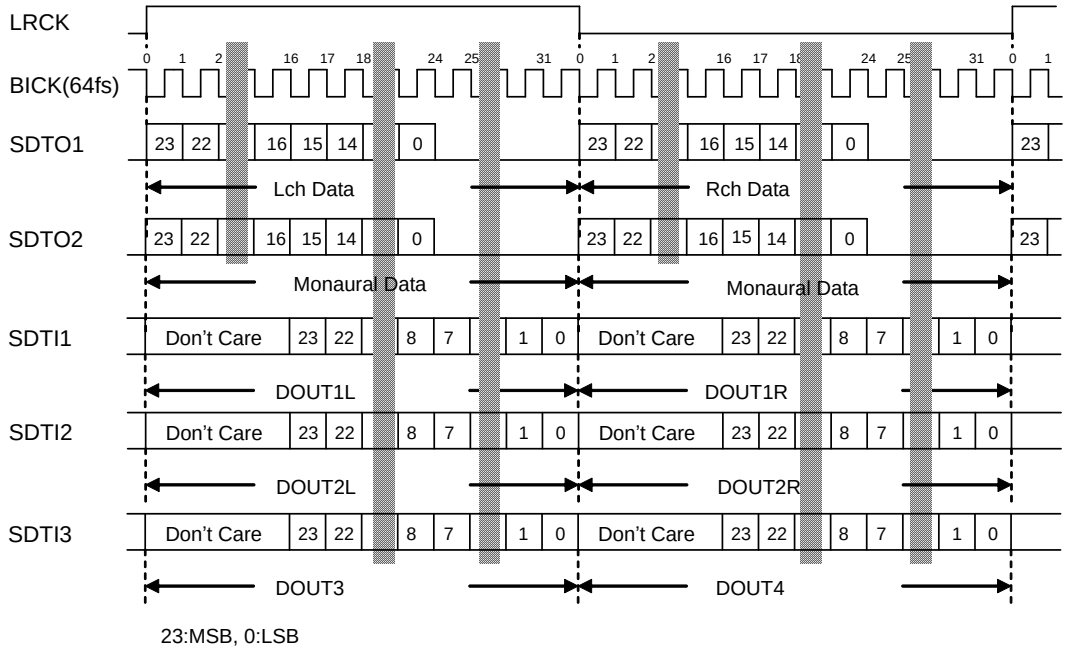


Figure 13. Mode 2 Timing (Stereo Mode)

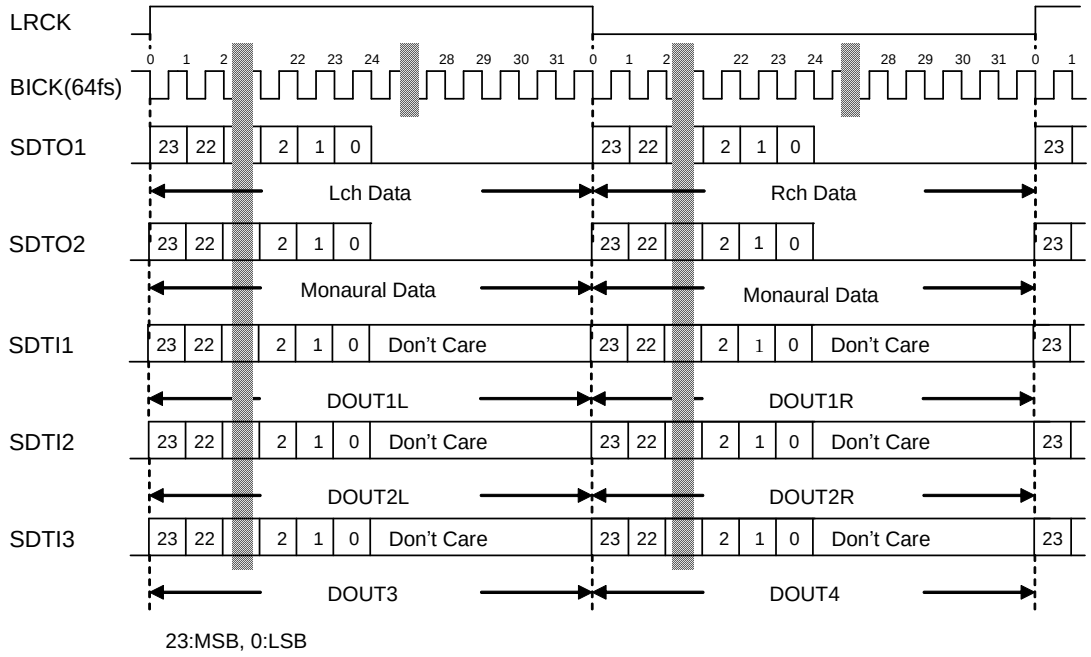


Figure 14. Mode 3 Timing (Stereo Mode)

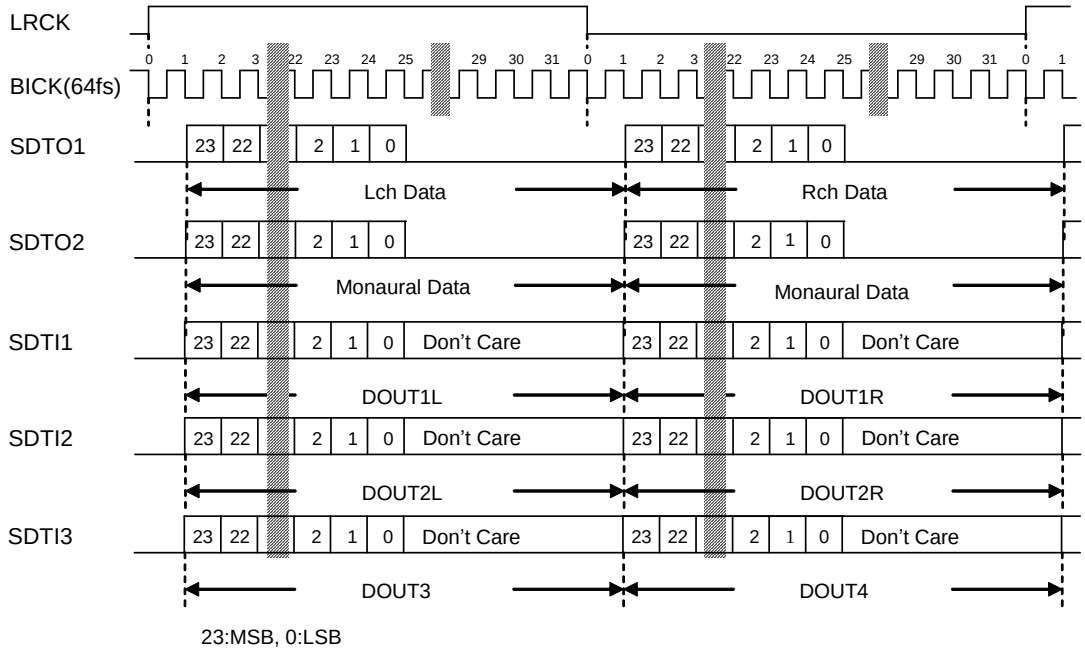


Figure 15. Mode 4 Timing (Stereo Mode)

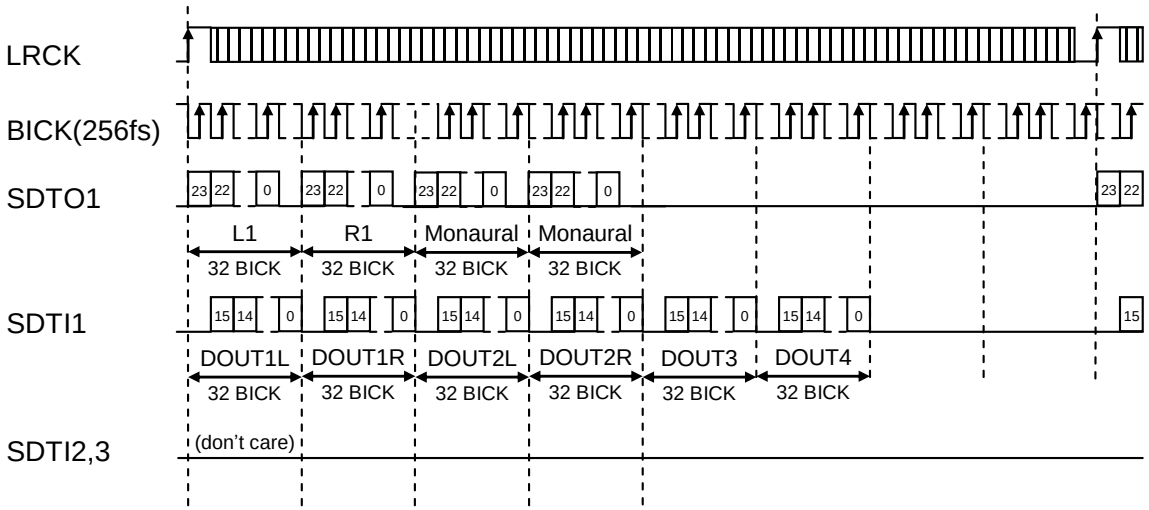


Figure 16. Mode 5 Timing (TDM256 Mode)

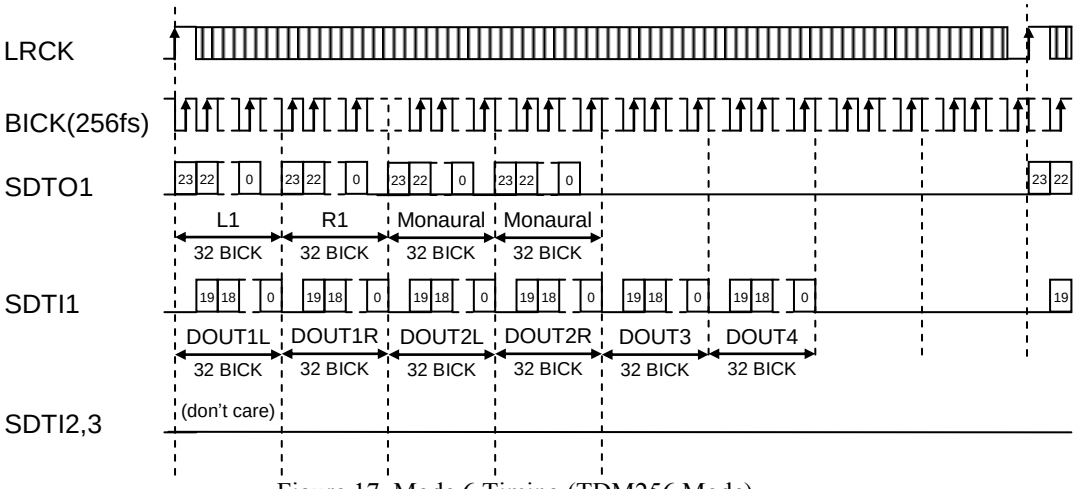


Figure 17. Mode 6 Timing (TDM256 Mode)

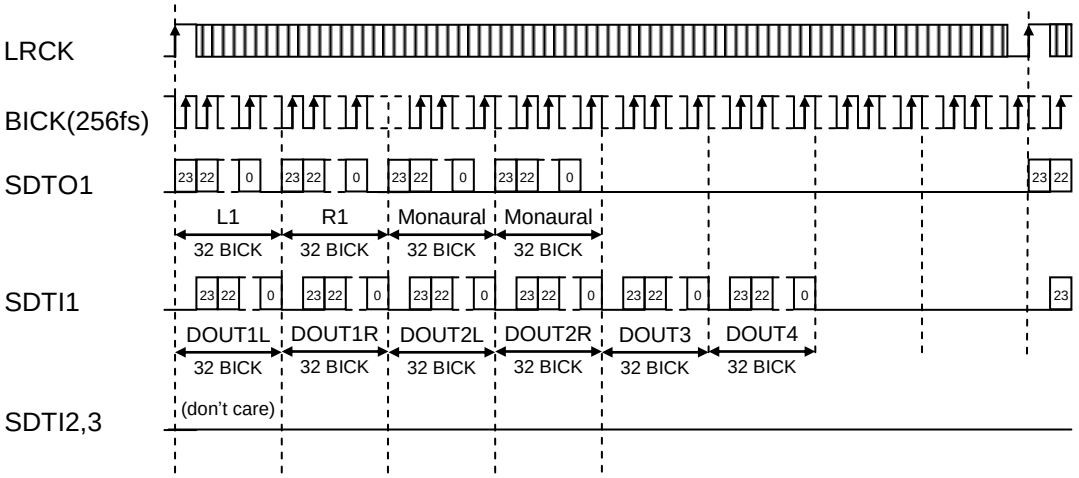


Figure 18. Mode 7 Timing (TDM256 Mode)

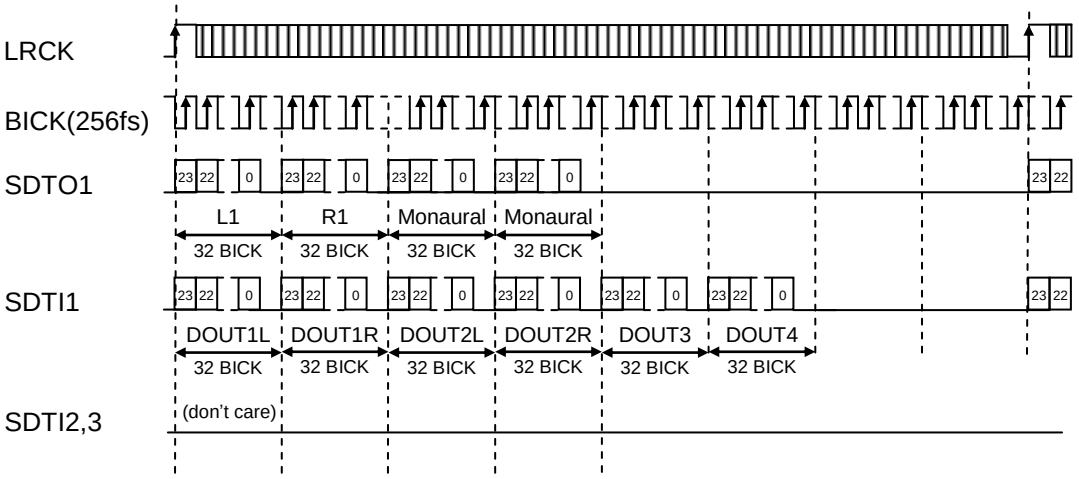


Figure 19. Mode 8 Timing (TDM256 Mode)

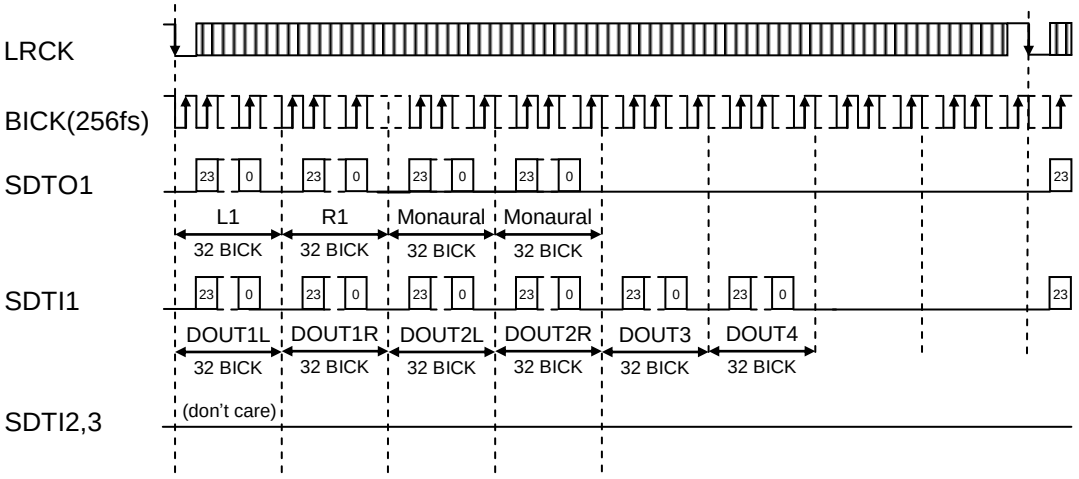


Figure 20. Mode 9 Timing (TDM256 Mode)

■ Digital Attenuator

AK4616 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each DAC1, DAC2, MONODAC3, ADC, MONOADC can be set by DAATL1/R1 7-0 bit, DAATL2/R2 7-0 bit, DAAT3 7-0 bit, SADATL/R 7-0 bit, MADAT 7-0 bit respectively. (Table 7, Table 8).

DAATL1/R17-0bits DAATL2/R27-0 bits DAAT37-0 bits	Attenuation Level	
00H	+0dB	(default)
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63.0dB	
7FH	-63.5dB	
:	:	
FEH	-127.0dB	
FFH	MUTE (-∞)	

Table 7. Attenuation level of DAC Digital Attenuator

SADATL/R 7-0 bits MADAT 7-0 bits	Attenuation Level	
00H	+0dB	(default)
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63.0dB	
7FH	-63.5dB	
:	:	
FEH	-127.0dB	
FFH	MUTE (-∞)	

Table 8. Attenuation level of ADC Digital Attenuator

The AK4616 has a monaural mixing function which adds DOUT4 volume output to DAC1L/1R volume output (Figure 21). The default setting of DAAT47-0 bits is MUTE (FFH). The output is clipped at full scale if the mixing result of DOUT1 and DOUT4 outputs was more than 0dB. Adjust DAC1L/R volume or DOUT4 volume to prevent this clipping.

DAAT4 7-0 bits	Attenuation Level	
00H	+0dB	
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63.0dB	
7FH	-63.5dB	
:	:	
FEH	-127.0dB	
FFH	MUTE (-∞)	(default)

Table 9. Attenuation level of DOUT4 Digital Attenuator

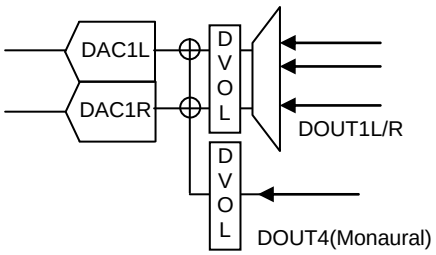


Figure 21. Monaural Mixing Block

Transition time between set values of DAAT17-0, DAAT27-0, DAAT37-0, DAAT47-0 bits and SADATL/R 7-0, MADAT7-0 bits can be selected by the DAATS1-0 bits and ADATS1-0 bits (Table 10 and Table 11). Transition between set values is the soft transition in Mode1/2/3 eliminating switching noise in the transition.

Mode	DAATS1	DAATS0	ATT speed	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 10. Transition Time between Set Values of DAAT17-0, DAAT27-0, DAAT37-0, DAAT47-0 bits

Mode	ADATS1	ADATS0	ATT speed	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 11. Transition Time between Set Values of SADATL/R 7-0, MADAT 7-0 bits

The transition between set values is a soft transition of 4080 levels in mode 0. It takes 4080/fs (85.0ms@fs=48kHz) from 00H to FFH. If the PDN pin goes to "L", DAAT17-0, DAAT27-0, DAAT37-0 bits and SADATL/R 7-0, MADAT7-0 bits are initialized to 00H, and DAAT47-0 bits are initialized to FFH. These bits are also set to 00H and FFH respectively when RSTN bit = "0", and fade to their current value when RSTN bit returns to "1".

■ MIC Gain Amplifier

The AK4616 has a gain amplifier which supports both single-ended and differential inputs. When MDIF bit is set to "1", differential inputs are supported by the INP/N pins and the maximum input voltage is dependent on A3V31. If the AVDD= 3.3V, the maximum input voltage for single-ended input is 2.2Vpp and ±2.2Vpp for differential inputs. The typical input impedance is 30kΩ (typ). MGAIN2-0 bits control the input gain of the microphone amplifier (Table 12). A pop nose occurs if the input gain is changed during an operation.

Mode	MGAIN2	MGAIN1	MGAIN0	Input Gain	
0	0	0	0	0dB	(default)
1	0	0	1	15dB	
2	0	1	0	18dB	
3	0	1	1	21dB	
4	1	0	0	24dB	
5	1	0	1	27dB	
6	1	1	0	30dB	
7	1	1	1	33dB	

Table 12. MIC Input Gain (typ.)

■ MIC Bias

The AK4616 integrates power supply for microphone. Connect a 1μF capacitor between the MPRF pin and the VSS2 pin. When PMMB bit = "1", the MICBIAS pin supplies power for the microphone. This output voltage is typically 2.32V and the load resistance is minimum 2.0kΩ. (Figure 22)

PMMB bit	MICBIAS pin	
0	Hi-Z	(default)
1	Output	

Table 13. MICBIAS pin

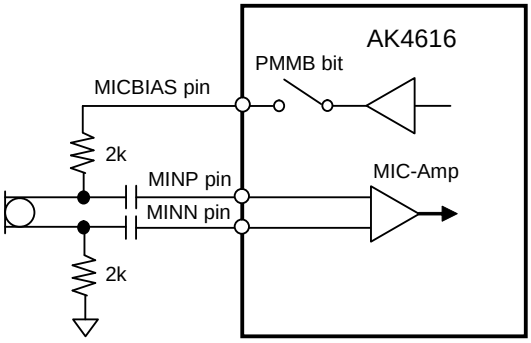


Figure 22. MIC Input Circuit (differential Input)

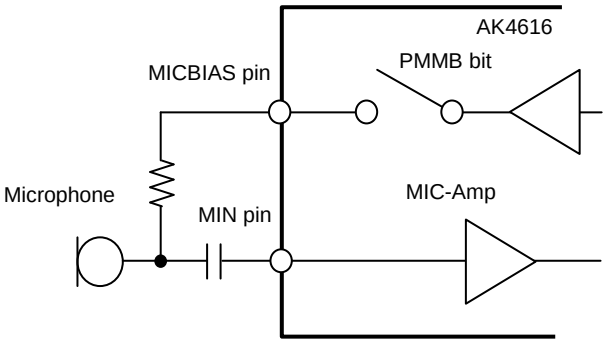
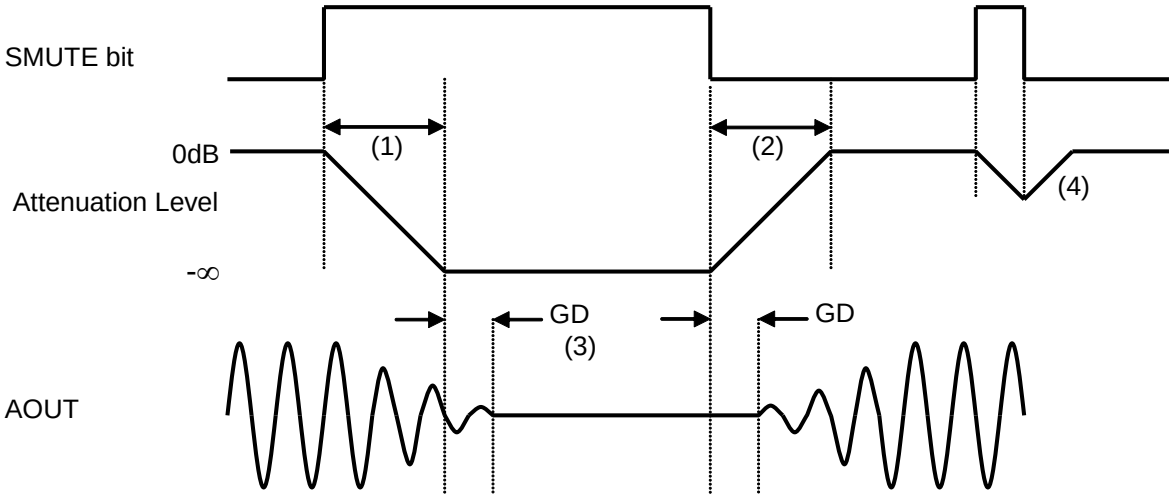


Figure 23. MIC Input Circuit (Single-ended Input)

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTE bit becomes "1", the output signal is attenuated to -∞ in the cycle set by DAATS1-0 bits (Table 10) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level in the cycle set by ATS bits. If the soft mute is cancelled before attenuating to -∞ after starting the operation, attenuation is discontinued and it is returned to ATT level by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The time for input data attenuation to -∞ (Table 10). For example, this time is 4080LRCK cycles (4080/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The time for input data recovery to ATT level (Table 10). For example, this time is 4080LRCK cycles (4080/fs) at ATT-DATA=FFH. ATT transition of soft-mute is from FFH to 00H.

(3) The analog output corresponding to the digital input has group delay, GD.

(4) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 24. Soft Mute

■ System Reset

Upon power-up, the AK4616 must be reset by bringing the PDN pin = "L". This reset is released when a dummy command is input after the PDN pin = "H". This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all "0" to the register address 00H.

The AK4616 is powered up and the internal timing starts clocking by LRCK "↑"after exiting the power down state of reference voltage (such as VCOM) by MCLK. The AK4616 is in power-down mode until MCLK, LRCK and BICK are input.

It is recommended to set the PDN pin = "L" before power up the AK4616.

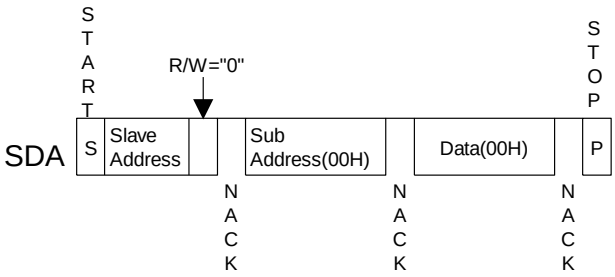
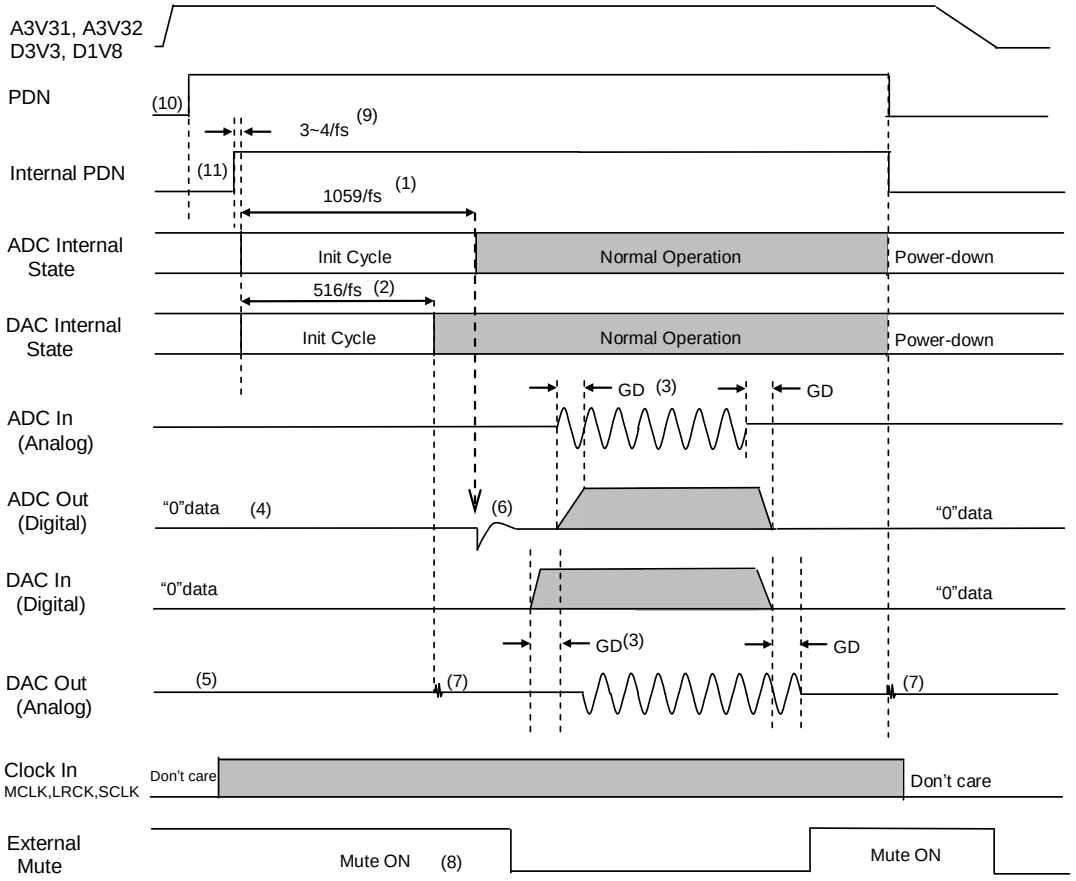


Figure 25. Dummy Command in I^2C-bus Mode

■ Power-Down

All ADCs and DACs of the AK4616 are placed in power-down mode by bringing the PDN pin "L" which resets both digital filters at the same time. The PDN pin "L" also resets the control registers to their default values. In power-down mode, the SDTO1-2 goes to "L", and the analog outputs go to Hi-Z. This reset should always be executed after power-up. For the ADC, an analog initialization cycle (1056/fs) starts 3~4/fs after exiting power-down mode. The output data, SDTO1-2, is available after 1059~1060 cycles of the LRCK clock. For the DAC, an analog initialization cycle (516/fs) starts 3~4/fs after exiting power-down mode. The analog outputs go to Hi-Z during the initialization. Figure 26 shows the power-down and power-up sequences. When the DACIN bit = "1", the DAC is available after 1059~1060 cycles of the LRCK clock.



Notes:

(1) The analog part of ADC is initialized after exiting internal power-down state.
When start-up the AK4616, ADC input voltage should be operating common voltage.
It is necessary to wait for the charge up time of HPF which consists of analog inputs.
When the external capacitor is 1uF and the input impedance is 60kΩ(typ), τ = 0.06 sec.

(2) The analog part of DAC is initialized after exiting internal power-down state.

(3) Digital output corresponds to analog input and analog output corresponds to digital input have group delay (GD).

(4) ADC output is "0" data at power-down state.

(5) The analog outputs go to Hi-Z in power-down mode.

(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system applications.

(7) Click noise occurs at the falling edge of PDN and at 519~520/fs after exiting internal power-down state.

(8) Mute the analog output externally if the click noise (7) influences system applications.

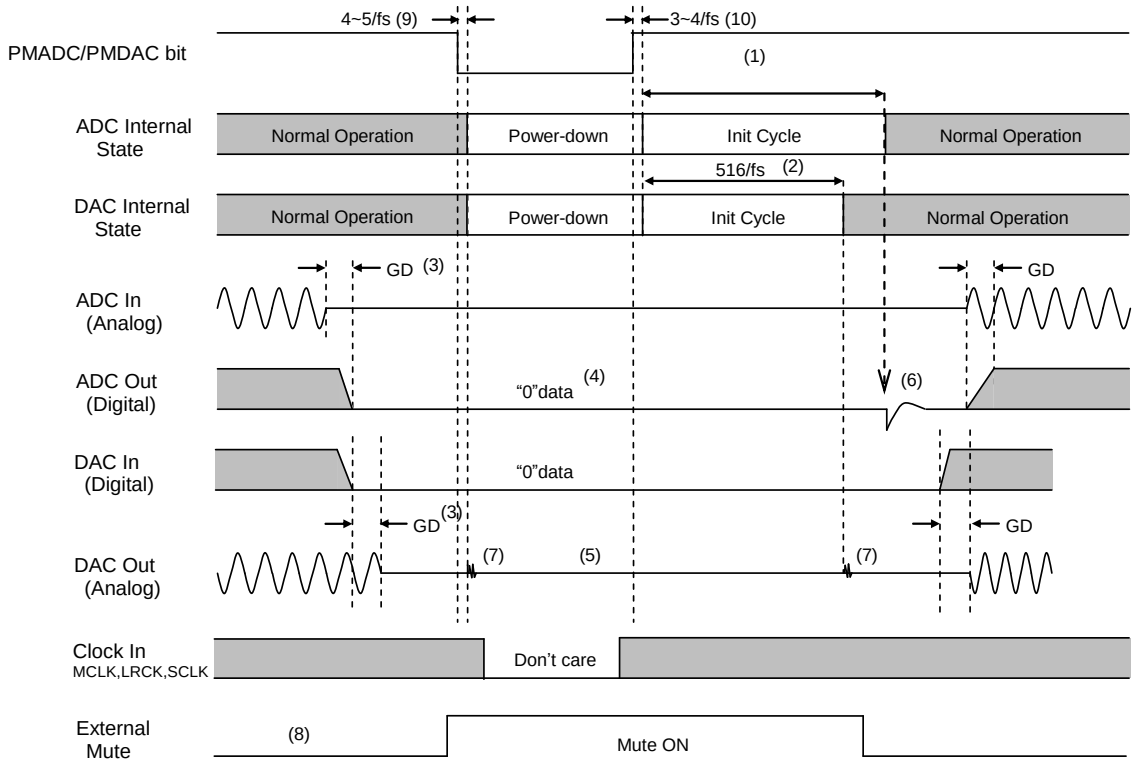
(9) There is a delay, 3~4/fs from internal power up to the start of initial cycle.

(10) The PDN pin must be "L" when power up the AK4616 and set to "H" after all poweres are supplied.

(11) After Dummy Command input, the internal power-down state is released.

Figure 26. Pin power-down/Pin power-up sequence example

All ADCs and all DACs can be powered-down individually by PMADC and PMDAC bits. DAC1-3 can be powered-down individually by PMDA1-3 bits. In this case, the internal register values are not initialized. When PMADC bit = "0", SDTO1-2 goes to "L". When PMDAC bit = "0", the analog outputs go to Hi-Z. As some click noise occurs, the analog output should be muted externally if the click noise influences system applications. Figure 27 shows the power-down and power-up sequences.



Notes:

(1) The analog section of ADC is initialized after exiting power-down state.
The initializing cycle is 1056fs. When start-up the AK4616, ADC input voltage should be operating common voltage.

(2) The analog section of DAC is initialized after exiting power-down state.

(3) Digital output corresponding to the analog inputs and analog outputs corresponding to the digital inputs have group delay (GD).

(4) ADC output is "0" data in power-down state.

(5) DAC output is Hi-Z in power-down state.

(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system application.

(7) Click noise occurs at 4~5/fs after PMDAC bit becomes "0", and it occurs at 519~520/fs after PMDAC bit becomes "1".

(8) Mute the analog output externally if the click noise (7) influences system application.

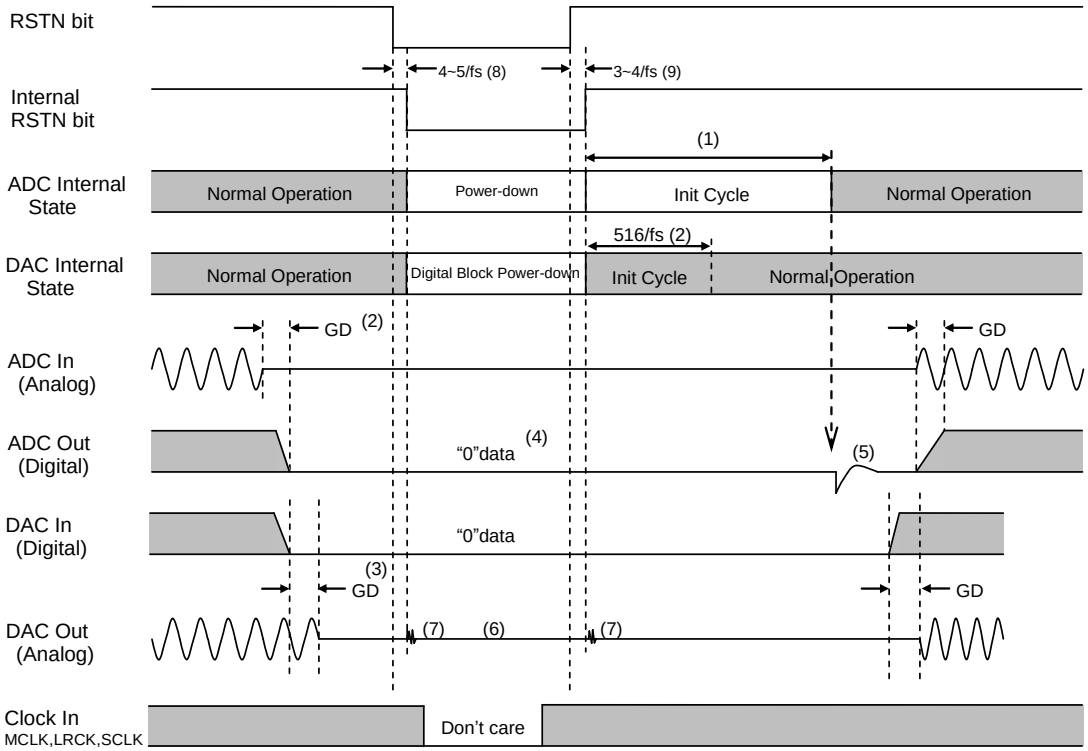
(9) There is a delay, 4~5/fs from PMADC bit becomes "0" to the applicable ADC power-down.
There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable DAC power-down.

(10) There is a delay, 3~4/fs from PMADC and PMDAC bits become "1" to the start of initial cycle.

Figure 27. Bit power-down/Bit power-up Sequence Example

■ Reset Function

When RSTN bit= "0", the analog and digital part of ADC and the digital part of DACs are powered-down, but the internal register are not initialized. The analog outputs go to Hi-Z, SDTO1-2 pin goes to "L". As some click noise occurs, the analog output should be muted externally if the click noise influences system application. Figure 28 shows the power-up sequence.



Notes:

(1) The analog section of the ADC is initialized after exiting reset state.
The initializing cycle is 1056fs. When start-up the AK4616, ADC input voltage should be operating common voltage.

(2) The analog parts of DACs are initialized after exiting power down mode.

(3) Digital output corresponding to the analog inputs, and analog outputs corresponding to the digital inputs have group delay (GD).

(4) ADC output is "0" data at power-down state.

(5) Click noise occurs when the initializing cycle is finished. Mute the digital output externally if the click noise influences system application.

(6) The analog outputs go to Hi-Z when RSTN bit becomes "0".

(7) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and it occurs at 3~4/fs after RSTN bit becomes "1".

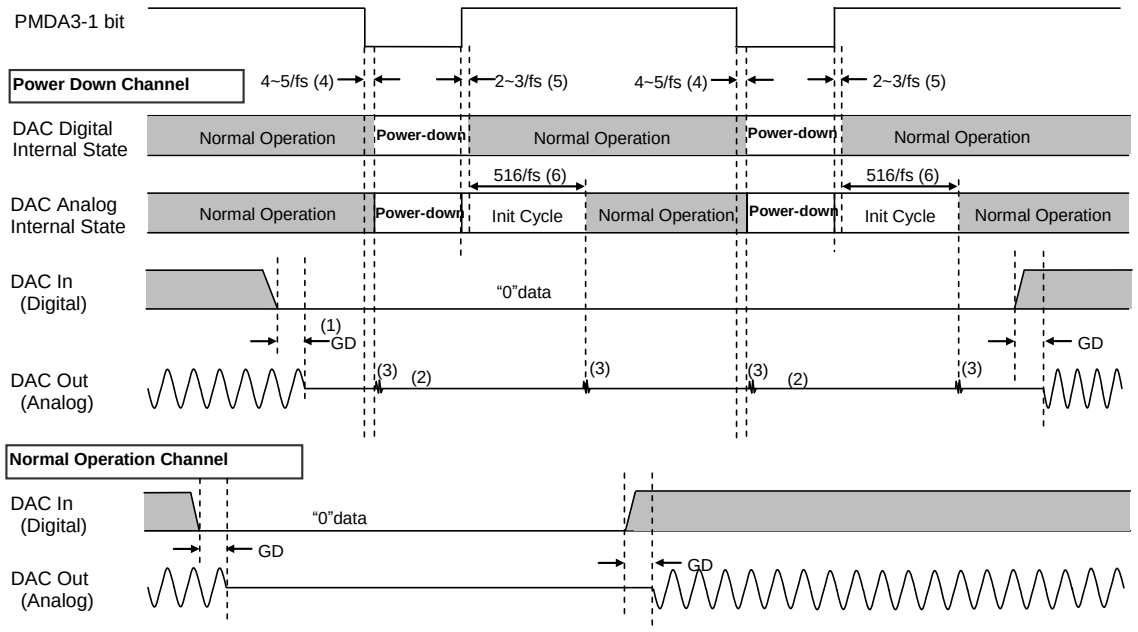
(8) There is a delay, 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

(9) There is a delay, 3~4/fs from RSTN bit "1" to the start of initial cycle.

Figure 28. Reset Sequence Example

■ DAC Partial Power-Down Function

All of the DACs can be powered-down individually by PMDA3-1 bits. The analog section and the digital section of the DAC are placed in power-down mode when the PMDA3-1 bits = "0". The analog output of the powered-down channels, which are set by PMDA3-1 bits, go to Hi-Z. Some click noise occurs in both set-up and release of power-down. Mute the analog output externally or set PMDA3-1 bits when PMDAC bit = "0" or RSTN bit = "0", if click noise aversely affects system performance. Figure 29 shows the sequence of the power-down and the power-up by PMDA3-1 bits.



Notes:

(1) Analog outputs corresponding to the digital inputs have group delay (GD).
(2) Analog output of the DAC is powered down by PMDA3-1 = "0" and goes to Hi-Z.
(3) Click noise occurs in 4~5/fs after PMDA3-1 bits are set to "0", and it occurs in 518~519/fs after PMDA3-1 bits are set to "1".
(4) The DACs will be powered-down 4~5fs after PMDA3-1 bits = "0"
(5) The initialization stars 2~3fs after PMDA3-1 bits are set to "1".
(6) The analog parts of DACs are initialized after exiting power down mode.

Figure 29. DAC Partial Power-down Example

■ Serial Control Interface

The AK4616's functions are controlled through registers or pins. The registers may be written by I^2C-bus modes. The PDN pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit, but the register data will not be initialized. *When the PDN pin = "L", control register writings are not valid.

The AK4616 supports the fast-mode I^2C-bus (max: 400kHz).

1. WRITE Operations

Figure 30 shows the data transfer sequence of the I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 36). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010000". If the slave address matches that of the AK4616, the AK4616 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 37). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4616. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 32). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 33). The AK4616 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 36).

The AK4616 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4616 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 0EH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 38) except for the START and STOP conditions.

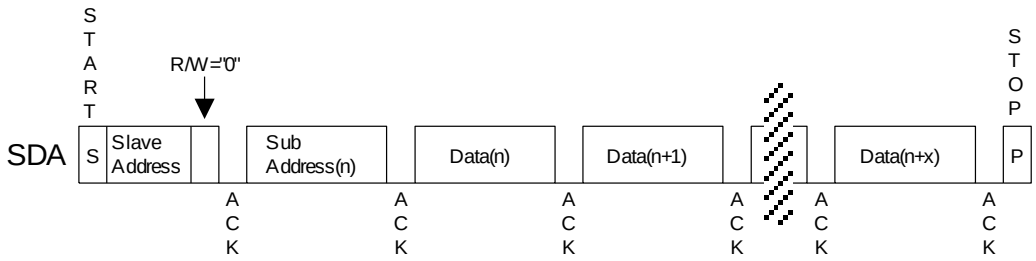


Figure 30. Data Transfer Sequence at the I^2C-Bus Mode

0	0	1	0	0	0	0	R/W

Figure 31. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 32. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 33. Byte Structure after the second byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4616. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 0EH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4616 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4616 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4616 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4616 ceases transmission.

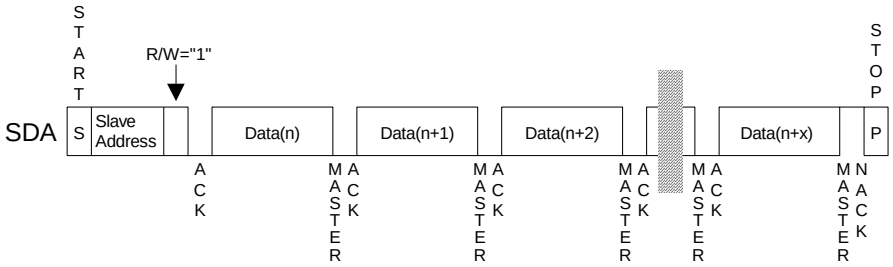


Figure 34. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK4616 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4616 ceases transmission.

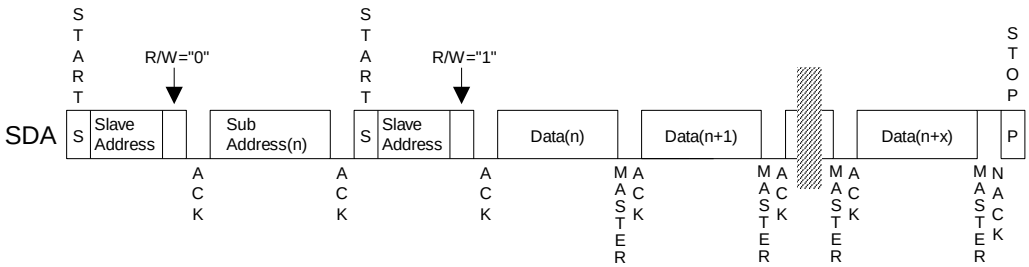


Figure 35. RANDOM ADDRESS READ

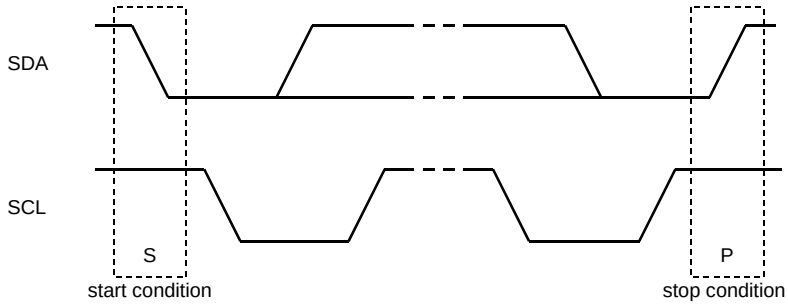


Figure 36. START and STOP Conditions

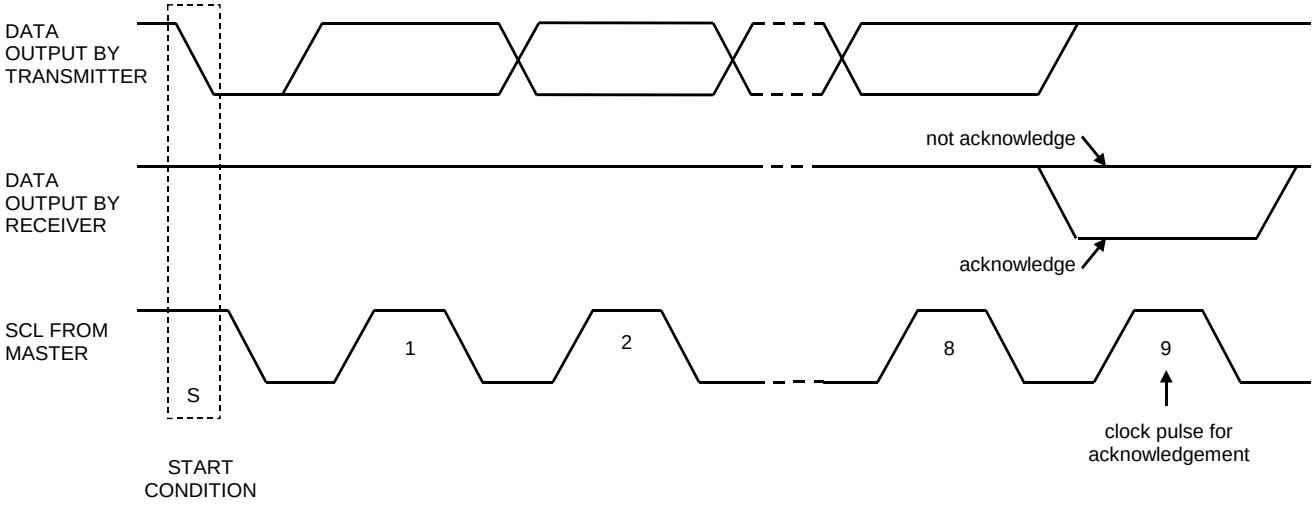


Figure 37. Acknowledge on the I^2C-Bus

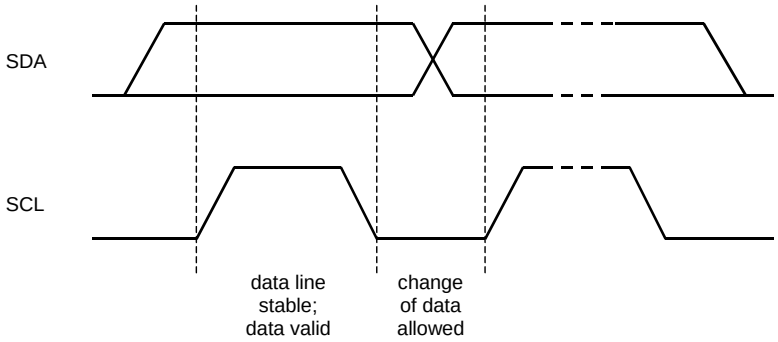


Figure 38. Bit Transfer on the I^2C-Bus

■ Register Map

Add	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMMB	PMADC	PMDAC	0	0	0	RSTN
01H	Power Management 2	0	0	0	0	0	PMDA3	PMDA2	PMDA1
02H	Audio Interface Format	0	0	0	TDM	0	DIF2	DIF1	DIF0
03H	Soft Mute	ADAST1	ADAST0	DAATS1	DAATS0	0	0	0	SMUTE
04H	Input Selector	0	0	0	DACIN	MOMIX	MDIF	AIN1	AIN0
05H	DAC1L Volume	DAATL17	DAATL16	DAATL15	DAATL14	DAATL13	DAATL12	DAATL11	DAATL10
06H	DAC1R Volume	DAATR17	DAATR16	DAATR15	DAATR14	DAATR13	DAATR12	DAATR11	DAATR10
07H	DAC2L Volume	DAATL27	DAATL26	DAATL25	DAATL24	DAATL23	DAATL22	DAATL21	DAATL20
08H	DAC2R Volume	DAATR27	DAATR26	DAATR25	DAATR24	DAATR23	DAATR22	DAATR21	DAATR20
09H	DOUT3 Volume	DAAT37	DAAT36	DAAT35	DAAT34	DAAT33	DAAT32	DAAT31	DAAT30
0AH	DOUT4 Volume	DAAT47	DAAT46	DAAT45	DAAT44	DAAT43	DAAT42	DAAT41	DAAT40
0BH	ADC Volume	SADATL7	SADATL6	SADATL5	SADATL4	SADATL3	SADATL2	SADATL1	SADATL0
0CH	ADC Volume	SADATR7	SADATR6	SADATR5	SADATR4	SADATR3	SADATR2	SADATR1	SADATR0
0DH	Monaural ADC Volume	MADAT7	MADAT6	MADAT5	MADAT4	MADAT3	MADAT2	MADAT1	MADAT0
0EH	Microphone Gain	0	0	0	0	0	MGAIN2	MGAIN1	MGAIN0

Note: For addresses from 0FH to 1FH, data must not be written. The bits defined as 0 must contain a “0” value.
When the PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMMB	PMADC	PMDAC	0	0	0	RSTN
R/W		RD	R/W	R/W	R/W	RD	RD	RD	R/W
Default		0	1	1	1	0	0	0	1

RSTN: Internal timing reset
0: Reset.
1: Normal operation (default)

PMDAC: Power management of DAC1-3
0: All DAC's Power-down. PMDA1-3 bits are invalid.
1: Normal operation. (default) PMDA1-3 bits are valid.

PMADC: Power management of mono-stereo
0: All ADC's Power-down.
1: Normal operation. (default)

PMMB: Power management of Mic Bias
0: Power-down
1: Normal operation (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	0	PMDA3	PMDA2	PMDA1
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	1

PMDA3-1: Power management of DAC1-3 (0: Power-down, 1: Normal operation)
PMDA1: Power management control of DAC1
PMDA2: Power management control of DAC2
PMDA3: Power management control of DAC3

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Audio Interface Format	0	0	0	TDM	0	DIF2	DIF1	DIF0
R/W		RD	RD	RD	R/W	RD	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

DIF2-0: Audio Data Interface Modes (Table 5, Table 6)
Initial: "100", mode 4

TDM: TDM Format Select (Table 5, Table 6)

Mode	TDM	Data Output Pins	Data Input Pins	TDM Format mode
0	0	SDTO1-2	SDTI1-3	Stereo mode
1	1	SDTO1	SDTI1	TDM256 mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Soft Mute	ADATS1	ADATS0	DAATS1	DAATS0	0	0	0	SMUTE
R/W		R/W	R/W	R/W	R/W	RD	RD	RD	R/W
Default		0	0	0	0	0	0	0	0

SMUTE: Soft Mute Enable
0: Normal operation (default)
1: All DAC outputs soft-muted

DAATS1-0: DAC Digital attenuator transition time setting (Table 10)
Initial: "00", mode 0

ADATS1-0: ADC Digital attenuator transition time setting (Table 11)
Initial: "00", mode 0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Input Selector	0	0	0	DACIN	MOMIX	MDIF	AIN1	AIN0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AIN1-0: ADC Input Select (Table 2)
Initial: "00", AIN1L/1R

MDIF: Single-ended/Differential Input Select for Microphone Amp
0: Single-ended input to the MIN/MINP pin. Leave the MINN pin open. (default)
1: Differential Input (MINP/MINN pin)

MOMIX: Mixing Switch for Mono ADC (Table 3)
Initial: "0"

DACIN: Input Selector for DAC1, 2 (Table 4)
Initial: "0"

When DACIN bit = "0", the digital ADC output is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-2 is ignored. The audio format of SDTO at loopback mode becomes mode 3 at mode 0, 1, 2, and 3, and mode 4 at mode 4, respectively. DACIN bit should be set "1" in TDM mode.

Add	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	DAC1L Volume	DAATL17	DAATL16	DAATL15	DAATL14	DAATL13	DAATL12	DAATL11	DAATL10
06H	DAC1R Volume	DAATR17	DAATR16	DAATR15	DAATR14	DAATR13	DAATR12	DAATR11	DAATR10
07H	DAC2L Volume	DAATL27	DAATL26	DAATL25	DAATL24	DAATL23	DAATL22	DAATL21	DAATL20
08H	DAC2R Volume	DAATR27	DAATR26	DAATR25	DAATR24	DAATR23	DAATR22	DAATR21	DAATR20
09H	DOUT3 Volume	DAAT37	DAAT36	DAAT35	DAAT34	DAAT33	DAAT32	DAAT31	DAAT30
0BH	ADC Volume	SADATL7	SADATL6	SADATL5	SADATL4	SADATL3	SADATL2	SADATL1	SADATL0
0CH	ADC Volume	SADATR7	SADATR6	SADATR5	SADATR4	SADATR3	SADATR2	SADATR1	SADATR0
0DH	Monaural ADC Volume	MADAT7	MADAT6	MADAT5	MADAT4	MADAT3	MADAT2	MADAT1	MADAT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DAATL1/R17-10, DAATL2/R27-20, DAAT37-30, SADATL/R7-0, MADAT7-0: Attenuation Level (Table 7, Table 8)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	DOUT4 Volume	DAAT47	DAAT46	DAAT45	DAAT44	DAAT43	DAAT42	DAAT41	DAAT40
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

DAAT47-40: Attenuation level of DOUT4 Digital Attenuator (Table 9)
DAAT47-40: "FF" (MUTE) (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Microphone Gain	0	0	0	0	0	MGAIN2	MGAIN1	MGAIN0
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MGAIN2-0: Microphone-Amp Gain Control (Table 12)
MGAIN2-0: "000" (0dB) (default)

SYSTEM DESIGN

Figure 39 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

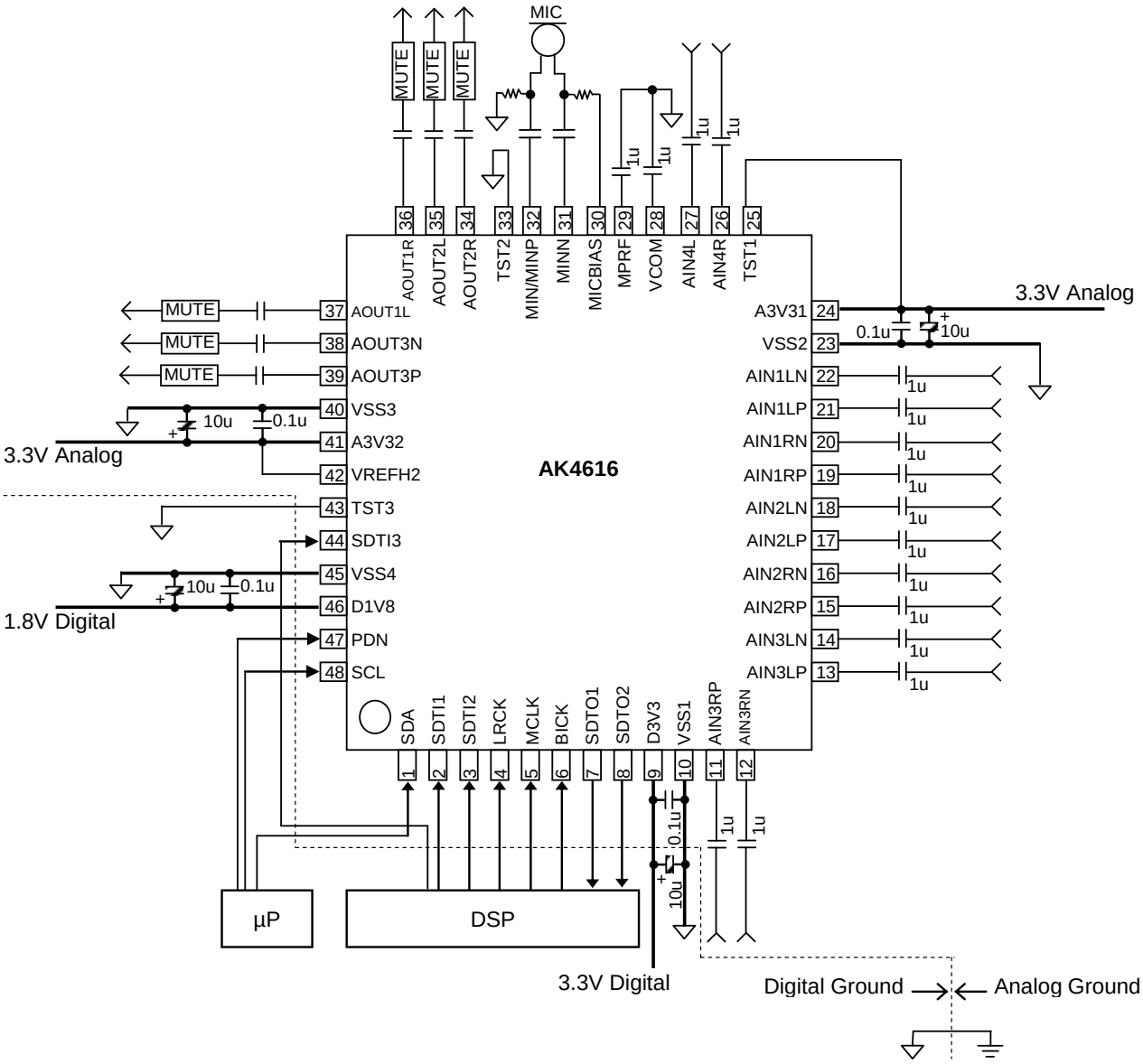


Figure 39. Typical Connection Diagram1

1. Grounding and Power Supply Decoupling

The AK4616 requires careful attention to power supply and grounding arrangements. A3V31, A3V32 and D3V3 are usually supplied from analog supply in system. Alternatively if A3V31, A3V32 and D3V3 are supplied separately, the power up sequence is not critical. **VSS1 ~ 4 of the AK4616 must be connected to analog ground plane.** System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4616 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip and output the voltage A3V31x1/2. A ceramic capacitor 1μF to the VCOM pin eliminates the effects of high frequency noise. This capacitor should be as close to the pin as possible. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREFH2 and VCOM pins in order to avoid unwanted coupling into the AK4616.

3. Analog Inputs

The Monaural ADC inputs correspond to single-ended and differential mode, and it is able to be selected by MDIF bit. The Stereo ADC have 3 differential inputs and 1 single-ended input. The single-ended input signal range scales with the supply voltage and nominally 0.81x AVDD1 Vpp (typ). The differential input signal range between LIN(RIN)+ and LIN(RIN)− scales with the supply voltage and nominally ±0.81x AVDD1 Vpp (typ). The power supply voltage range of the AK4616 is from VSS2 to A3V31. The ADC output data format is 2's complement. The internal HPF removes the DC offset.

The AK4616 samples the analog inputs at 64fs (@ fs=48kHz). The digital filter removes noise above the stop band except for multiples of the sampling frequency of analog inputs. The AK4616 includes an anti-aliasing filter (RC filter) to attenuate a noise around the sampling frequency of analog inputs.

4. Analog Outputs

The single-ended output signal range is nominally 0.61 x VREFH2 Vpp centered around the VCOM voltage. The differential output signal range is ±0.62 x VREFH2 Vpp (typ) centered around the VCOM voltage. The differential outputs are summed externally, V_{AOUT} = [L(R)OUT+]-[L(R)OUT-] between L(R)OUT+ and L(R)OUT-. If the summing gain is 1, the output range is 4.12Vpp (typ@A3V32=3.3V). The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband, in single-ended input mode. There are no internal analog filters for differential output mode, therefore this noise should be removed by the external analog filters.

The DAC outputs have DC offsets of a few millivolts to VCOM voltage.

5. External Analog Inputs Circuit

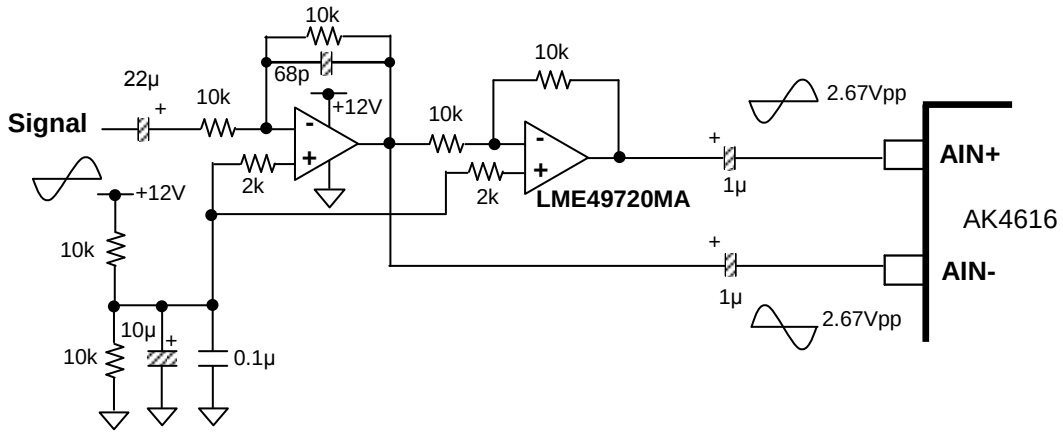


Figure 40. Input Buffer Circuit Example 1 (AC coupled single-ended input)
(AIN1LP/N, AIN1RP/N, AIN2LP/N, AIN2RP/N, AIN3LP/N, AIN3RP/N pins)

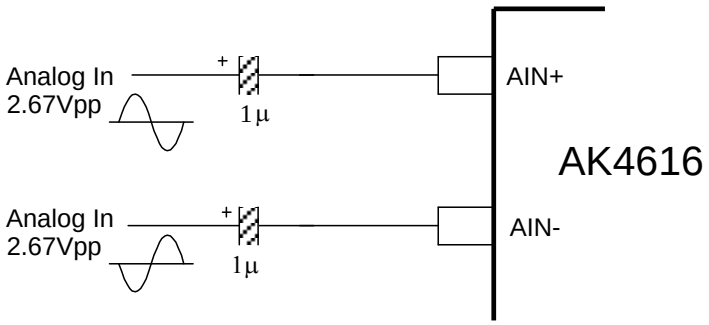


Figure 41. Input Buffer Circuit Example 2 (AC coupled differential input)
(AIN1LP/N, AIN1RP/N, AIN2LP/N, AIN2RP/N, AIN3LP/N, AIN3RP/N pins)

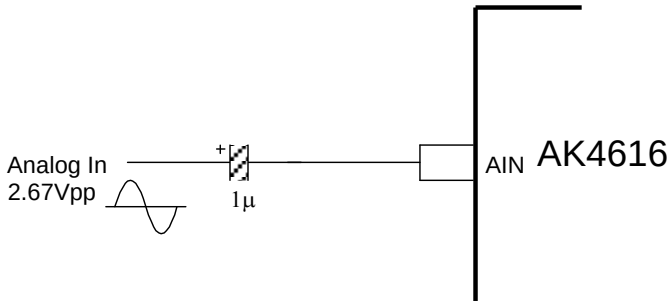


Figure 42. Input Buffer Circuit Example 3 (AC coupled single-ended input)
(AIN4L/R pins)

6. External Analog Outputs Circuit

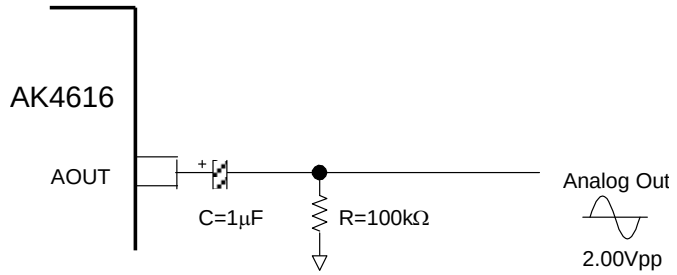


Figure 43. External LPF Circuit Example 1 (AOUT1L/R, AOUT2L/R)

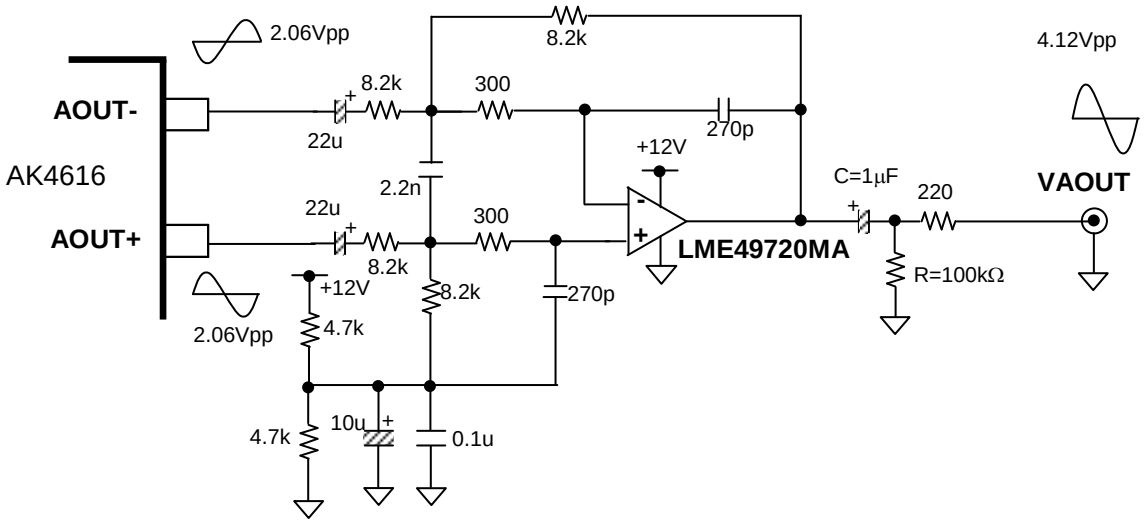


Figure 44. External LPF Circuit Example 2 (AC coupled differential output) (AOUT3P/N)

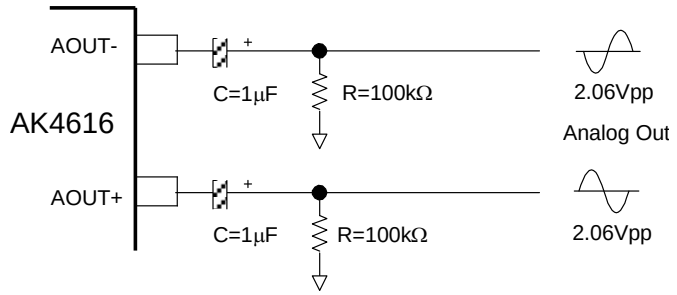


Figure 45. External LPF Circuit Example 3 (AC coupled differential output) (AOUT3P/N)

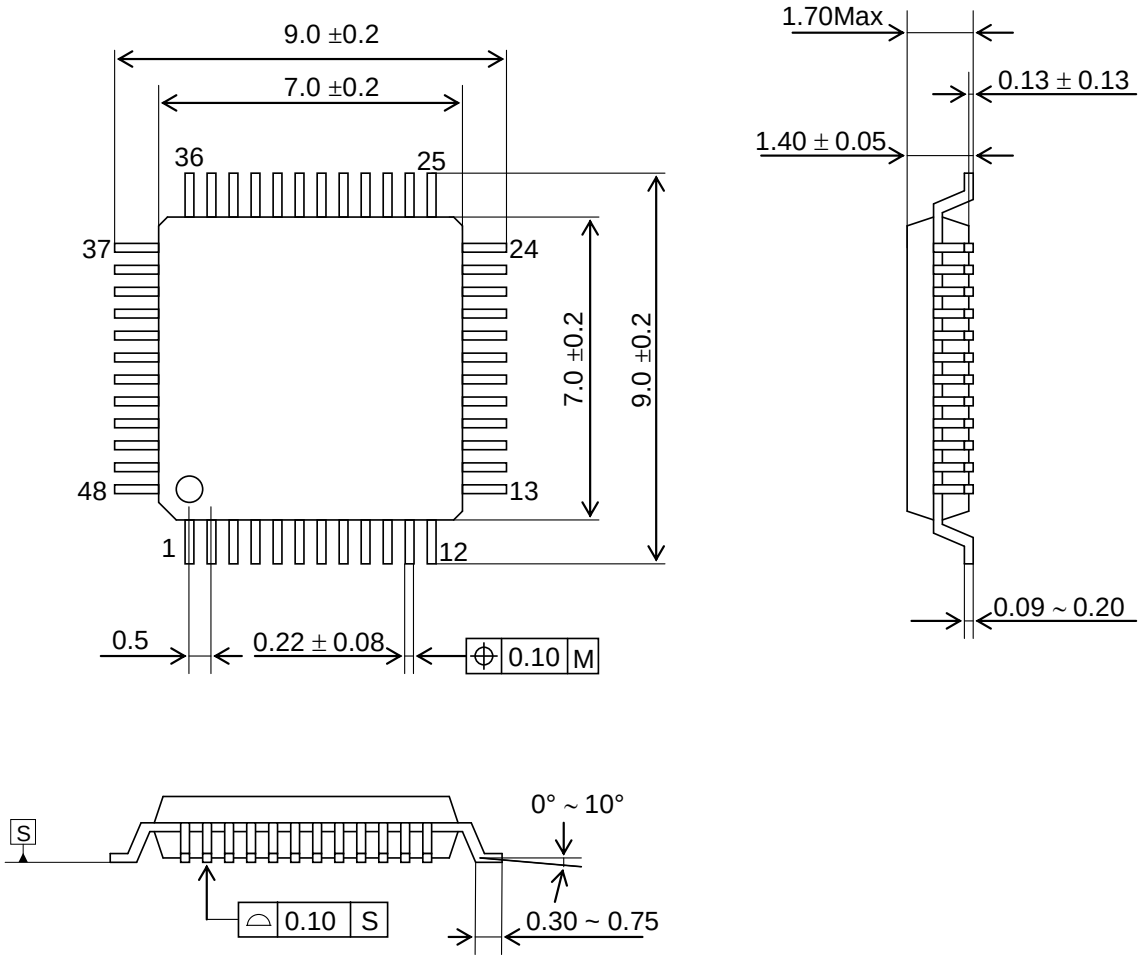
Note: The cut-offfrequency (fc) of HPF is determined by following equation.

$$fc = 1/(2 \times \pi \times R \times C)\ [Hz]$$

Where the C is the external AC coupling capacitor and the R is load resistance.
When C = 1μF and R = 100kΩ, then fs = 1.6Hz.

PACKAGE

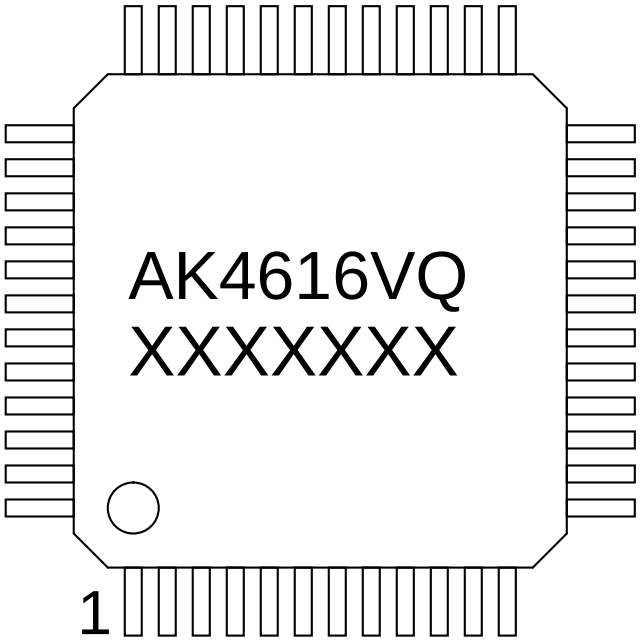
48pin LQFP(Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy resin, Halogen (Br, Cl) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4616VQ

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/11/05	00	First Edition		
12/11/14	01	Error Correction	41	SYSTEM DESIGN 2. Voltage Reference: "VREF1" was deleted.
13/07/11	02	Description Addition	15	OPERATION OCERVIEW ■ System Clock The description was changed.
13/08/23	03	Description Addition	44	PACKAGE Package dimensions were changed.
13/12/10	04	Error Correction	5	■ Handling of Unused Pin Digital: "Connect to VSS2" → "Connect to VSS1"

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