AK4629

High Performance Multi-channel Audio CODEC

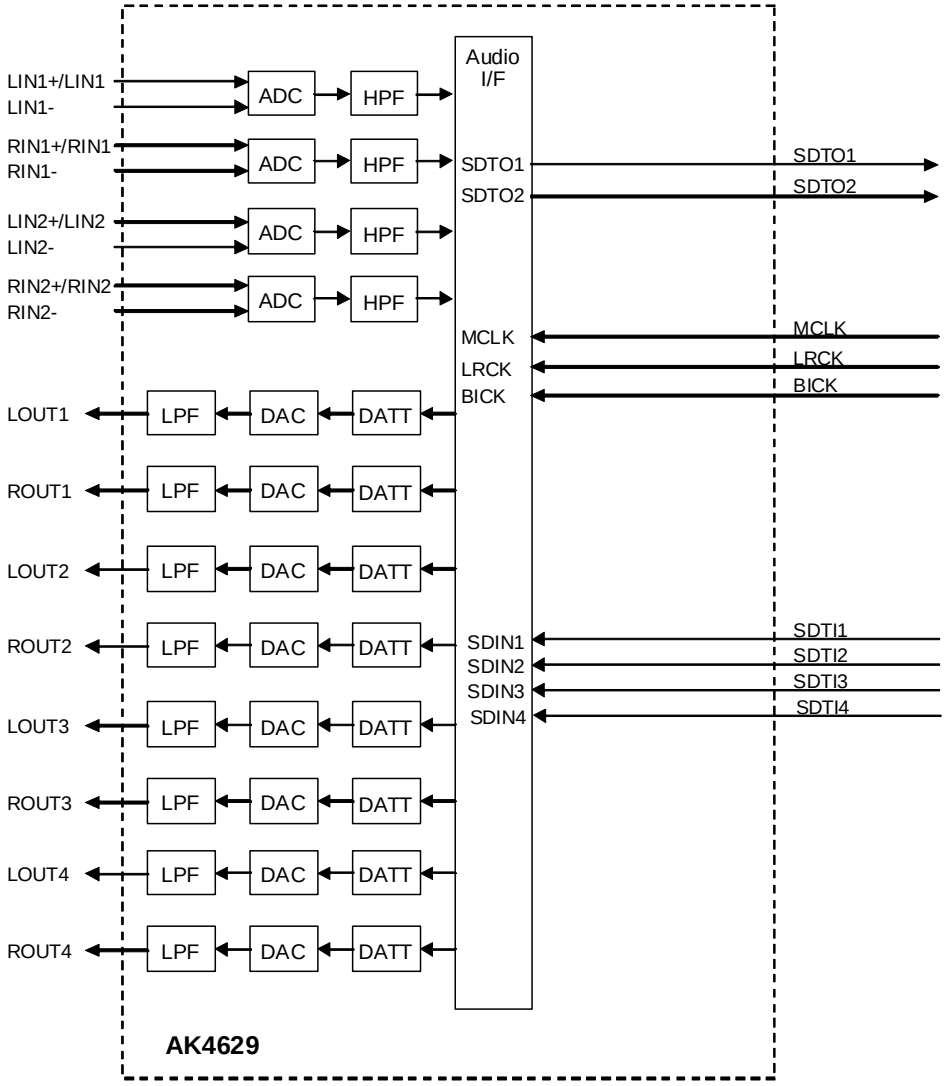
GENERAL DESCRIPTION

The AK4629 is a single chip audio CODEC that includes four ADC channels and eight DAC channels. The converters are designed with Enhanced Dual Bit architecture for the ADC's, and Advanced Multi-Bit architecture for the DAC, enabling very low noise performance. The AK4629 ADC supports both single-ended and differential inputs and outputs. A wide range of applications can be realized, including home theater, pro audio and car audio. The AK4629 is available in a 48-pin LQFP package.

FEATURES

- ☐ **4ch 24bit ADC**
  - **- 64x Oversampling**
  - **- Sampling Rate up to 96kHz**
  - **- Linear Phase Digital Anti-Alias Filter**
  - **- Single-ended / Differential Input**
  - **- S/(N+D): 92dB (Single-ended, Differential)**
  - **- Dynamic Range, S/N: 102dB (Single-ended), 103dB (Differential)**
  - **- Digital HPF for offset cancellation**
  - **- I/F format: MSB justified, I^2S or TDM**
- ☐ **8ch 24bit DAC**
  - **- 128x Oversampling**
  - **- Sampling Rate up to 192kHz**
  - **- 24bit 8 times Digital Filter**
  - **- Single-ended Outputs**
  - **- On-chip Switched-Capacitor Filter**
  - **- S/(N+D): 90dB**
  - **- Dynamic Range, S/N: 106dB**
  - **- I/F format: MSB justified, LSB justified(20bit,24bit), I^2S or TDM**
  - **- Individual channel digital volume with 128 levels and 0.5dB step**
  - **- Soft mute**
  - **- De-emphasis for 32kHz, 44.1kHz and 48kHz**
  - **- Zero Detect Function**
- ☐ **High Jitter Tolerance**
- ☐ **TTL Level Digital I/F**
- ☐ **3-wire Serial and I^2C Bus µP I/F for mode setting**
- ☐ **Master clock: 256fs, 384fs or 512fs for fs=32kHz to 48kHz**
  128fs, 192fs or 256fs for fs=64kHz to 96kHz
  128fs for fs=120kHz to 192kHz
- ☐ **Power Supply: 4.5 to 5.5V**
- ☐ **Power Supply for output buffer: 2.7 to 5.5V**
- ☐ **Small 48pin LQFP**

■ Block Diagram

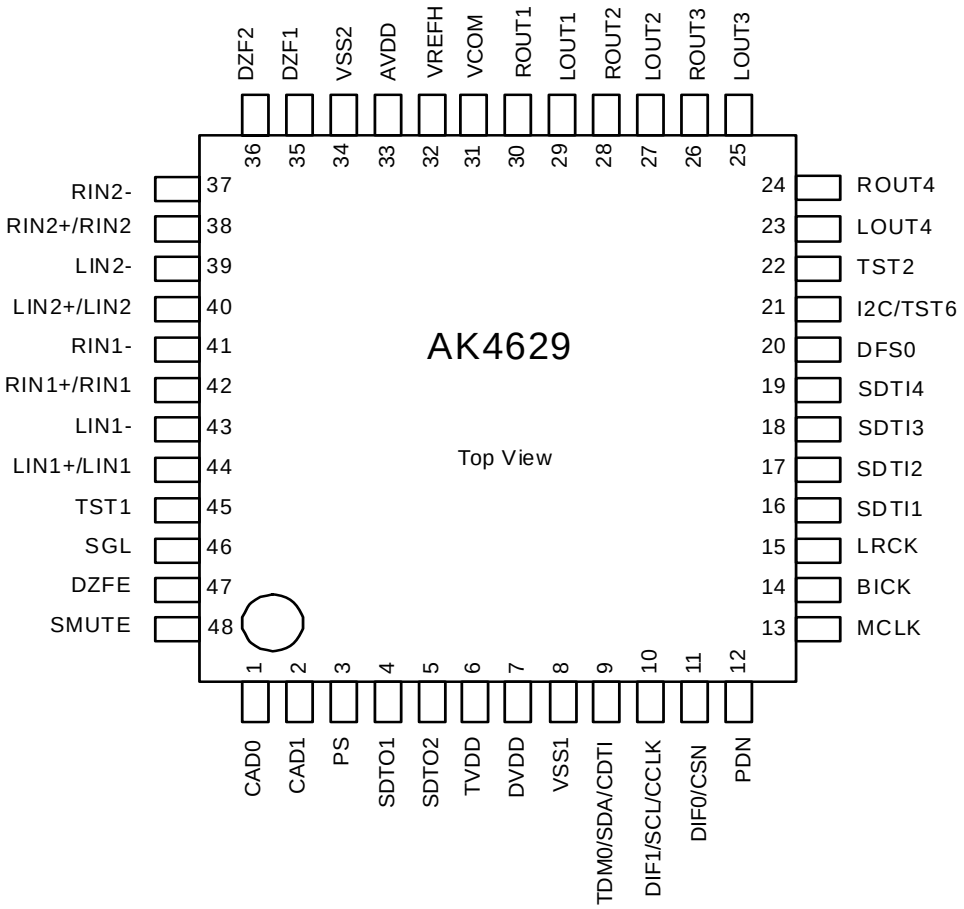


Block Diagram

■ Ordering Guide

AK4629VQ	-40 ~ +105°C	48pin LQFP(0.5mm pitch)
AKD4629	Evaluation Board for AK4629	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	CAD0	I	Chip Address 0 Pin
2	CAD1	I	Chip Address 1 Pin
3	PS	I	Parallel/Serial Select Pin "L": Serial control mode, "H": Parallel control mode
4	SDTO1	O	ADC1 Audio Serial Data Output Pin
5	SDTO2	O	ADC2 Audio Serial Data Output Pin
6	TVDD	-	Output Buffer Power Supply Pin, 2.7V~5.5V
7	DVDD	-	Digital Power Supply Pin, 4.5V~5.5V
8	VSS1	-	Digital Ground Pin, 0V
9	TDM0	I	TDM I/F Format Mode Pin in parallel control mode "L": Normal mode, "H": TDM mode
	SDA/CDTI	I/O	Control Data Input Pin in serial control mode I2C pin= "L": CDTI (3-wire Serial), I2C pin= "H": SDA (I^2C Bus)
10	DIF1	I	Audio Data Interface Format 1 Pin in parallel control mode
	SCL/CCLK	I	Control Data Clock Pin in serial control mode I2C pin= "L": CCLK (3-wire Serial), I2C pin= "H": SCL (I^2C Bus)
11	DIF0	I	Audio Data Interface Format 0 Pin in parallel control mode
	CSN	I	Chip Select Pin in 3-wire serial control mode This pin should be connected to DVDD at I^2C bus control mode
12	PDN	I	Power-Down & Reset Pin When "L", the AK4629 is powered-down and the control registers are reset to default state. If the state of the PS pin or CAD1-0 changes, then the AK4629 must be reset by the PDN pin.
13	MCLK	I	Master Clock Input Pin
14	BICK	I	Audio Serial Data Clock Pin
15	LRCK	I	Input Channel Clock Pin
16	SDTI1	I	DAC1 Audio Serial Data Input Pin
17	SDTI2	I	DAC2 Audio Serial Data Input Pin
18	SDTI3	I	DAC3 Audio Serial Data Input Pin
19	SDTI4	I	DAC4 Audio Serial Data Input Pin
20	DFS0	I	Double Speed Sampling Mode Pin (Note 1) "L": Normal Speed, "H": Double Speed
21	I2C	I	Control Mode Select Pin (PS pin = "L") "L": 3-wire Serial, "H": I^2C Bus
	TST6	I	Test Pin (PS pin = "H") This pin should be connected to VSS1
22	TST2		Test Pin This pin should be connected to VSS1.
23	LOUT4	O	DAC4 Lch Analog Output Pin
24	ROUT4	O	DAC4 Rch Analog Output Pin
25	LOUT3	O	DAC3 Lch Analog Output Pin
26	ROUT3	O	DAC3 Rch Analog Output Pin
27	LOUT2	O	DAC2 Lch Analog Output Pin
28	ROUT2	O	DAC2 Rch Analog Output Pin
29	LOUT1	O	DAC1 Lch Analog Output Pin
30	ROUT1	O	DAC1 Rch Analog Output Pin

No.	Pin Name	I/O	Function
31	VCOM	O	Common Voltage Output Pin, AVDD/2 Large external capacitor around 2.2μF is used to reduce power-supply noise.
32	VREFH	I	Positive Voltage Reference Input Pin, AVDD
33	AVDD	-	Analog Power Supply Pin, 4.5V~5.5V
34	VSS2	-	Analog Ground Pin, 0V
35	DZF1	O	Zero Input Detect 1 Pin (Note 2) When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PWDAN pin is "L", this pin goes to "H". It always is in "L" when PS pin is "H".
36	DZF2	O	Zero Input Detect 2 Pin (Note 2) When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PWDAN pin is "L", this pin goes to "H". It always is in "L" when PS pin is "H".
37	RIN2-	I	ADC2 Rch Analog Negative Input Pin (SGL pin = "L")
38	RIN2+	I	ADC2 Rch Analog Positive Input Pin (SGL pin = "L")
	RIN2	I	ADC2 Rch Analog Input Pin (SGL pin = "H")
39	LIN2-	I	ADC2 Lch Analog Negative Input Pin (SGL pin = "L")
40	LIN2+		ADC2 Lch Analog Positive Input Pin (SGL pin = "L")
	LIN2	I	ADC2 Lch Analog Input Pin (SGL pin = "H")
41	RIN1-	I	ADC1 Rch Analog Negative Input Pin (SGL pin = "L")
42	RIN1+	I	ADC1 Rch Analog Positive Input Pin (SGL pin = "L")
	RIN1	I	ADC1 Rch Analog Input Pin (SGL pin = "H")
43	LIN1-	I	ADC1 Lch Analog Negative Input Pin (SGL pin = "L")
44	LIN1+	I	ADC1 Lch Analog Positive Input Pin (SGL pin = "L")
	LIN1	I	ADC1 Lch Analog Input Pin (SGL pin = "H")
45	TST1	I	Test Pin This pin should be connected to VSS1.
46	SGL	I	Single-ended Input Mode Select Pin. "L": ADC Differential Input Mode "H": ADC Single-ended Input Mode
47	DZFE	I	Zero Input Detect Enable Pin "L": mode 7 (disable) at parallel mode, zero detect mode is selectable by DZFM3-0 bits at serial mode "H": mode 0 (DZF1 is AND of all six channels)
48	SMUTE	I	Soft Mute Pin (Note 1) When this pin goes to "H", soft mute cycle is initialized. When returning to "L", the output mute releases.

Note 1. SMUTE and DFS0 pins are ORed with register data when the PS pin= "L".

Note 2. The output pin (DZF1 and DZF2) of zero detection results of each lineout channels can be selected by DZFM3-0 bits when the PS pin and DZFE pin= "L". (Table 11)

Note 3. All digital input pins except for pull-down should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 4)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	Output buffer	TVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (power applied) (Note 6)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 4. All voltages with respect to ground.
Note 5. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 6. In case that PCB wiring density is 100% or more.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; Note 4)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 7)	Analog	AVDD	4.5	5.0	5.5	V
	Digital	DVDD	4.5	5.0	5.5	V
	Output buffer	TVDD	2.7	5.0	5.5	V

Note 4. All voltages with respect to ground.
Note 7. The power up sequence between AVDD, DVDD and TVDD is not critical. Do not turn off only the AK4629 under the condition that a surrounding device is powered on and the I^2C bus is in use.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=TVDD=5V; VSS1=VSS2=0V; VREFH=AVDD; fs=48kHz; BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at 48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
ADC Analog Input Characteristics (Single-ended Inputs)					
Resolution				24	Bits
S/(N+D) (-0.5dBFS)	fs=48kHz	84	96		dB
	fs=96kHz	-	92		dB
DR (-60dBFS)	fs=48kHz, A-weighted	94	102		dB
	fs=96kHz	88	99		dB
	fs=96kHz, A-weighted	93	105		dB
S/N (Note 11)	fs=48kHz, A-weighted	94	102		dB
	fs=96kHz	88	99		dB
	fs=96kHz, A-weighted	93	105		dB
Interchannel Isolation		90	110		dB
DC Accuracy (Single-ended Inputs)					
Interchannel Gain Mismatch			0.2	0.3	dB
Gain Drift			20	-	ppm/°C
Input Voltage	AIN=0.68xVREFH	3.2	3.4	3.6	Vpp
Input Resistance	fs=48kHz	10	14		kΩ
	fs=96kHz		11		kΩ
Power Supply Rejection (Note 9)			50		dB
ADC Analog Input Characteristics (Differential inputs)					
S/(N+D) (-0.5dBFS)	fs=48kHz	84	96		dB
	fs=96kHz	-	94		dB
DR (-60dBFS)	fs=48kHz, A-weighted	95	103		dB
	fs=96kHz	89	100		dB
	fs=96kHz, A-weighted	94	106		dB
S/N (Note 11)	fs=48kHz, A-weighted	95	103		dB
	fs=96kHz	89	100		dB
	fs=96kHz, A-weighted	94	106		dB
Interchannel Isolation		90	110		dB
DC Accuracy (Differential inputs)					
Interchannel Gain Mismatch			0.2	0.3	dB
Gain Drift			20	-	ppm/°C
Input Voltage	AIN=0.68xVREFH (Note 8)	±3.2	±3.4	±3.6	Vpp
Input Resistance	fs=48kHz	22	32		kΩ
	fs=96kHz		19		kΩ
Power Supply Rejection (Note 9)			50	-	dB
Common Mode Rejection Ratio (CMRR) (Note 10)		60			dB

DAC Analog Output Characteristics						
Resolution					24	Bits
S/(N+D)	(0dBFS)	fs=48kHz	80	98		dB
		fs=96kHz	78	98		dB
		fs=192kHz	-	98		dB
DR	(-60dBFS)	fs=48kHz, A-weighted	95	106		dB
		fs=96kHz	88	100		dB
		fs=96kHz, A-weighted	94	106		dB
		fs=192kHz	-	100		dB
		fs=192kHz, A-weighted	-	106		dB
S/N	(Note 12)	fs=48kHz, A-weighted	95	106		dB
		fs=96kHz	88	100		dB
		fs=96kHz, A-weighted	94	106		dB
		fs=192kHz	-	100		dB
		fs=192kHz, A-weighted	-	106		dB
Interchannel Isolation			90	110		dB
DC Accuracy						
Interchannel Gain Mismatch				0.2	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage		AOUT=0.6xVREFH	2.75	3.0	3.25	Vpp
Load Resistance			5			kΩ
Load Capacitance					25	pF
Power Supply Rejection		(Note 10)		50		dB

Note 8. (LIN+) – (LIN-) or (RIN+) – (RIN-); this value is proportional to VREFH voltage.
Note 9. PSR is applied to AVDD, DVDD and TVDD with 1kHz, 50mVpp. VREFH pin is held +5V.
Note 10. VREFH is held +5V, the input bias voltage is set to AVDD1, AVDD2 x 0.5. The 1kHz, 1.52Vpp signal is applied to LIN- and LIN+ with same phase (e.g. shorted) or RIN- and RIN+. The CMRR is measured as the attenuation level from 1.52Vpp = -7dBFS.
Note 11. S/N measured by CCIR-ARM is 98dB(@fs=48kHz).
Note 12. S/N measured by CCIR-ARM is 102dB(@fs=48kHz).

Parameter			min	typ	max	Unit
Power Supplies						
Power Supply Current (AVDD+DVDD+TVDD)						
Normal Operation (PDN = "H")						
AVDD	fs=48kHz, 96kHz			57	86	mA
	fs=192kHz			34	51	mA
DVDD+TVDD	fs=48kHz	(Note 13)		19	29	mA
	fs=96kHz			27	40	mA
	fs=192kHz			27	40	mA
Power-down mode (PDN = "L")		(Note 14)		80	200	μA

Note 13. TVDD=0.1mA(typ).
Note 14. In the power-down mode. All digital input pins including clock pins (MCLK, BICK, LRCK) are held VSS1.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=4.5~5.5V; TVDD=2.7~5.5V; fs=48kHz)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 15)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note 16)		GD		16		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 15)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note 15)	-0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 16)		GD		19.2		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz	(Note 17)	FR		±0.3		dB
80.0kHz	(Note 17)	FR		±1.0		dB

Note 15. The passband and stopband frequencies scale with fs.
For example, 21.8kHz at –0.1dB is 0.454 x fs.

Note 16. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 20/24bit data of both channels on input register to the output of analog signal.

Note 17. 40.0kHz; fs=96kHz , 80.0kHz; fs=192kHz.

DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=4.5~5.5V; TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage					
(SDTO1-2 pins: Iout=-100μA)	VOH	TVDD-0.5	-	-	V
(DZF1, DZF2 pins: Iout=-100μA)	VOH	AVDD-0.5	-	-	V
Low-Level Output Voltage					
(SDTO1-2, DZF1, DZF2 pins: Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=4.5~5.5V; TVDD=2.7~5.5V; C_L=20pF)

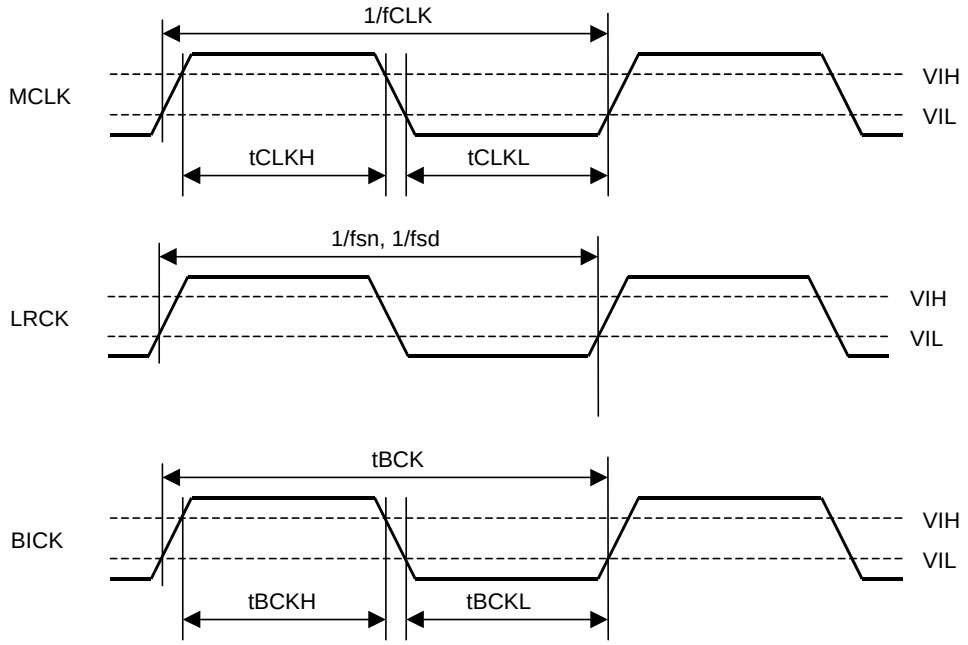
Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
256fsn, 128fsd:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	27			ns
Pulse Width High	tCLKH	27			ns
384fsn, 192fsd:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
512fsn, 256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	15			ns
Pulse Width High	tCLKH	15			ns
LRCK Timing					
Normal mode (TDM0= "0", TDM1= "0")					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM0= "1", TDM1= "0")					
LRCK frequency	fsn	32		48	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (TDM0= "1", TDM1= "1")					
LRCK frequency	fsn	64		96	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
Audio Interface Timing					
Normal mode (TDM0= "0", TDM1= "0")					ns
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	20			ns
LRCK to SDTO(MSB)	tLRS			40	ns
BICK "↓" to SDTO1-2	tBSD			40	ns
SDTI1-4 Hold Time	tSDH	20			ns
SDTI1-4 Setup Time	tSDS	20			ns
TDM256 mode (TDM0= "1", TDM1= "0")					ns
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	20			ns
BICK "↓" to SDTO1	tBSD			20	ns
SDTI1 Hold Time	tSDH	10			ns
SDTI1 Setup Time	tSDS	10			ns
TDM128 mode (TDM0= "1", TDM1= "1")					ns
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	20			ns
BICK "↓" to SDTO1	tBSD			20	ns
SDTI1-2 Hold Time	tSDH	10			ns
SDTI1-2 Setup Time	tSDS	10			ns

Note 18. BICK rising edge must not occur at the same time as LRCK edge.

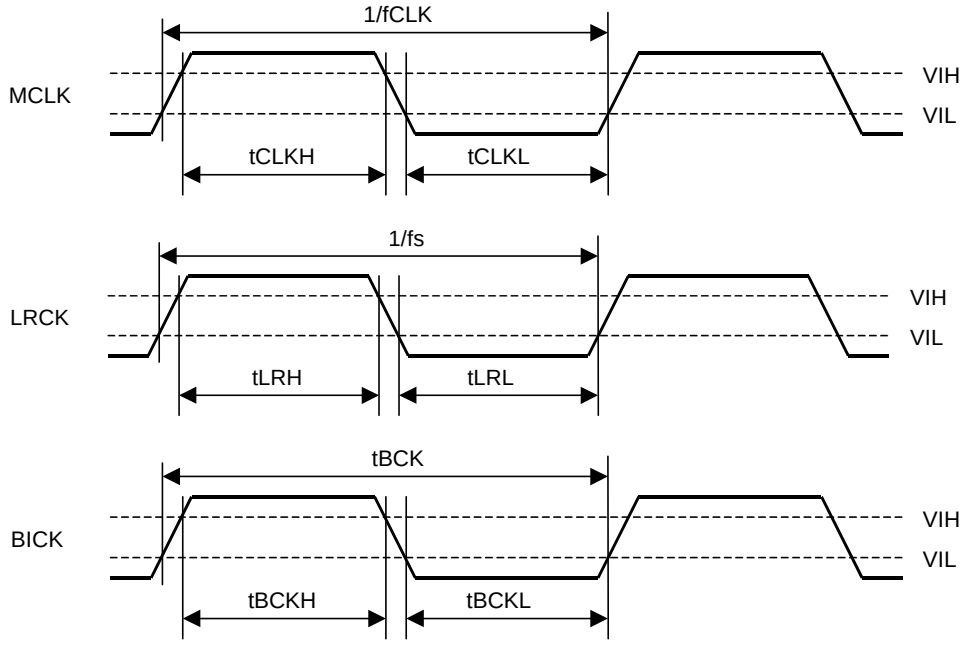
Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 19)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 20)	tPD	150			ns
PDN "↑" to SDTO1-2 valid (Note 21)	tPDV		522		1/fs

Note 19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 20. The AK4629 can be reset by bringing the PDN pin "L" to "H" upon power-up.
Note 21. These cycles are the number of LRCK rising from the PDN pin rising edge.
Note 22. I^2C-bus is a trademark of NXP B.V.

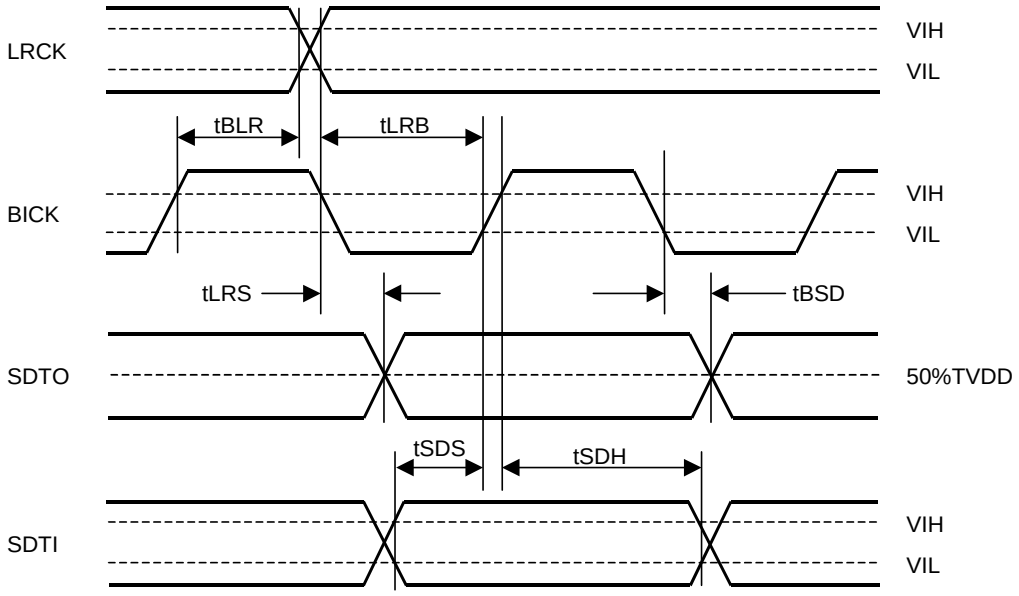
■ **Timing Diagram**



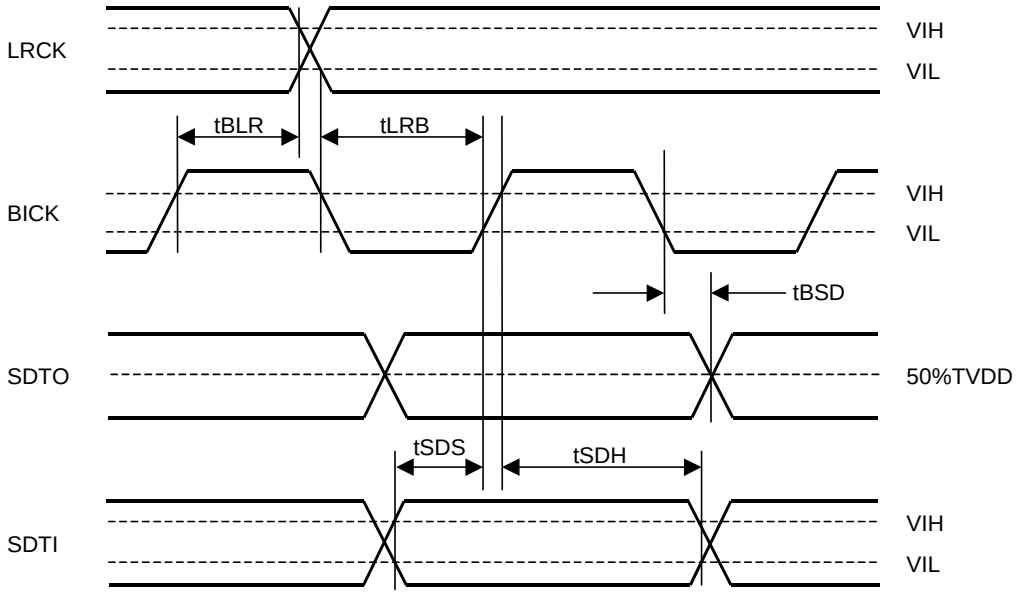
Clock Timing (TDM0 bit= "0")



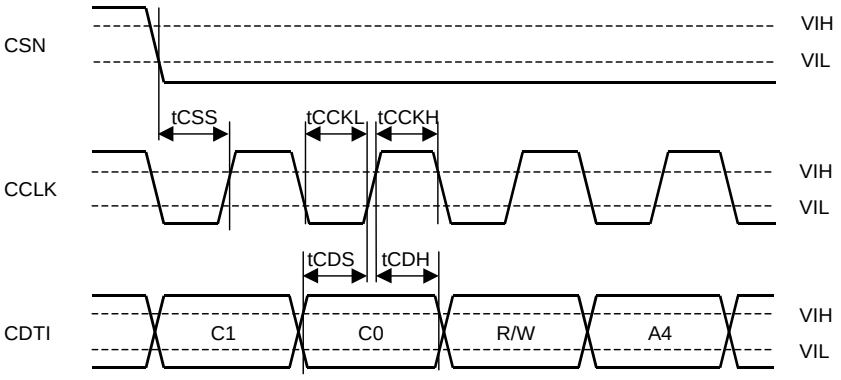
Clock Timing (TDM0 bit= "1")



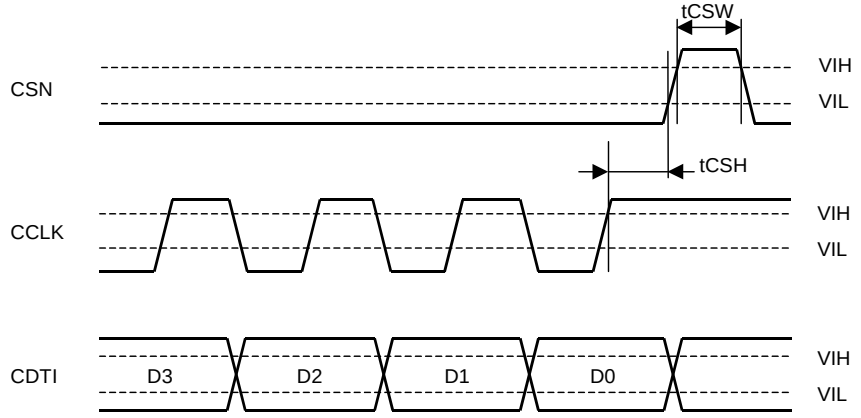
Audio Interface Timing (TDM0 bit= "0")



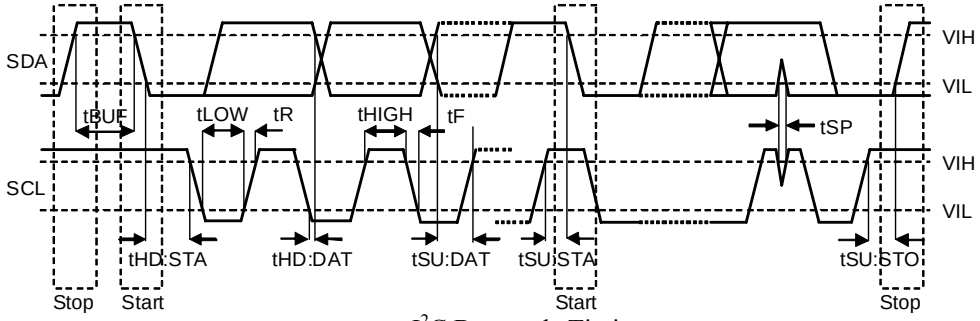
Audio Interface Timing (TDM0 bit= "1")



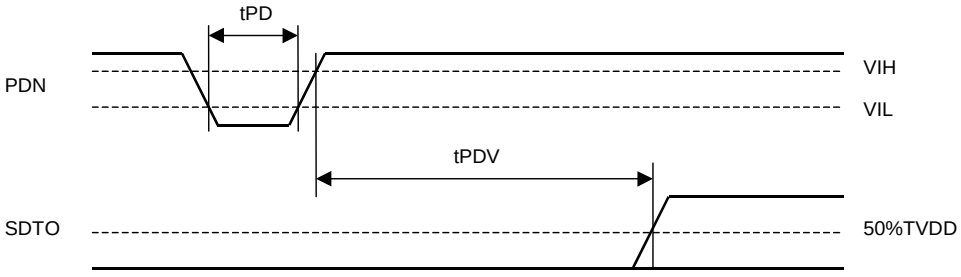
WRITE Command Input Timing (3-wire Serial mode)



WRITE Data Input Timing (3-wire Serial mode)



I^{2}C Bus mode Timing



Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4629, are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by DFS0 and DFS1 bits (Table 1). The frequency of MCLK at each sampling speed is set automatically (Table 2, Table 3, Table 4). In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 5) and the internal master clock becomes the appropriate frequency (Table 6), it is not necessary to set DFS bits.

The AK4629 is automatically placed in power saving mode when MCLK or LRCK is stopped during normal operation mode, and the analog output goes to VCOM (typ). When MCLK and LRCK are input again, the AK4629 is powered up. After exiting reset following power-up, the AK4629 is not fully operational until MCLK and LRCK are input.

DFS1	DFS0	Sampling Speed (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)			BICK (MHz)
fs	128fs	192fs	256fs	64fs
88.2kHz	11.2896	16.9344	22.5792	5.6448
96.0kHz	12.2880	18.4320	24.5760	6.1440

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)
(Note: At Double speed mode(DFS1 bit= "0", DFS0 bit= "1"), 128fs and 192fs are not available for ADC.)

LRCK	MCLK (MHz)			BICK (MHz)
fs	128fs	192fs	256fs	64fs
176.4kHz	22.5792	-	-	11.2896
192.0kHz	24.5760	-	-	12.2880

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)
(Note: At Quad speed mode(DFS1bit= "1", DFS0 bit= "0") are not available for ADC.)

MCLK	Sampling Speed
512fs	Normal
256fs	Double
128fs	Quad

Table 5. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)			Sampling Speed
fs	128fs	256fs	512fs	
32.0kHz	-	-	16.3840	Normal
44.1kHz	-	-	22.5792	
48.0kHz	-	-	24.5760	
88.2kHz	-	22.5792	-	Double
96.0kHz	-	24.5760	-	
176.4kHz	22.5792	-	-	Quad
192.0kHz	24.5760	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Differential/Single-ended Input selection

The AK4629 supports differential inputs (Figure 1) by setting the SGL pin = "L", and single-ended inputs (Figure 2) by setting the SGL pin= "H". When single-ended input mode, L/RIN1-2 pins should be open, because L/RIN1-2 pins output an invert signal of the input signal. The AK4629 includes an anti-aliasing filter (RC filter) for both differential input and the single-ended input.

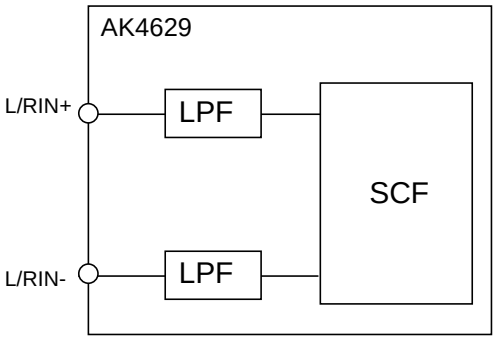


Figure 1. Differential Input (SGL pin = "L")

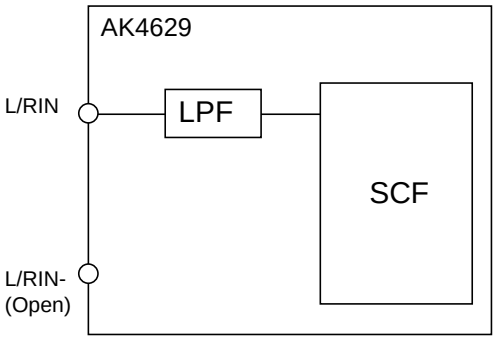


Figure 2. Single-ended Input (SGL pin = "H")

■ De-emphasis Filter

The AK4629 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. De-emphasis filter is not available in Double Speed Mode and Quad Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by register data of DEMA1-D0 (DAC1: DEMA1-0, DAC2: DEMB1-0, DAC3: DEMC1-0, DAC4: DEMD1-0 see "Register Definitions").

Mode	Sampling Speed	DEM1	DEM0	DEM	
0	Normal Speed	0	0	44.1kHz	
1	Normal Speed	0	1	OFF	(default)
2	Normal Speed	1	0	48kHz	
3	Normal Speed	1	1	32kHz	

Table 7. De-emphasis control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and scales with sampling rate (fs).

■ Audio Serial Interface Format

When TDM1 bit = "0" and TDM0 pin = "L" or when TDM1-0 bits = "00", four modes can be selected by the DIF1-0 bits as shown in Table 8. In all modes the serial data is MSB-first, 2's complement format. The SDTO1-2 are clocked out on the falling edge of BICK and the SDTI1-4 are latched on the rising edge of BICK.

Mode 2, 3, 6, 7, 10, 11 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

Mode	TDM 1	TDM0	DIF1	DIF0	SDTO1-2	SDTI1-4	LRCK		BICK		
0	0	0	0	0	24bit, Left justified	20bit, Right justified	H/L	I	≥ 48fs	I	
1	0	0	0	1	24bit, Left justified	24bit, Right justified	H/L	I	≥ 48fs	I	
2	0	0	1	0	24bit, Left justified	24bit, Left justified	H/L	I	≥ 48fs	I	(default)
3	0	0	1	1	24bit, I^2S	24bit, I^2S	L/H	I	≥ 48fs	I	

Table 8. Audio data formats (Normal mode)

The audio serial interface format becomes the TDM mode when the TDM0 pin is set to "H". The serial data of all ADC (four channels) are output from the SDTO1 pin and the SDTO2 pin outputs "L". In the TDM256 mode, the serial data of all DAC (six channels) are input to the SDTI1 pin. The input data to SDTI2-4 pins are ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be 1/256fs at least. Four modes can be selected by DIF1-0 bits as shown in Table 9. In all modes the serial data is MSB-first, 2's complement format. The SDTO1 is clocked out on the falling edge of BICK and the SDTI1 is latched on the rising edge of BICK. LOOP1-0 bits should be set to "0" at the TDM mode. TDM128 Mode can be set by TDM1 bit as show in Table 10. In Double Speed Mode, the serial data of DAC (four channels; L1, R1, L2, R2) is input to the SDTI1 pin. Other two data (four channels; L3, R3, L4, L4) are input to the SDTI2 pin. The TDM0 pin (or TDM0 register) should be set to "H" (or "1") if TDM256 Mode is selected. The TDM0 register and TDM1 register should be set to "1" if Double Speed Mode is selected in TDM128 Mode.

Mode	TDM 1	TDM0	DIF1	DIF0	SDTO1	SDTI1	LRCK		BICK	
								I/O		I/O
4	0	1	0	0	24bit, Left justified	20bit, Right justified	↑	I	256fs	I
5	0	1	0	1	24bit, Left justified	24bit, Right justified	↑	I	256fs	I
6	0	1	1	0	24bit, Left justified	24bit, Left justified	↑	I	256fs	I
7	0	1	1	1	24bit, I^2S	24bit, I^2S	↓	I	256fs	I

Table 9. Audio data formats (TDM256 mode)

Mode	TDM 1	TDM0	DIF1	DIF0	SDTO1	SDTI1, SDTI2	LRCK		BICK	
								I/O		I/O
8	1	1	0	0	24bit, Left justified	20bit, Right justified	↑	I	128fs	I
9	1	1	0	1	24bit, Left justified	24bit, Right justified	↑	I	128fs	I
10	1	1	1	0	24bit, Left justified	24bit, Left justified	↑	I	128fs	I
11	1	1	1	1	24bit, I^2S	24bit, I^2S	↓	I	128fs	I

Table 10. Audio data formats (TDM128 mode)

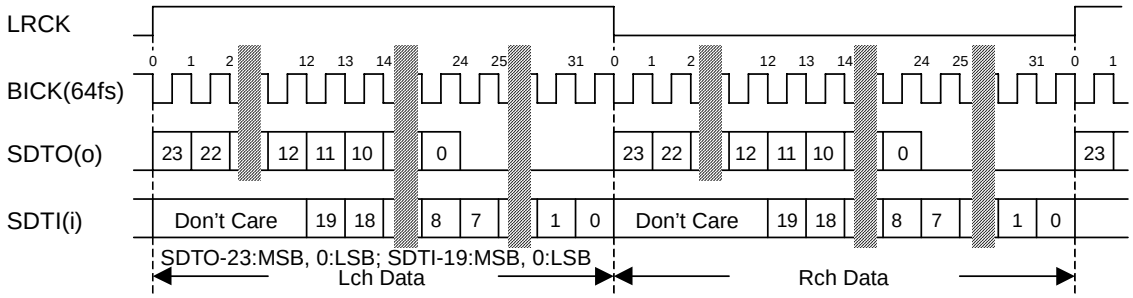


Figure 3. Mode 0 Timing

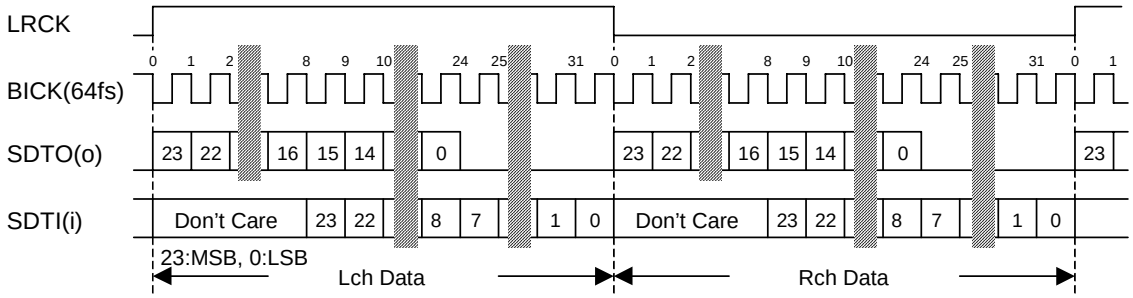


Figure 4. Mode 1 Timing

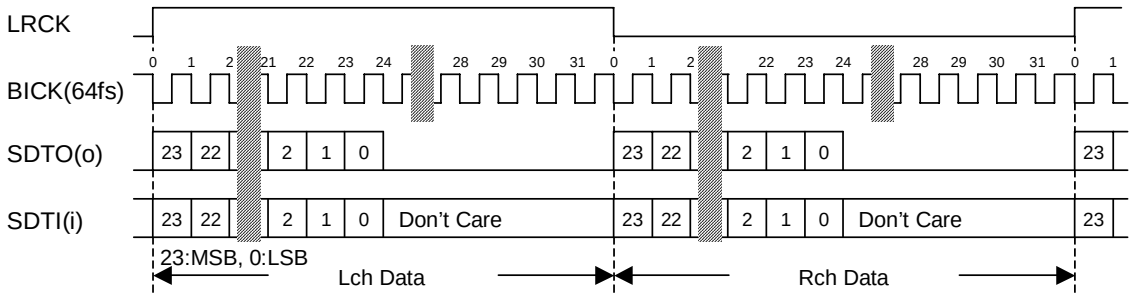


Figure 5. Mode 2 Timing

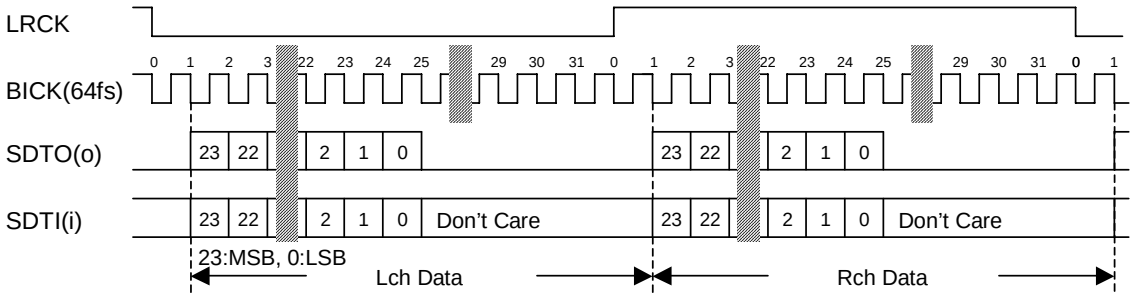


Figure 6. Mode 3 Timing

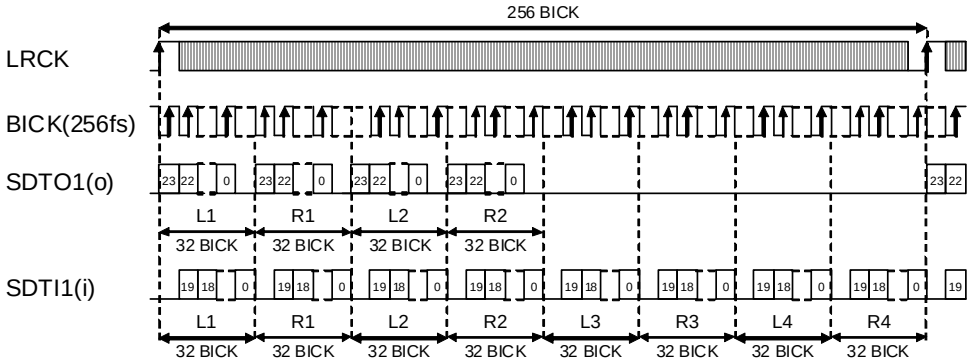


Figure 7. Mode 4 Timing

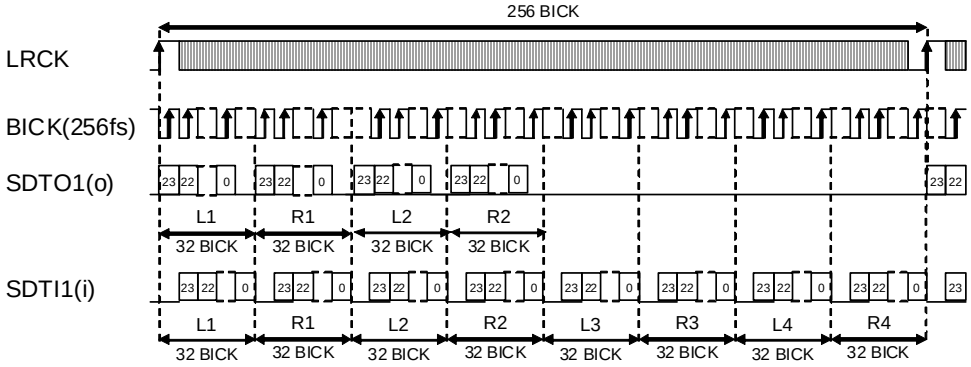


Figure 8. Mode 5 Timing

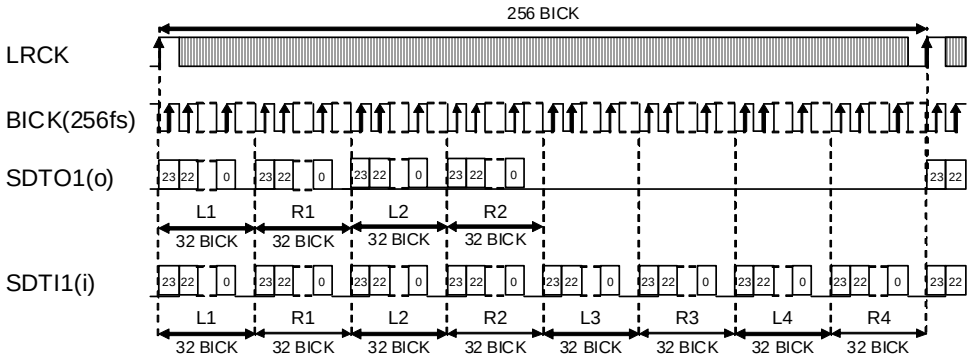


Figure 9. Mode 6 Timing

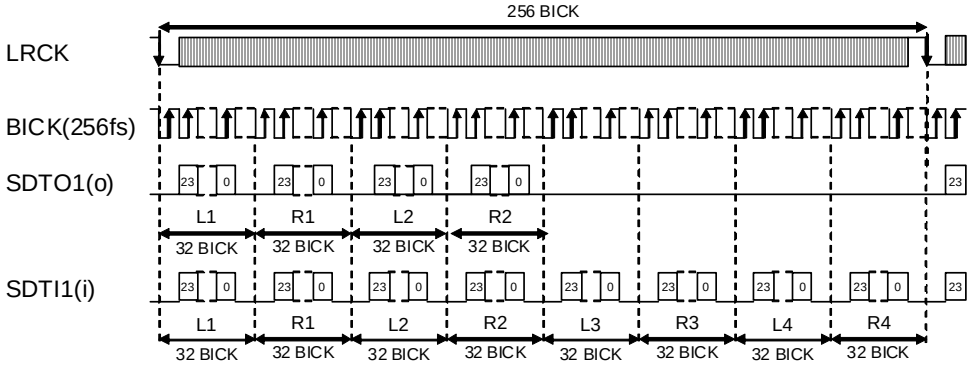


Figure 10. Mode 7 Timing

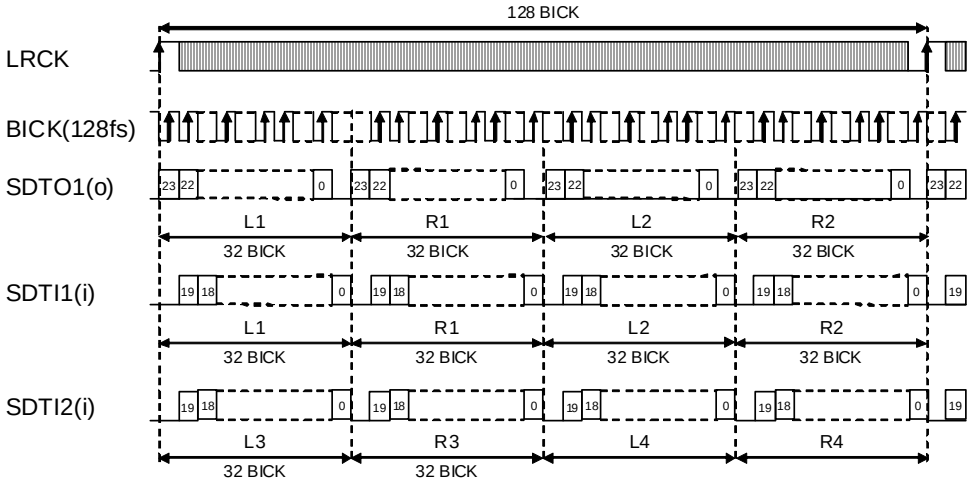


Figure 11. Mode 8 Timing

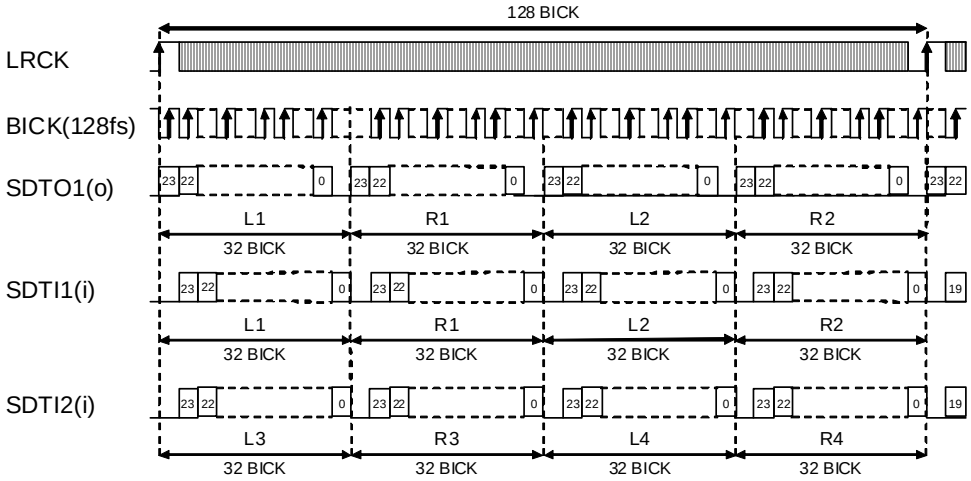


Figure 12. Mode 9 Timing

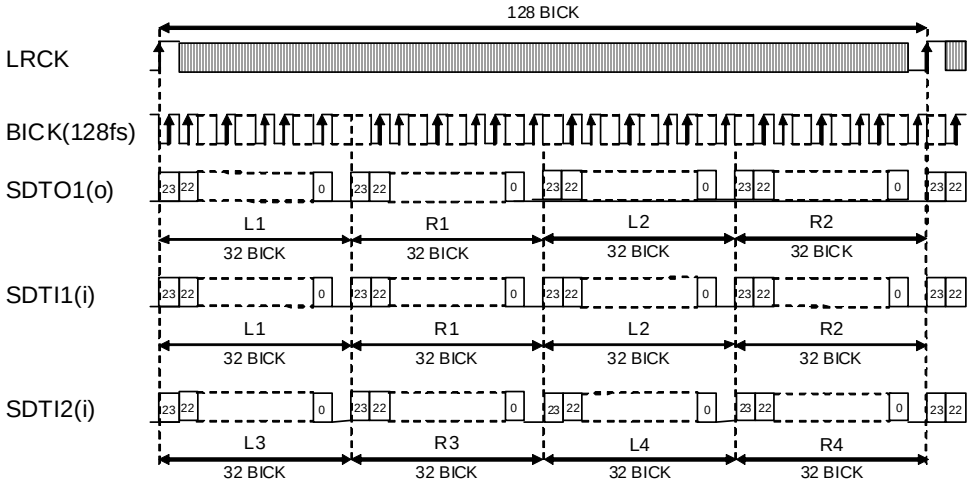


Figure 13. Mode 10 Timing

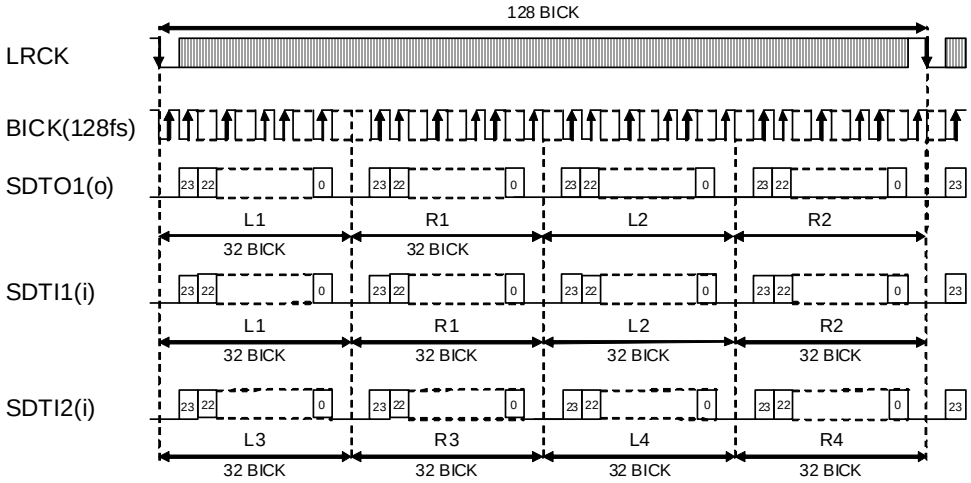


Figure 14. Mode 11 Timing

■ Zero Detection

The AK4629 has two pins for zero detect flag outputs. The output pin (DZF1 and DZF2 pins) for zero detection results of each lineout channels can be selected by DZFM3-0 bits when the PS pin and DZFE pin = "L" (Table 11). Zero detection mode is set to mode 0 when the DZFE pin= "H" regardless of the PS pin. The DZF1 pin outputs AND result of all eight channels and the DZF2 pin is disabled ("L") at mode 0.

When the input data of all lineout channels of DZF1 (DZF2) pin are continuously zeros for 8192 LRCK cycles, the DZF1 (DZF2) pin becomes "H". The DZF1 (DZF2) pin immediately returns to "L" if input data of any channel of DZF1 (DZF2) pin is not zero.

Mode	DZFM				AOUT								
	3	2	1	0	L1	R1	L2	R2	L3	R3	L4	R4	
0	0	0	0	0	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	
1	0	0	0	1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF2	DZF2	DZF2	
2	0	0	1	0	DZF1	DZF1	DZF1	DZF1	DZF2	DZF2	DZF2	DZF2	
3	0	0	1	1	DZF1	DZF1	DZF1	DZF2	DZF2	DZF2	DZF2	DZF2	
4	0	1	0	0	DZF1	DZF1	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	
5	0	1	0	1	DZF1	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	
6	0	1	1	0	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	
7	0	1	1	1	disable (DZF1=DZF2 = "L")								(default)
8	1	0	0	0	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF2	
9	1	0	0	1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF2	DZF2	
10	1	0	1	0	disable (DZF1=DZF2 = "L")								
11	1	0	1	1									
12	1	1	0	0									
13	1	1	0	1									
14	1	1	1	0									
15	1	1	1	1									

Table 11. Zero detect control

■ Digital Attenuator

The AK4629 has channel-independent digital attenuator (128 levels, 0.5dB step). Attenuation level of each channel can be set by each ATT7-0 bits (Table 12).

ATT7-0	Attenuation Level	
00H	0dB	(default)
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63dB	
7FH	MUTE (-∞)	
	:	
FEH	MUTE (-∞)	
FFH	MUTE (-∞)	

Table 12. Attenuation level of digital attenuator

Transition time between set values of ATT7-0 bits can be selected by ATS1-0 bits (Table 13). Transition between set values is soft transition. Therefore, the switching noise does not occur in the transition.

Mode	ATS1	ATS0	ATT speed	
0	0	0	1792/fs	(default)
1	0	1	896/fs	
2	1	0	256/fs	
3	1	1	256/fs	

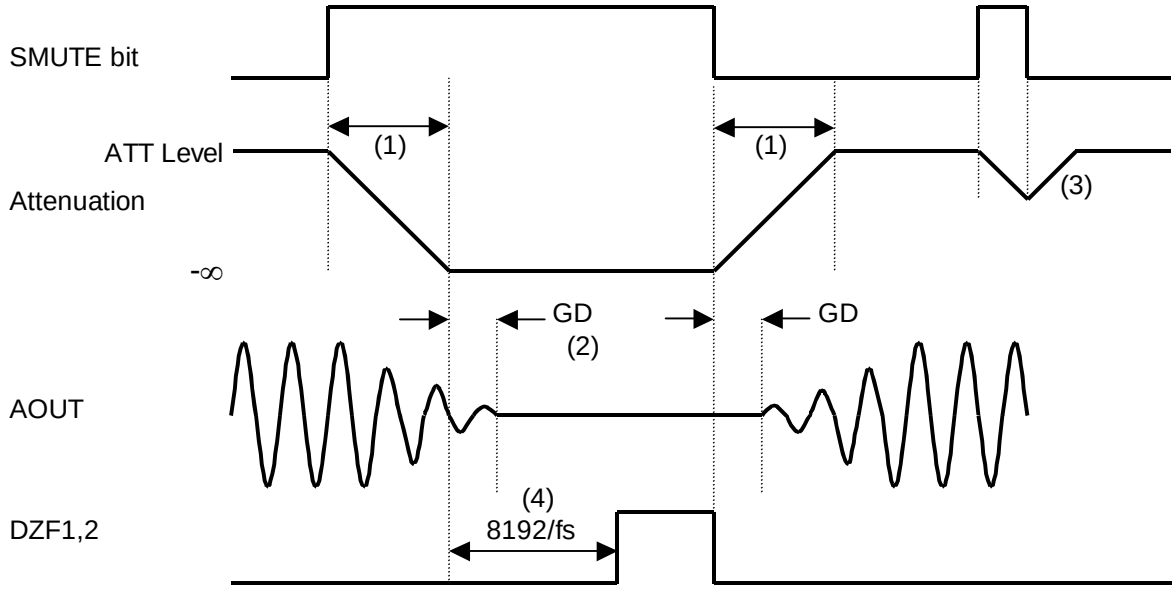
Table 13. Transition time between set values of ATT7-0 bits

The transition between set values is soft transition of 1792 levels in mode 0. It takes 1792/fs (37.3ms@fs=48kHz) from 00H(0dB) to 7FH(MUTE). When the PDN pin becomes “L”, the ATTs are initialized to 00H. The ATTs are 00H when RSTN bit= “0”. When RSTN bit return to “1”, the ATTs fade to their current value.

Note: The attenuation level is calculated in 11bit accuracy.

■ Soft mute operation

Soft mute operation is performed at digital domain. When the SMUTE pin changes to "H", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 13) from the current ATT level. When the SMUTE pin returns to "L", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 13). For example, in Normal Speed Mode, this time is 1792LRCK cycles (1792/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to 7FH

(2) The analog output corresponding to the digital input has group delay. (GD)

(3) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at all the channels of the group are continuously zeros for 8192 LRCK cycles, the DZF pin of each channel becomes "H". The DZF pin immediately returns to "L" if the input data of either channel of the group are not zero.

Figure 15. Soft mute and zero detection

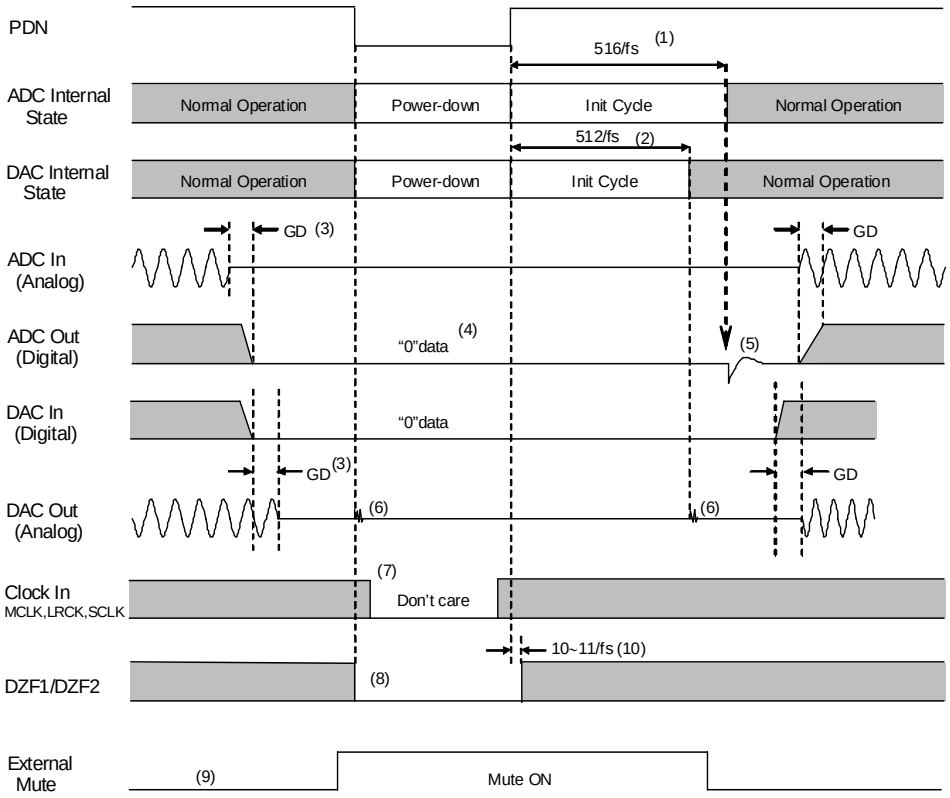
■ System Reset

The AK4629 should be reset once by bringing the PDN pin = "L" upon power-up. The AK4629 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4629 is in the power-down mode until MCLK and LRCK are input.

■ Power-Down

The ADC and DACs of AK4629 are placed in the power-down mode by bringing the PDN "L" and both digital filters are reset at the same time. Bringing the PDN pin="L" also resets the control registers to their default values. In the power-down mode, the analog outputs become to VCOM voltage and DZF1-2 pins output "L". This reset should always be made after power-up. In case of ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO1-2 become available after 516 cycles of LRCK clock. In case of the DAC, an analog initialization cycle starts after exiting the power-down mode. The analog outputs are VCOM voltage during the initialization. Figure 16 shows the power-down/up sequences.

All ADCs and all DACs can be powered-down by PWADN and PWDAN bits respectively. DAC1-4 can be power-down individually by PDDA1-4 bits. In this case, the internal register values are not initialized. When PWADN bit= "0" and PDAD1-2 bits = "0", SDTO1-2 become "L". When PWDAN bit = "0" and PDDA1-4 bits= "0", the analog outputs go to VCOM voltage and DZF1-2 pins go to "H". As some click noise occurs, the analog output should be muted externally if the click noise influences system applications.



Notes:

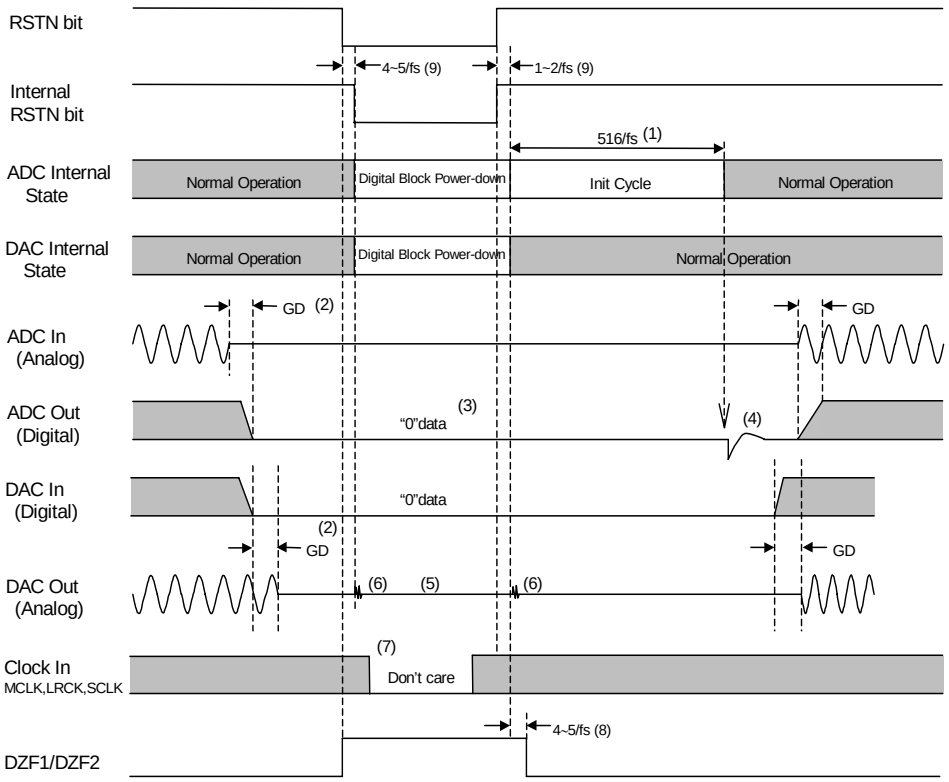
(1) The analog part of ADC is initialized after exiting the power-down state.
(2) The analog part of DAC is initialized after exiting the power-down state.
(3) Digital outputs corresponding to analog inputs and analog outputs corresponding to digital inputs have group delay (GD).
(4) ADC outputs "0" data in power-down state.
(5) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system application.
(6) Click noise occurs at the falling edge of PDN and at 512/fs after the rising edge of PDN.
(7) When the external clocks (MCLK, BICK and LRCK) are stopped, the AK4629 should be in the power-down mode.
(8) DZF pins are "L" in power-down mode (PDN pin= "L").
(9) Mute the analog output externally if the click noise (6) influences system application.
(10) DZF1-2 pins are "L" for 10~11/fs after PDN = "↑".

Figure 16. Power-down/up sequence example

■ Reset Function

(1) Reset by RSTN bit

When RSTN bit = "0", ADC and DACs are powered-down but the internal registers are not initialized. The analog outputs go to VCOM voltage, DZF1-2 pins output "H" and the SDTO1-2 pins outputs "L". As some click noise occurs, the analog output should be muted externally if the click noise influences system application. Figure 17 shows the power-up sequence.



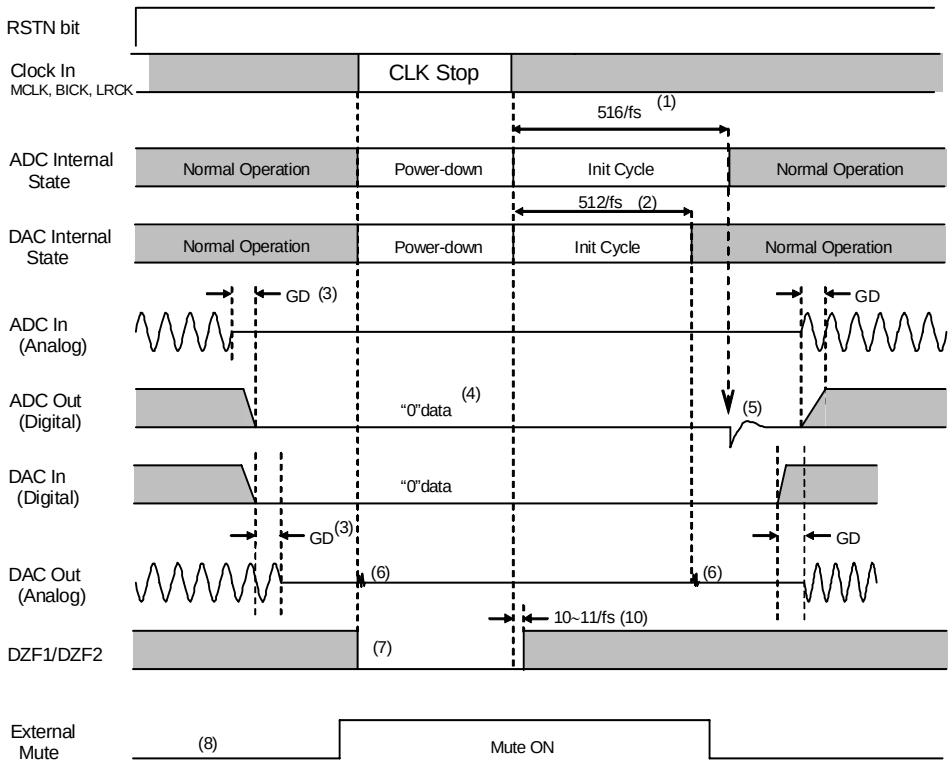
Notes:

(1) The analog part of the ADC is initialized after exiting reset state.
(2) Digital outputs corresponding to analog inputs and analog outputs corresponding to digital inputs have group delay (GD).
(3) ADC outputs "0" data in power-down state.
(4) Click noise occurs when the internal RSTN bit becomes "1". Mute the digital output externally if the click noise influences system application.
(5) The analog outputs become VCOM voltage.
(6) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and occurs at 1~2/fs after RSTN bit becomes "1". This noise is output even if "0" data is input.
(7) The external clocks (MCLK, BICK and LRCK) can be stopped in reset mode. When exiting reset mode, "1" should be written to RSTN bit after the external clocks (MCLK, BICK and LRCK) are fed.
(8) The DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 6~7/fs after RSTN bit becomes "1".
(9) There is a delay, 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

Figure 17. Reset Sequence Example

(2) Reset by MCLK, LRCK or BICK stop

The AK4629 is automatically placed in reset state when MCLK, LRCK or BICK is stopped during normal operation (RSTN pin = "H"). In this reset state, the analog output becomes VCOM voltage, and SDTO1-2, DZF1-2 pins output "L", but register values are not initialized. When MCLK, LRCK or BICK are input again, the AK4629 is powered up. After exiting reset following power-up, the ADC enters initializing cycle. Therefore, SDTO1-2 output data is not stable in 516x LRCK cycle. After exiting reset following power-up, the DAC enters initializing cycle. The analog output becomes VCOM voltage during this initializing cycle. Figure 18 shows the reset sequence by clock stop.

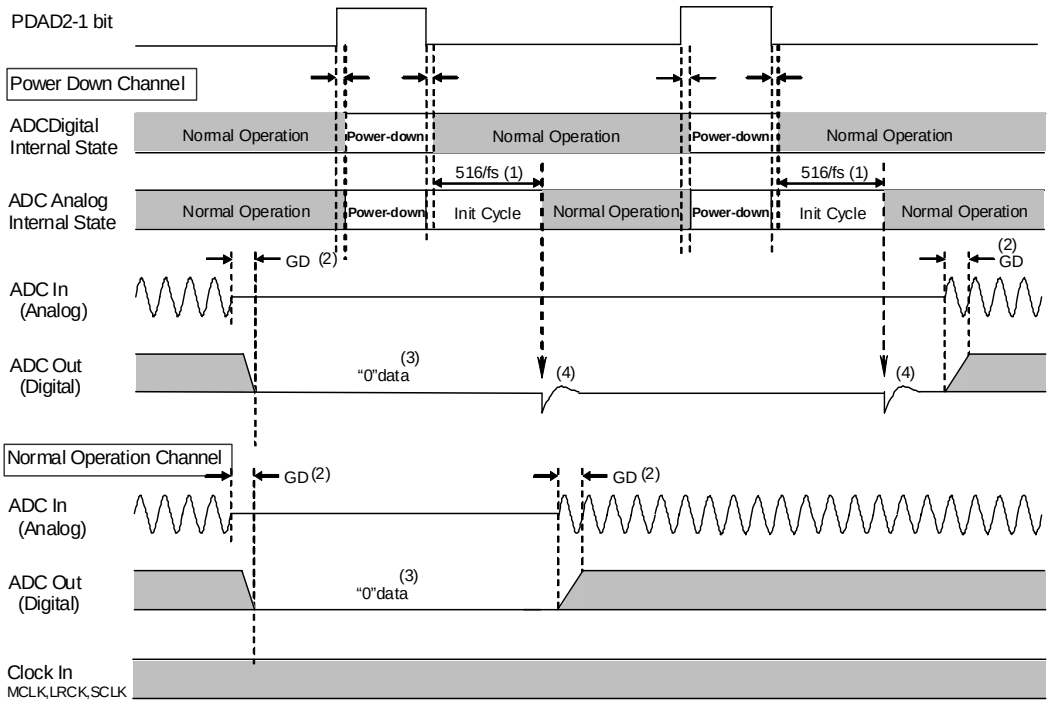


Notes:
(1) The analog section of the ADC is initialized after exiting reset state.
(2) The analog section of the DAC is initialized after exiting reset state.
(3) The Digital output corresponding to a specific analog input, and the analog ouput corresponding to a specific digital input have group delay (GD).
(4) ADC output is "0" data during reset.
(5) Click noise occurs at the end of initilizing cycle of the ADC. Mute the digital output if click noise influences systemapplications.
(6) Click noise occurs within 20usec from MCLK, LRCK or BICK stop/start.
(7) DZF1-2 pins output "L" during reset.
(8) Mute the analog output externally if click noise (6) influences system applications.

Figure 18. Reset 2 Sequence Example

■ ADC partial Power-Down Function

All of the ADCs can be powered-down individually by PDAD2-1 bits. The analog part and the digital part of the ADC are in power-down mode when the PDAD2-1 bits = "1". The analog section of ADCs are initialized after exiting the power-down state. Digital outputs corresponding to analog inputs have group delay (GD). ADC outputs "0" data in power-down state. Click noise occurs when the internal RSTN bit becomes "1". Mute the digital output externally if the click noise influences system applications. Figure 19 shows the power-down and power-up sequences by PDAD2-1 bits.



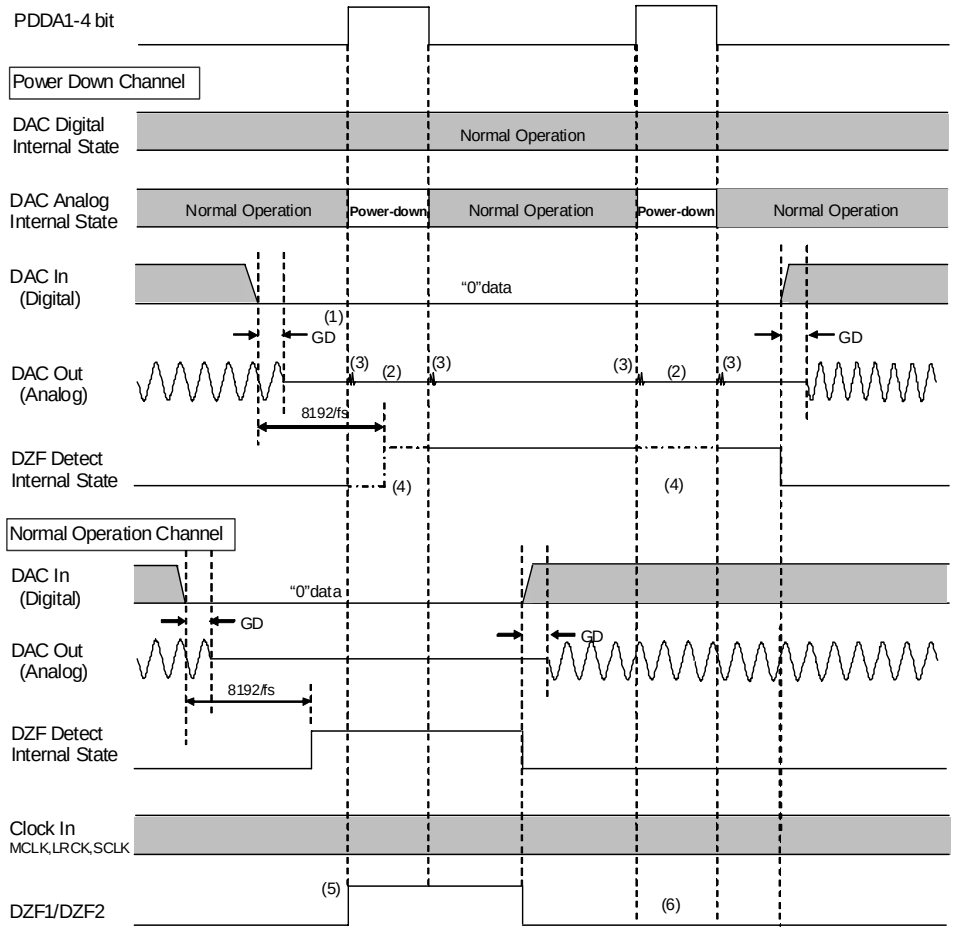
Note:

(1) The analog part of the ADC is initialized after exiting reset state.
(2) Analog outputs corresponding to the digital inputs have group delay (GD).
(3) ADC outputs "0" data in power-down state.
(4) Click noise occurs when the internal RSTN bit becomes "1". Mute the digital output externally if the click noise influences system applications.

Figure 19. ADC partial power-down example

■ DAC partial Power-Down Function

All DACs of AK4629 can be powered-down individually by PDDA1-4 bits. The analog part of DAC is in power-down mode by PDDA1-4 bits = "1", however, the digital part is not powered-down. Even if all DACs were set in power-down mode by the partial power-down bits, the digital part continues an operation. The analog output channels which are powered-down by PDDA1-4 bits are fixed to the VCOM voltage. Although DZF detection is in operation, DZF detection results of these analog output channels are not reflected to DZF1-2 pins. Some click noise occurs in both set-up and release of power-down. Mute the analog output externally or set PDDA1-4 bits when PWDAN bit = "0" or RSTN bit = "0", if click noise aversely affects system performance. Figure 20 shows the power-down/up sequences by PDDA1-4 bits.



Notes:

(1) Digital outputs corresponding to analog inputs and analog outputs corresponding to digital inputs have group delay (GD).

(2) Analog outputs of the DAC when powered down by PDDA1-4 bits = "1" are fixed to the VCOM voltage.

(3) Immediately after PDDA1-4 bits are changed, a click noise occurs at the output of the channel which is changed by the own PDDA bits.

(4) Although DZF detection is in operation, DZF detection results of powered-down DAC analog output channels are not reflected to DZF1-2 pins.

(5) DZF detection of the DAC which is in power-down mode is ignored, and DZF1-2 pins become "H".

(6) When signal is input to a DAC, even if other DACs are powered-down by partial power-down by PDDA bits, DXF1-2 pins do not become "H". Mute the analog output externally if the click noise influences system applications.

Figure 20. DAC partial power-down example

■ Serial Control Interface

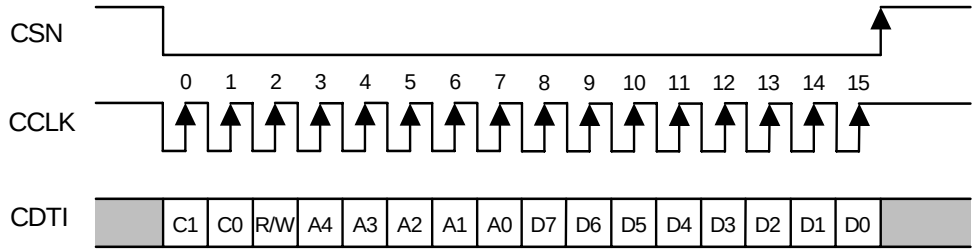
The AK4629's functions are controlled through registers. The registers may be written by two types of control modes. The chip address is determined by the state of the CAD0 and CAD1 inputs. The PDN pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit but the register data will not be initialized. When the PS pin state is changed, the AK4629 should be reset by the PDN pin.

* Writing to control register is invalid when the PDN pin = "L".

(1) 3-wire Serial Control Mode (I2C pin= "L")

Internal registers may be written through the 3 wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of Chip address (2bits, CAD0/1), Read/Write (1bit, Fixed to "1", Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max).

* The AK4629 does not support read commands in 3wire serial control mode.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: Read/Write (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 21. 3-wire Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin= "H")

The AK4629 supports the fast-mode I²C-bus (max: 400kHz).

1. WRITE Operations

Figure 22 shows the data transfer sequence in I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 28). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit which is a data direction bit (R/W) (Figure 23). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set these device address bits. If the slave address matches that of the AK4629, the AK4629 generates an acknowledge and the operation is executed. R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the address for control registers of the AK4629. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 24). Those data after the second byte contain control data. The format is MSB first, 8bits (Figure 25). The AK4629 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 28).

The AK4629 is capable of more than one byte write operation by one sequence. After receipt of the third byte, the AK4629 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 0DH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 30) except for the START and the STOP condition.

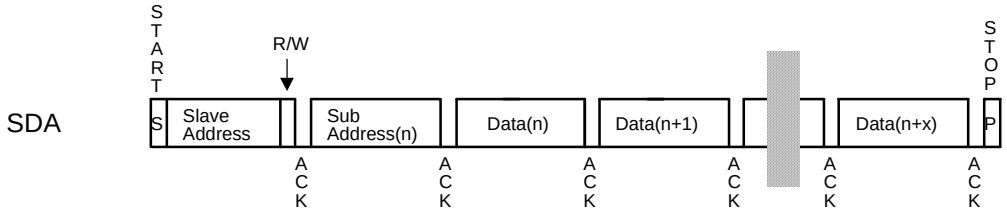


Figure 22. Data transfer sequence at the I²C-bus mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)

Figure 23. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 24. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 25. Byte structure after the second byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4629. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 16H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4629 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4629 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4629 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4629 ceases transmission.

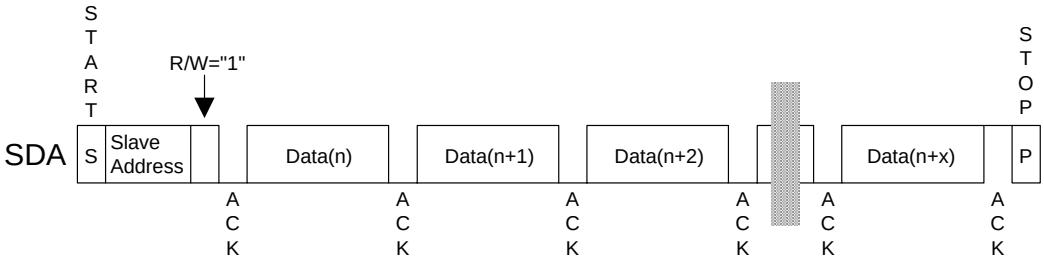


Figure 26. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK4629 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4629 ceases transmission.

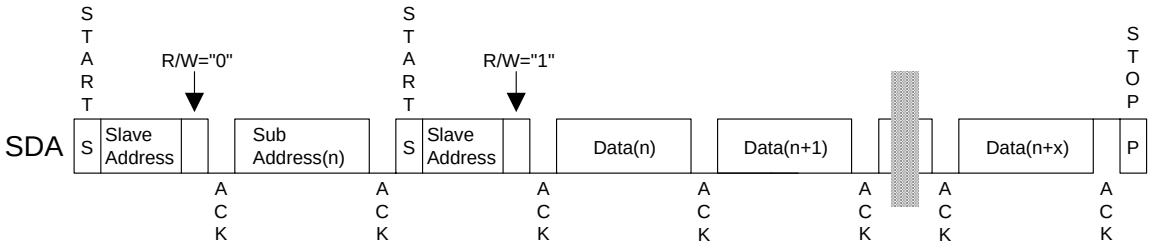


Figure 27. RANDOM ADDRESS READ

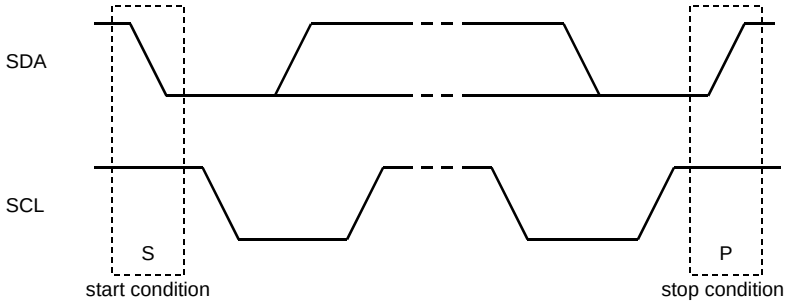


Figure 28. START and STOP conditions

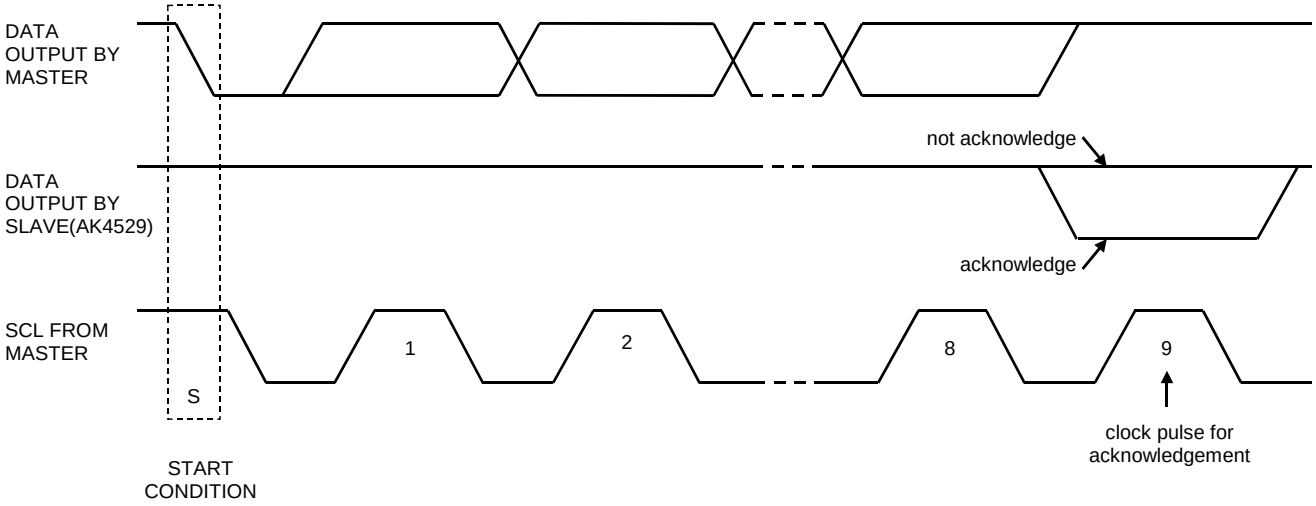


Figure 29. Acknowledge on the I^2C-bus

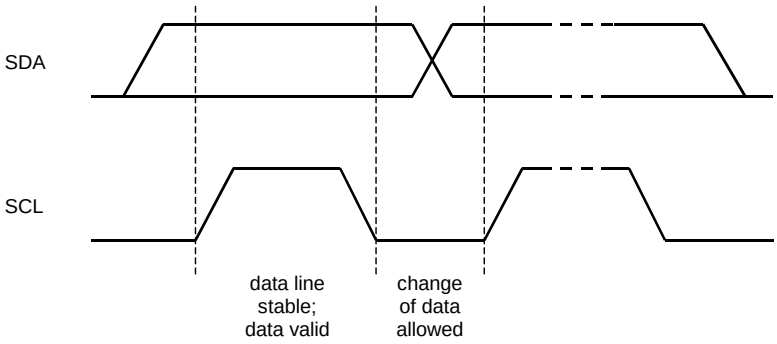


Figure 30. Bit transfer on the I^2C-bus

■ Mapping of Program Registers

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	TDM1	TDM0	DIF1	DIF0	0	SMUTE
01H	Control 2	0	DFS1	LOOP1	LOOP0	0	DFS0	ACKS	0
02H	LOUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
03H	ROUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	LOUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	De-emphasis	DEMD1	DEMD0	DEMA1	DEMA0	DEMB1	DEMB0	DEMC1	DEMC0
09H	ATT speed & Power Down Control	0	PDDA4	ATS1	ATS0	PDDA3	PDDA2	PDDA1	RSTN
0AH	Zero detect	0	DZFM3	DZFM2	DZFM1	DZFM0	PWVRN	PWADN	PWDAN
0BH	LOUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0CH	ROUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0DH	Power Down Control	0	0	0	0	0	0	PDAD2	PDAD1

Note: For addresses 0EH and 0FH, data must not be written.
When the PDN goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset and DZF1-2 pins go to “H”, but registers are not initialized to their default values.
SMUTE and DFS0 bits are ORed with pins.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	TDM1	TDM0	DIF1	DIF0	0	SMUTE
Default		0	0	0	0	1	0	0	0

SMUTE: Soft Mute Enable
0: Normal operation
1: All DAC outputs soft-muted
Register bit of SMUTE is ORed with the SMUTE pin when the PS pin= "L".

DIF1-0: Audio Data Interface Modes (Table 8, Table 9, Table 10)
Initial: "10", mode 2

TDM1-0: TDM Format Select (Table 8, Table 9, Table 10)

Mode	TDM1	TDM0	Data Output Pins	Data Input Pins	Sampling Speed
0	0	0	SDTO1-2	SDTI1-3	Normal, Double, Quad Speed
1	0	1	SDTO1	SDTI1	Normal Speed
2	1	0	-	-	N/A
3	1	1	SDTO1	SDTI1-2	Normal, Double Speed

(N/A: Not Available)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	DFS1	LOOP1	LOOP0	0	DFS0	ACKS	0
Default		0	0	0	0	0	0	0	0

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the settings of DFS bits are ignored. When this bit is "0", DFS0 and DFS1 bits set the sampling speed mode.

DFS1-0: Sampling speed mode (Table 1)
Register bit of DFS0 is ORed with DFS0 pin when the PS pin= "L".
The settings of DFS bits are ignored at ACKS bit "1".

LOOP1-0: Loopback mode enable
00: Normal (No loop back)
01: LIN1 → LOUT1, LOUT2, LOUT3, LOUT4
RIN1 → ROUT1, ROUT2, ROUT3, ROUT4
The digital ADC output is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-4 is ignored. In loopback mode, the actual audio format is forced to mode2 when the SDTO audio format setting is for mode0/1/2, and the actual audio format is forced to mode3 when the setting is for mode3. (Table 8)
10: SDTI1(L) → SDTI2(L), SDTI3(L), SDTI4(L)
SDTI1(R) → SDTI2(R), SDTI3(R), SDTI4(R)
In this mode the input DAC data to SDTI2-4 is ignored.
11: LIN2 → LOUT1, LOUT2, LOUT3, LOUT4
RIN2 → ROUT1, ROUT2, ROUT3, ROUT4
The digital ADC output is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-4 is ignored. In loopback mode, the actual audio format is forced to mode2 when the SDTO audio format setting is for mode0/1/2, and the actual audio format is forced to mode3 when the setting is for mode3. (Table 8)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	LOUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
03H	ROUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	LOUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0BH	LOUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0CH	ROUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		0	0	0	0	0	0	0	0

ATT7-0: Attenuation Level (Table 12)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	De-emphasis	DEMD1	DEMD0	DEMA1	DEMA0	DEMB1	DEMB0	DEMC1	DEMC0
Default		0	1	0	1	0	1	0	1

DEMA1-0: De-emphasis response control for DAC1 data on SDTI1 (Table 7)
Initial: “01”, OFF

DEMB1-0: De-emphasis response control for DAC2 data on SDTI2 (Table 7)
Initial: “01”, OFF

DEMC1-0: De-emphasis response control for DAC3 data on SDTI3 (Table 7)
Initial: “01”, OFF

DEMD1-0: De-emphasis response control for DAC4 data on SDTI4 (Table 7)
Initial: “01”, OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	ATT speed & Power Down Control	0	PDDA4	ATS1	ATS0	PDDA3	PDDA2	PDDA1	RSTN
Default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. DZF1-2 pins go to "H", but registers are not initialized.
1: Normal operation

ATS1-0: Digital attenuator transition time setting (Table 13)
Initial: "00", mode 0

PDDA4-1: Power-down control (0: Power-up, 1: Power-down)
PDDA1: Power down control of DAC1
PDDA2: Power down control of DAC2
PDDA3: Power down control of DAC3
PDDA4: Power down control of DAC4

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Zero detect	0	DZFM3	DZFM2	DZFM1	DZFM0	PWVRN	PWADN	PWDAN
Default		0	0	1	1	1	1	1	1

PWDAN: Power-down control of DAC1-4
0: Power-down
1: Normal operation

PWADN: Power-down control of ADC
0: Power-down
1: Normal operation

PWVRN: Power-down control of reference voltage
0: Power-down
1: Normal operation

DZFM3-0: Zero detect mode select (Table 11)
Initial: "0111", disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Power Down Control	0	0	0	0	0	0	PDAD2	PDAD1
Default		0	0	0	0	0	0	0	0

PDAD2-1: Power-down control (0: Power-up, 1: Power-down)
PDAD1: Power down control of ADC1
PDAD2: Power down control of ADC2

SYSTEM DESIGN

Figure 31 shows the system connection diagram. An evaluation board (AKD4629) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

Condition: TVDD=5V, 3-wire serial control mode, CAD1-0 = "00"

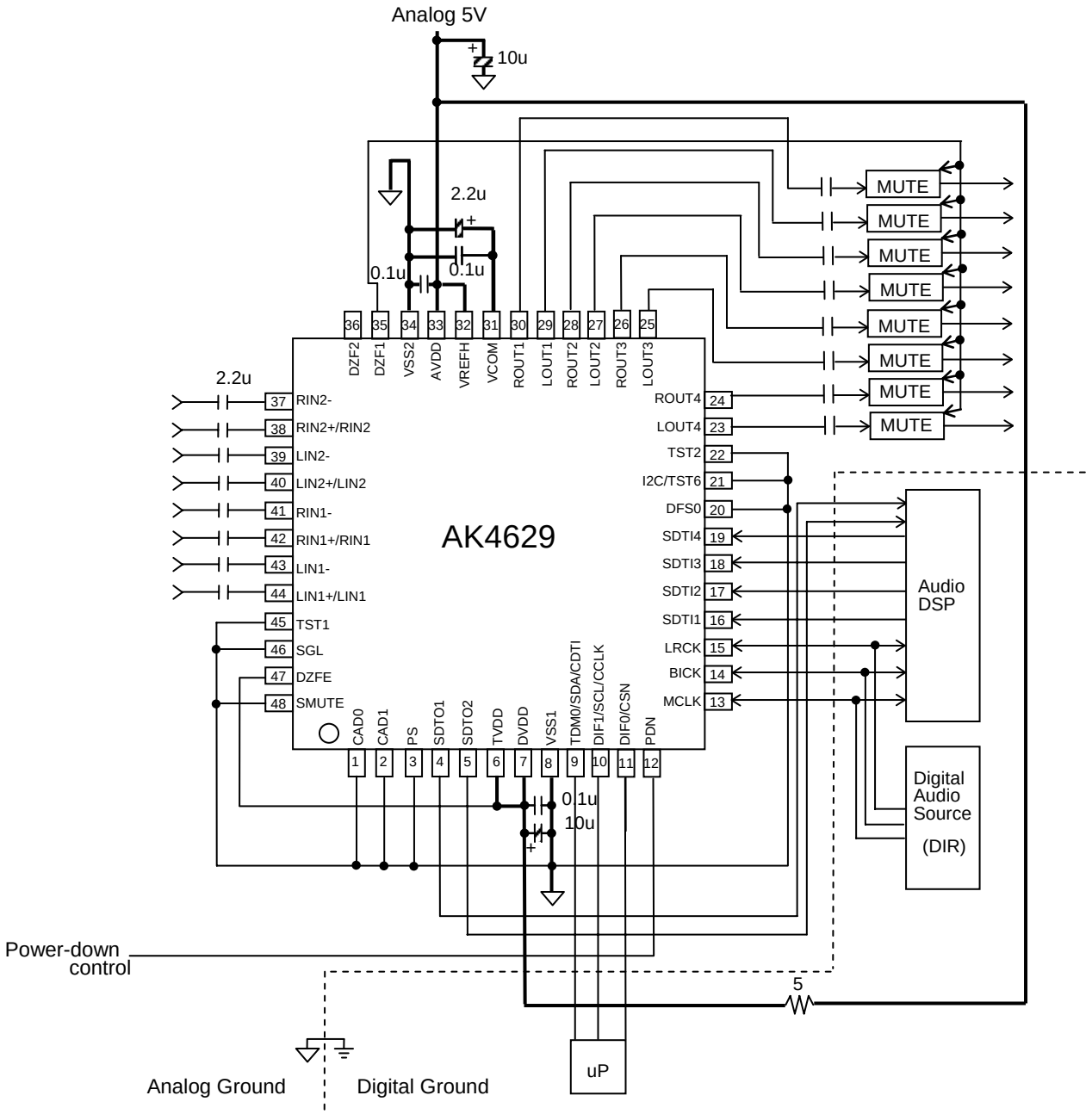


Figure 31. Typical Connection Diagram

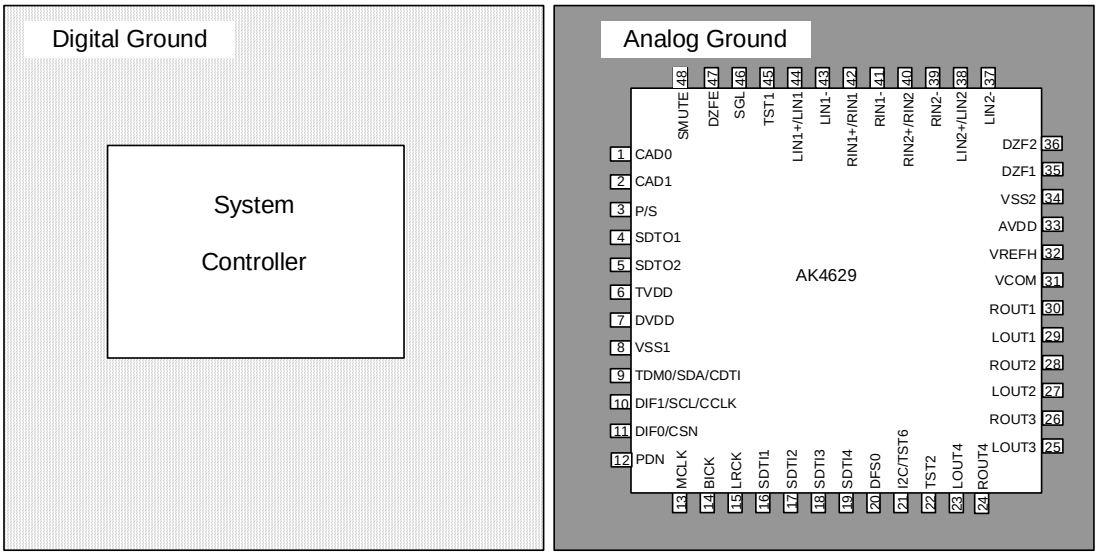


Figure 32. Ground Layout

Note: VSS1 and VSS2 must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK4629 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from analog supply in system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **VSS1 and VSS2 of the AK4629 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4629 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage of VREFH sets the analog input/output range. VREFH pin is normally connected to the AVDD pin with a 0.1μF ceramic capacitor in between the VSS2 pin. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2μF parallel with a 0.1μF ceramic capacitor attached to between the VCOM and VSS2 pins eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4629.

3. Analog Inputs

The ADC inputs correspond to single-ended and differential which able to select by the SGL pin. When the inputs are single-ended, the signal is internally biased to the common voltage (AVDD1x1/2) with 14kΩ(typ) resistance. The input signal range scales with the supply voltage and nominally 0.68xVREFH Vpp (typ) @fs=48kHz. When the inputs are differential, the signal is internally biased to the common voltage (AVDD2x1/2) with 32kΩ(typ) resistance. The input signal range between LIN(RIN)+ and LIN(RIN)– scales with the supply voltage and nominally ±0.68xVREFH Vpp (typ) @fs=48kHz .The ADC output data format is 2's complement. The internal HPF removes the DC offset.

The AK4629 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of the sampling frequency of analog inputs. The AK4629 includes an anti-aliasing filter (RC filter) to attenuate a noise around the sampling frequency of analog inputs.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

5. External Analog Inputs Circuit

Figure 33 shows the input buffer circuit example 3. The input level of this circuit is ±3.4Vpp.

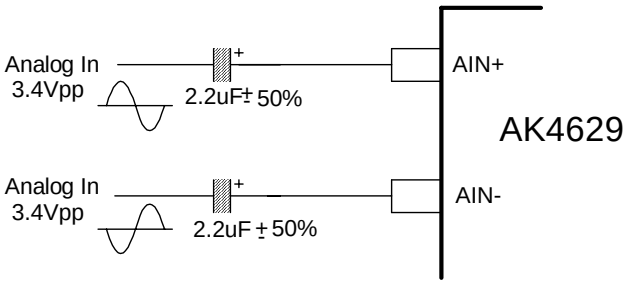


Figure 33. Input buffer circuit example 1 (AC coupled differential input)

Figure 34 shows the input buffer circuit example 3. The input level of this circuit is 3.4Vpp.

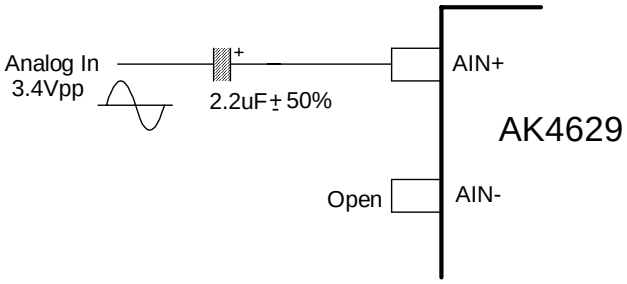


Figure 34. Input buffer circuit example 2 (AC coupled single-ended input)

6. Peripheral I/F Example

The AK4629 supports signals from external devices which are operated on 3.3V power supplies for TTL inputs. The power supply for output buffer (TVDD) should be 3.3V when those external devices are connected. Figure 35 shows an I/F example when 3.3V and 5V power supply devices are used.

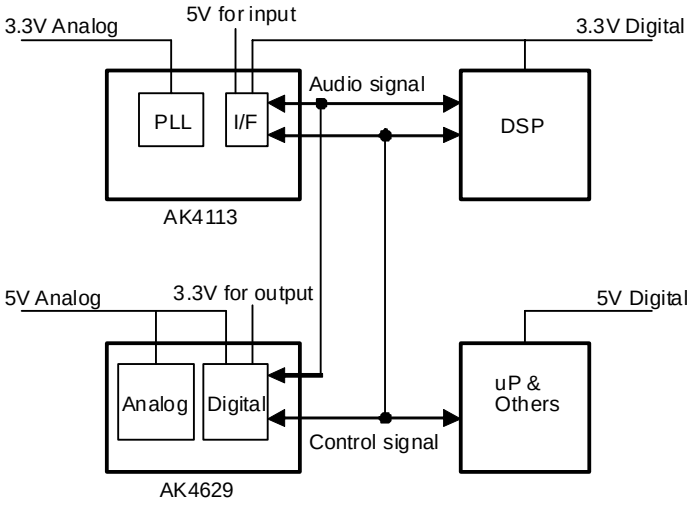
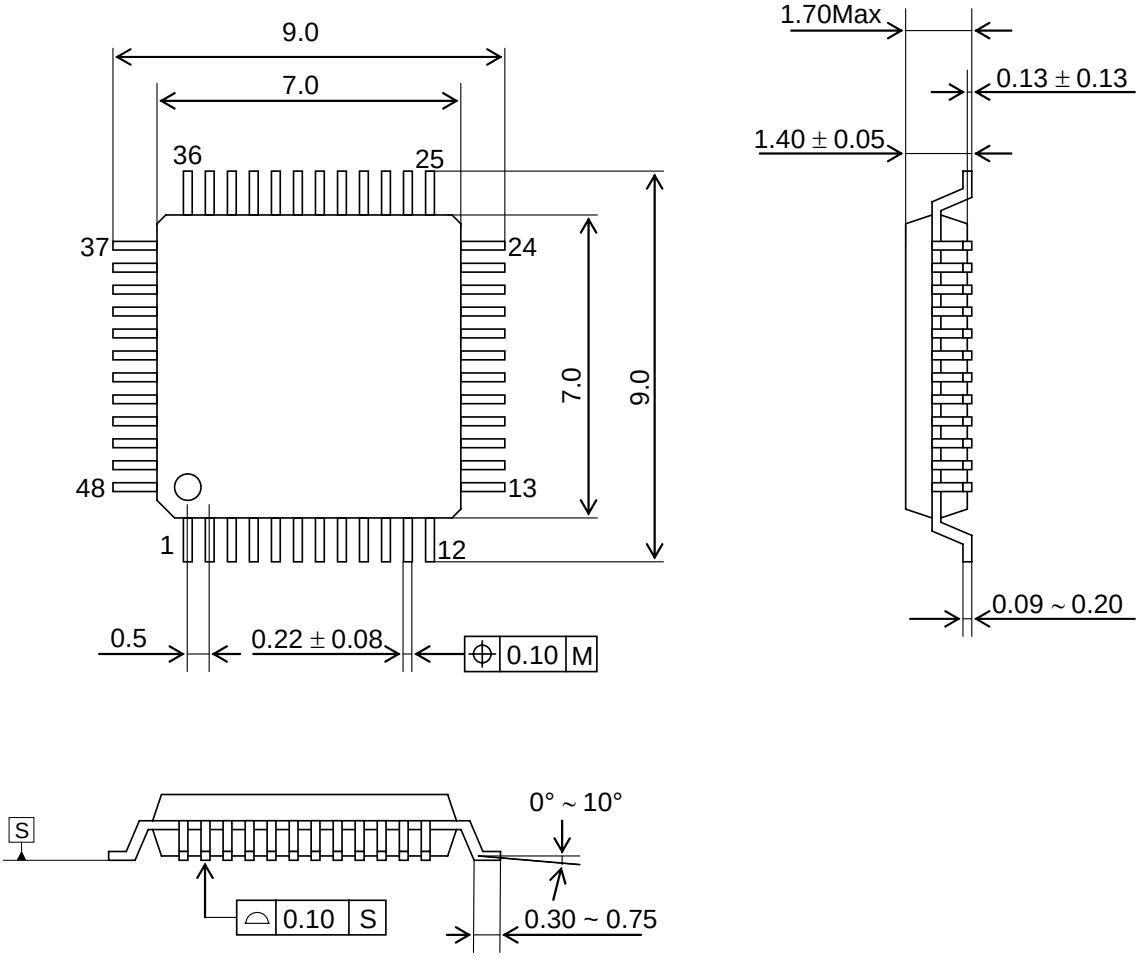


Figure 35. Power Supply Connection Example

PACKAGE

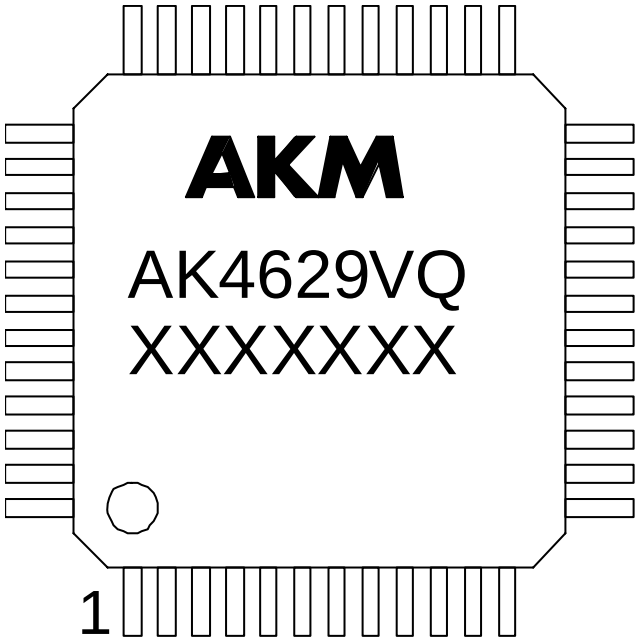
48pin LQFP(Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4629VQ
4) Asahi Kasei Logo

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
11/01/26	00	First Edition		
11/08/29	01	Specification Change	7	ANALOG CHARACTERISTICS ADC Analog Input Characteristics (Single-ended Inputs) S/(N+D), fs=48kHz: 92 → 96dB (typ) fs=96kHz: 86 → 92dB (typ) DR, fs=96kHz: 96 → 99dB (typ) fs=96kHz, A-weighted: 102 → 105dB (typ) S/N: fs=96kHz: 96 → 99dB (typ) fs=96kHz, A-wieghted: 102 → 105dB (typ) ADC Analog Input Characteristics (Differential Inputs) S/(N+D), fs=48kHz: 92 → 96dB (typ) fs=96kHz: 86 → 94dB (typ) DR, fs=96kHz: 97 → 100dB (typ) fs=96kHz, A-weighted: 103 → 106dB (typ) S/N: fs=96kHz: 97 → 100dB (typ) fs=96kHz, A-wieghted: 103 → 106dB (typ)
			8	DAC Analog Output Characteristics S/(N+D), fs=48kHz: 90 → 98dB (typ) fs=96kHz: 88 → 98dB (typ) fs=192kHz: 88 → 98dB (typ)

Date (Y/M/D)	Revision	Reason	Page	Contents
12/03/07	02	Error Correction	3	■ Ordering Guide AK4629 → AK4629VQ
			9	DC CHARACTERISTICS High-level Output Voltage Condition: SDTO1-2, LRCK, BICK pins → SDTO1-2 pins Low-level Output Voltage Condition: SDTO1-2, LRCK, BICK, DZF1, DZF2 pins → SDTO1-2, DZF1, DZF2 pins