AK4707
AV SCART Switch
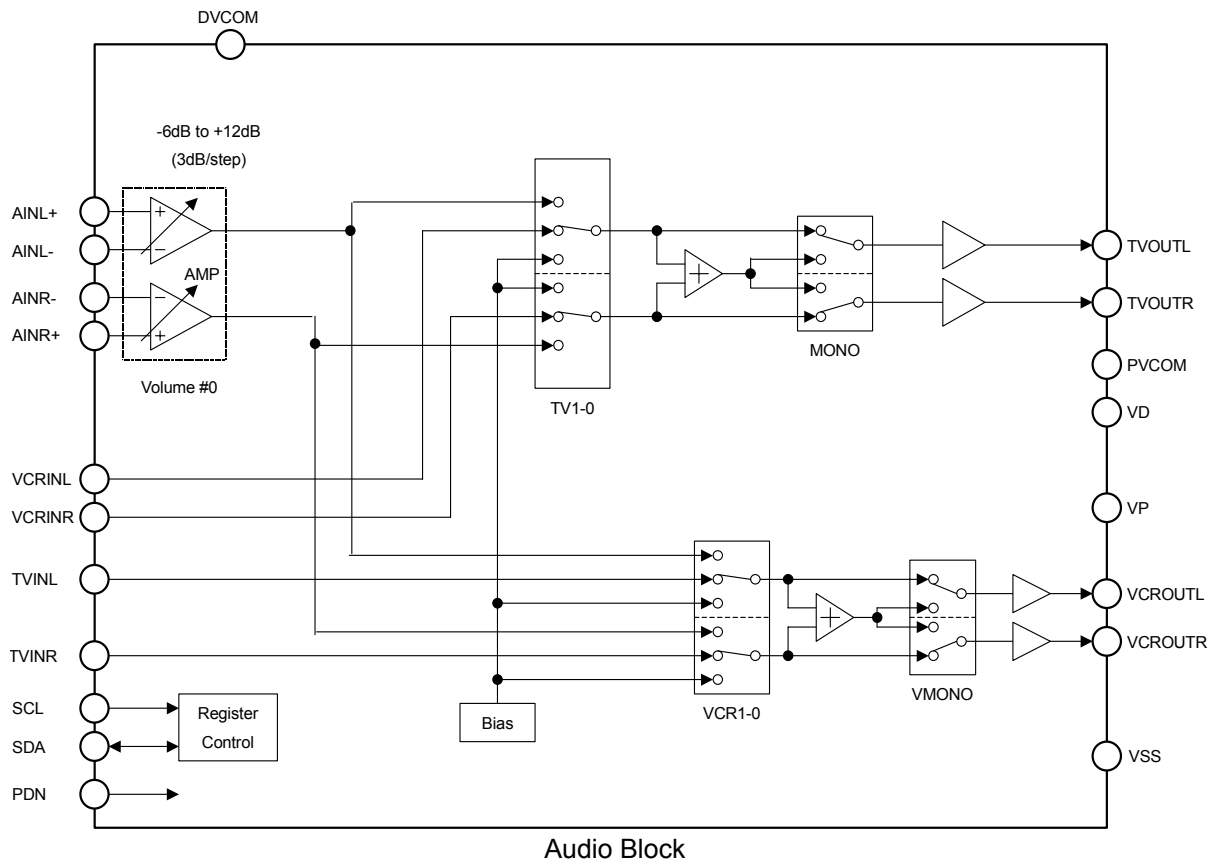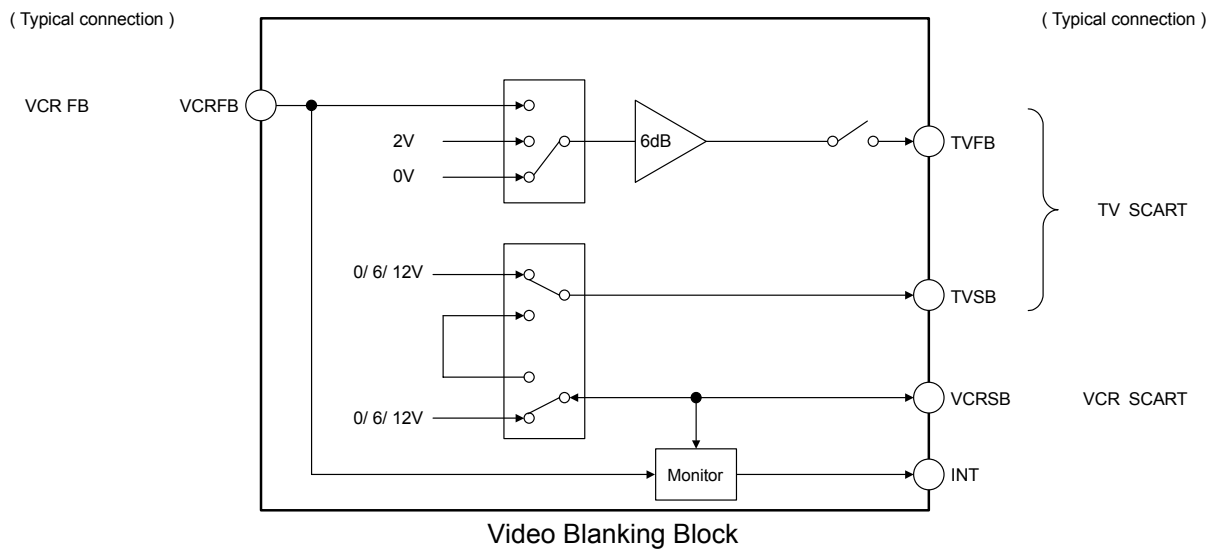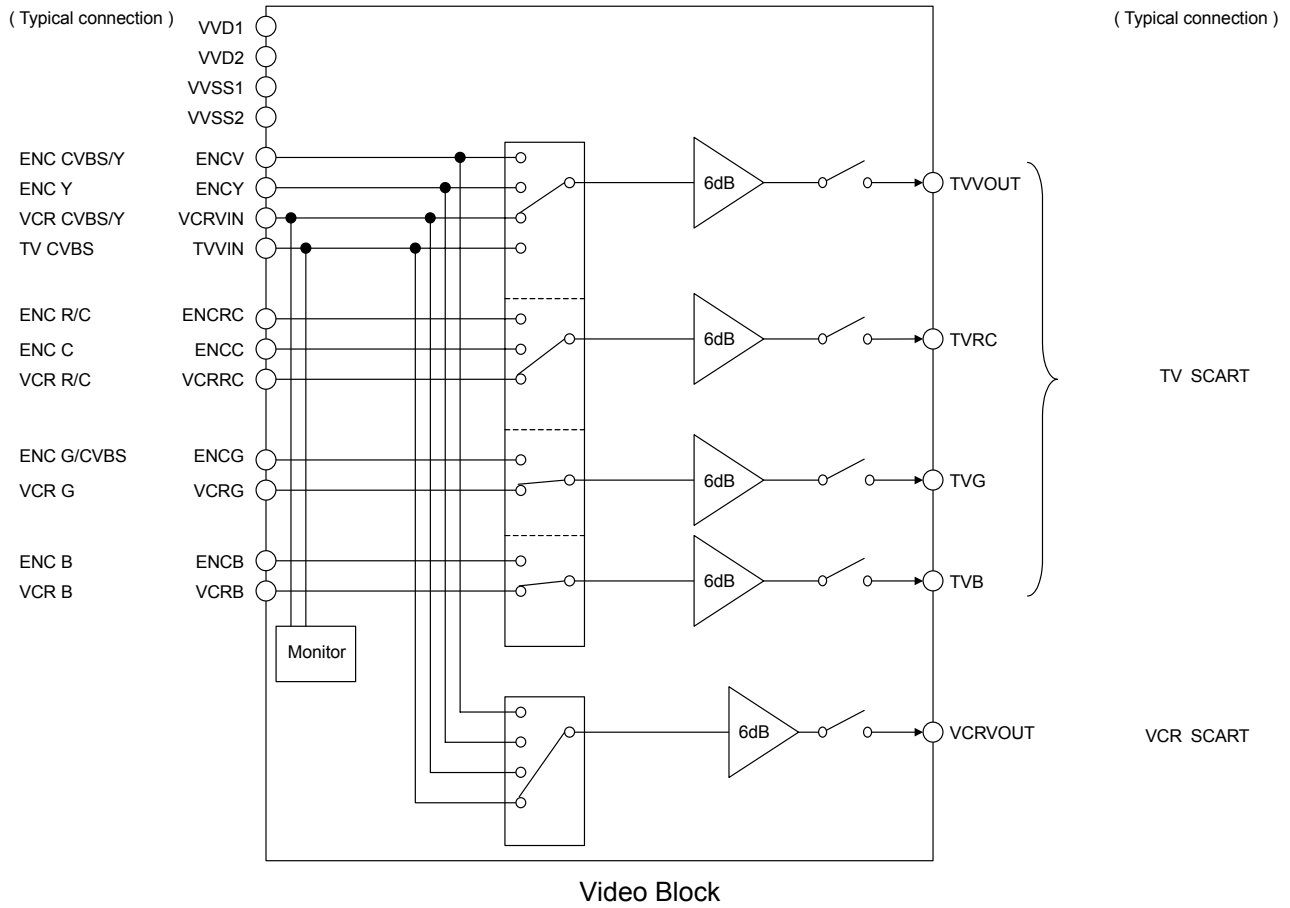
GENERAL DESCRIPTION

The AK4707 offers the ideal features for digital set-top-box systems. The AK4707 includes the audio switches, video switches, etc. designed primarily for digital set-top-box systems. The AK4707 is offered in a space saving 48-pin LQFP package.

FEATURES

☐ **Analog switches for SCART**
  Audio section
      THD+N: −86dB (@2Vrms)
      Dynamic Range: 96dB (@2Vrms)
      Analog Inputs
          Two Full Differential Stereo Input or Single-ended input for Decoder DAC
          Two Stereo Input (TV & VCR SCART)
      Analog Outputs
          Two Stereo Outputs (TV & VCR SCART)
      Pop Noise Free Circuit for Power on/off
  Video section
      75ohm driver
      6dB Gain for Outputs
      Four CVBS/Y inputs (ENCx2, TV, VCR), Two CVBS/Y outputs (TV, VCR)
      Three R/C inputs (ENCx2, VCR), One R/C output (TV)
      Two G and B inputs (ENC, VCR), One G and B outputs (TV)
      TV/VCR input monitor
  Loop-through Mode for standby
  Auto-Startup Mode for power saving
  SCART pin#16 (Fast Blanking), pin#8 (Slow Blanking) Control
☐ **Power supply**
    5V+/−5% and 12V+/−5%
    Low Power Dissipation / Low Power Standby Mode
☐ **Package**
    Small 48pin LQFP
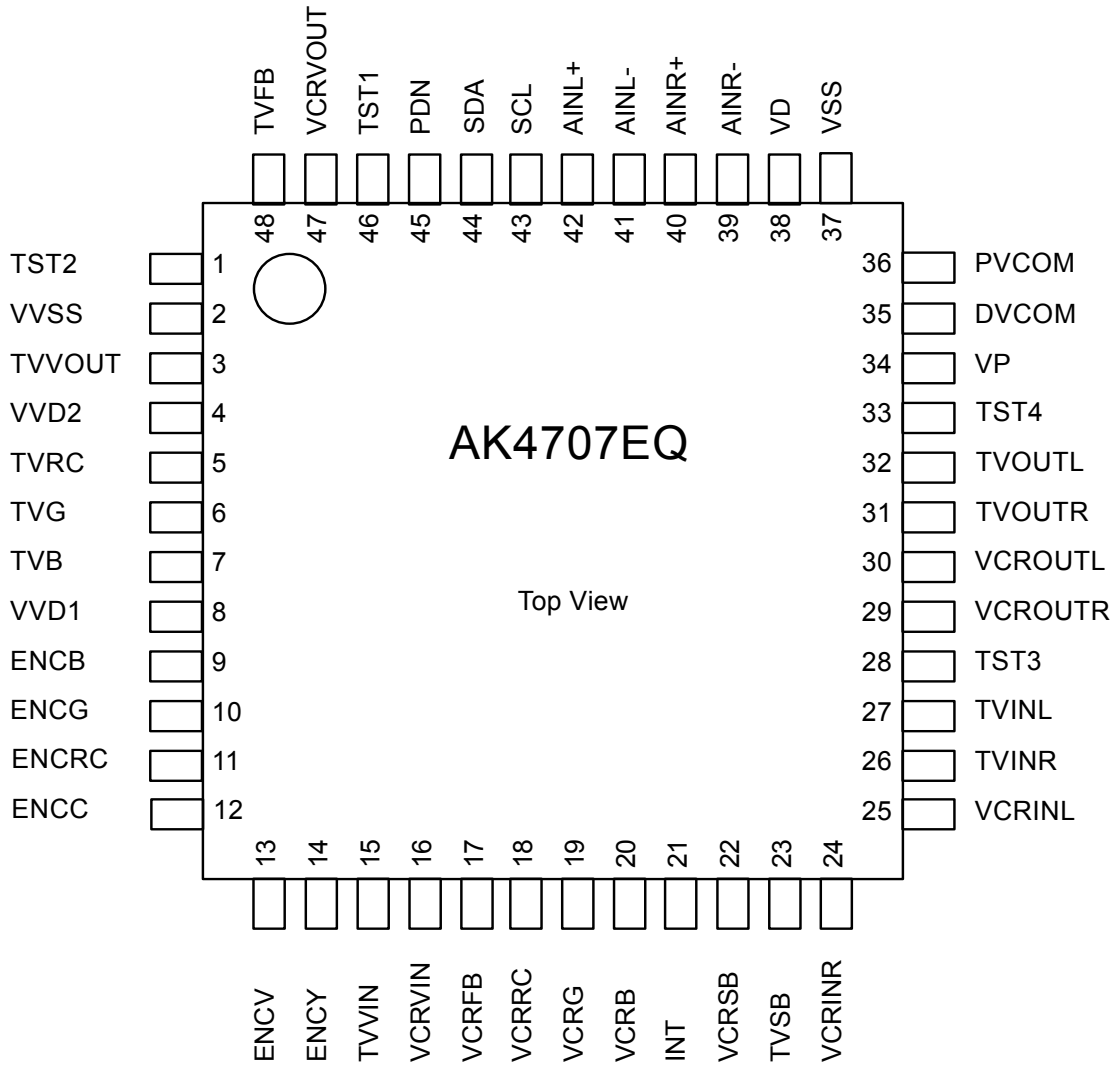☐ **AK4702 Pin Compatible**

■ Block Diagram

Audio Block

(Typical connection)   VVD1   (Typical connection)
                           VVD2
                           VVSS1
                           VVSS2

ENC CVBS/Y   ENCV
ENC Y   ENCY   6dB   TVVOUT
VCR CVBS/Y   VCRVIN
TV CVBS   TVVIN

ENC R/C   ENCRC   6dB   TVRC
ENC C   ENCC   TV SCART
VCR R/C   VCRRC

ENC G/CVBS   ENCG   6dB   TVG
VCR G   VCRG

ENC B   ENCB   6dB   TVB
VCR B   VCRB

                 Monitor

                                                    6dB   VCRVOUT   VCR SCART

Video Block

(Typical connection)   (Typical connection)

VCR FB   VCRFB
                              2V   6dB   TVFB
                              0V   TV SCART

                              0/ 6/ 12V   TVSB

                              0/ 6/ 12V   VCRSB   VCR SCART

                                            Monitor   INT

Video Blanking Block

■ **Ordering Guide**

AK4707EQ   −10 ~ +70°C   48pin LQFP (0.5mm pitch)

■ **Pin Layout**

TST2	1	36 PVCOM
VVSS	2	35 DVCOM
TVVOUT	3	34 VP
VVD2	4	33 TST4
TVRC	5	32 TVOUTL
TVG	6	31 TVOUTR
TVB	7	30 VCROUTL
VVD1	8	29 VCROUTR
ENCB	9	28 TST3
ENCG	10	27 TVINL
ENCRC	11	26 TVINR
ENCC	12	25 VCRINL

Top pins (48–37): TVFB(48), VCRVOUT(47), TST1(46), PDN(45), SDA(44), SCL(43), AINL+(42), AINL−(41), AINR+(40), AINR−(39), VD(38), VSS(37)

Bottom pins (13–24): ENCV(13), ENCY(14), TVVIN(15), VCRVIN(16), VCRFB(17), VCRRC(18), VCRG(19), VCRB(20), INT(21), VCRSB(22), TVSB(23), VCRINR(24)

AK4707EQ

Top View

■ **Main difference between AK4702 and AK4707**

Items		AK4702	AK4707
Audio	DAC	X	-
	MONO input/ output	X	-
Video	RGB video gain control	X	-
	TV/VCR video input monitor	-	X
	VCR Slow Blanking monitor in output mode.	Enabled	Disabled
	TV/VCR CVBS input detection & Power Save Mode	-	X
	RF modulator output	X	-
	VCR Y output	X	-
	Bi-Directional Control for VCR-Red/Chroma	X	
Pinout	Pin#1	VCRC	TST2
	PIN#28	MONOIN	NC
	PIN#33	MONOOUT	NC
	Pin #39 ~ #42	I/F for DAC	AMP input
	Pin#46	RFV	TST1
Others	I^{2}C speed (max)	100kHz	400kHz
	Mask bits for INT function (09H)	-	X
	FB/SB loop back in auto mode.	-	X

-: NOT available. X: Available

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	TST2	I	Test Mode Input Pin #2 Internal Pull Down 100kΩ Normally connected to VSS.
2	VVSS	-	Video Ground Pin , 0V
3	TVVOUT	O	Composite/Luminance Output Pin for TV

4	VVD2	-	Video Power Supply Pin #2: 5V
			    Normally connected to VVSS with a 0.1µF ceramic capacitor in parallel
			        with a 10µF electrolytic cap.

5	TVRC	O	Red/Chrominance Output Pin for TV
6	TVG	O	Green Output Pin for TV
7	TVB	O	Blue Output Pin for TV

8	VVD1	-	Video Power Supply Pin #1: 5V
			    Normally connected to VVSS with a 0.1µF ceramic capacitor in parallel
			        with a 10µF electrolytic cap.

9	ENCB	I	Blue Input Pin for Encoder
10	ENCG	I	Green Input Pin for Encoder
11	ENCRC	I	Red/Chrominance Input Pin #1 for Encoder
12	ENCC	I	Chrominance Input Pin #2 for Encoder
13	ENCV	I	Composite/Luminance Input Pin #1 for Encoder
14	ENCY	I	Composite/Luminance Input Pin #2 for Encoder
15	TVVIN	I	Composite/Luminance Input Pin for TV
16	VCRVIN	I	Composite/Luminance Input Pin for VCR
17	VCRFB	I	Fast Blanking Input Pin for VCR
18	VCRRC	I	Red/Chrominance Input Pin for VCR
19	VCRG	I	Green Input Pin for VCR
20	VCRB	I	Blue Input Pin for VCR
21	INT	O	Interrupt Pin for Video Blanking
22	VCRSB	I/O	Slow Blanking Input/Output Pin for VCR
23	TVSB	O	Slow Blanking Output Pin for TV
24	VCRINR	I	Rch VCR Audio Input Pin
25	VCRINL	I	Lch VCR Audio Input Pin
26	TVINR	I	Rch TV Audio Input Pin
27	TVINL	I	Lch TV Audio Input Pin
28	TST3	-	Test Mode Input Pin #3 This pin should be connected to VSS.
29	VCROUTR	O	Rch Analog Output Pin #1
30	VCROUTL	O	Lch Analog Output Pin #1
31	TVOUTR	O	Rch Analog Output Pin #2
32	TVOUTL	O	Lch Analog Output Pin #2
33	TST4	-	Test Mode Input Pin #4 This pin should be connected to VSS.

34	VP	-	Power Supply Pin, 12V
			    Normally connected to VSS with a 0.1µF ceramic capacitor in parallel
			        with a 10µF electrolytic cap.

35	DVCOM	O	Audio Common Voltage Pin #1
			    Normally connected to VSS with a 0.1µF ceramic capacitor in parallel
			        with a 10µF electrolytic cap.

36	PVCOM	O	Audio Common Voltage Pin #2
			    Normally connected to VSS with a 0.1µF ceramic capacitor in parallel
			        with a 10µF electrolytic cap. The caps affect the settling time of audio bias
			        level.

37	VSS	-	Ground Pin , 0V

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function

38	VD	-	Power Supply Pin, 5V
			    Normally connected to VSS with a 0.1μF ceramic capacitor in parallel
			    with a 10μF electrolytic cap.

39	AINR−	I	Rch Negative Analog Input Pin
40	AINR+	I	Rch Positive Analog Input Pin
41	AINL−	I	Lch Negative Analog Input Pin
42	AINL+	I	Lch Positive Analog Input Pin
43	SCL	I	Control Data Clock Pin
44	SDA	I/O	Control Data Pin

45	PDN	I	Power-Down Mode Pin
			    When at "L", the AK4707 is in the power-down mode and is held in reset.
			    The AK4707 should always be reset upon power-up.

46	TST1	I	Test Mode Input Pin #1 Internal Pull Down 100kΩ Normally connected to VSS
47	VCRVOUT	O	Composite/Luminance Output Pin for VCR
48	TVFB	O	Fast Blanking Output Pin for TV

Note: All digital input pins should not be left floating.

INTERNAL EQUIVALENT CIRCUIT

Pin No.	Pin Name	Type	Equivalent Circuit	Description
43 45	SCL PDN	Digital IN	VD 200 VSS	
39 40 41 42	AINR- AINR+ AINL− AINL+	Audio IN	VD 150K VSS	
44	SDA	Digital I/O	VD 200 VSS	I2C Bus voltage must not exceed VD.
21	INT	Digital OUT	VVD1 VSS	Normally connected to VD(5V) through 10kΩ resister externally.
3 5 6 7 47 48	TVVOUT TVRC TVG TVB VCRVOUT TVFB	Video OUT	VVD2 VVD2 VVSS VVSS	

Pin No.	Pin Name	Type	Equivalent Circuit	Description
9 10 11 12 13 14 15 16 17 18 19 20	ENCB ENCG ENCRC ENCC ENCV ENCY TVVIN VCRVIN VCRFB VCRRC VCRG VCRB	Video IN	VVD1 / 200 / VVSS	
22 23	VCRSB TVSB	Video SB	VP VP / 200 / (120k) / VVSS VVSS VVSS	The 120kΩ is not attached for TVSB.
24 25 26 27	VCRINR VCRINL TVINR TVINL	Audio IN	VP / 150k / VSS	
29 30 31 32	VCROUTR VCROUTL TVOUTR TVOUTL	Audio OUT	VP VP / 100 / VSS VSS	
35 36	DVCOM PVCOM	VCOM OUT	VD VD VD / 100 / VSS VSS VSS	

ABSOLUTE MAXIMUM RATINGS

(VSS =VVSS = 0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply (Note 2)	VD	−0.3	6.0	V
	VVD1	−0.3	6.0	V
	VVD2	−0.3	6.0	V
	VP	−0.3	14	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	−0.3	VD+0.3	V
Video Input Voltage	VINV	−0.3	VVD1+0.3	V
Audio Input Voltage (VCRINR/L, TVINR/L pins)	VINA1	−0.3	VP+0.3	V
Audio Input Voltage (AINL+/−, AINR+/− pins)	VINA2	−0.3	VD+0.3	V
Ambient Operating Temperature	Ta	−10	70	°C
Storage Temperature	Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS and VVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
           Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS = VVSS = 0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	(Note 3)	VD	4.75	5.0	5.25	V
		VVD1	4.75	5.0	5.25	V
		VVD2	4.75	5.0	VVD1	V
		VP	11.4	12	12.6	V

Note 1. All voltages with respect to ground.
Note 3. VVD1 and VVD2 must be connected to the same voltage.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VP = 12V, VD = 5V; VVD1 = VVD2 = 5V)

Power Supplies		min	typ	max	Units
Power Supply Current					
Normal Operation (PDN = "H")	(Note 4)				
VD			10	20	mA
VVD1+VVD2			20	40	mA
VP			5	10	mA
Power-Down Mode (PDN = "L")	(Note 5)				
VD			10	100	μA
VVD1+VVD2			10	100	μA
VP			10	100	μA

Note 4. STBY bit = "0", All video outputs active. No signal, no load for A/V switches.
Note 5. All digital inputs are held at VSS.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VD = 4.75 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.0	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
Low-Level Output Voltage (SDA pin: Iout= 3mA, INT pin: Iout= 1mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

ANALOG CHARACTERISTICS (AUDIO)

(Ta = 25°C; VP = 12V, VD = 5V; VVD1 = VVD2 = 5V; Signal Frequency = 1kHz;

Measurement frequency = 20Hz ~ 20kHz; $R_L \geq$ 4.5kΩ; 0dB=2Vrms output; unless otherwise specified)

Parameter	min	typ	max	Units
Analog Input: (TVINL/TVINR/VCRINL/VCRINR pins)				
Analog Input Characteristics				
Input Voltage			2.0	Vrms
Input Resistance	100	150	-	kΩ
Analog Input: (AINL+/AINL-/AINR-/AINR+ pins)				
Analog Input Characteristics				
Input Voltage			1.0	Vrms
Input Resistance	100	150	-	kΩ
Stereo/Mono Output: (TVOUTL/TVOUTR/VCROUTL/VCROUTR pins) (Note 6)				
Analog Output Characteristics				
Volume#0 Step Width	2.3	3.0	3.7	dB
THD+N (at 2Vrms output) (Note 7)		-86	-80	dB
Dynamic Range ($-$60dB Output, A-weighted) (Note 7)	92	96		dB
S/N (A-weighted) (Note 7)	92	96		dB
Interchannel Isolation (Note 7,Note 8)	80	90		dB
Interchannel Gain Mismatch (Note 7,Note 8)	-	0.3	-	dB
Gain Drift	-	200	-	ppm/°C
Load Resistance (AC-Lord, Note 10) TVOUTL/R, VCROUTL/R	4.5			kΩ
Load Capacitance TVOUTL/R, VCROUTL/R			20	pF
Output Voltage	1.85	2	2.15	Vrms
Frequency Response 0 ~ 20.0kHz		$\pm$ 0.5		dB
Power Supply Rejection (PSR) (Note 9)	-	50		dB

Note 6. Measured by Audio Precision System Two Cascade.

Note 7. Analog In to TVOUT. Path : AINL+/$-$ $\rightarrow$ TVOUTL, AINR+/$-$ $\rightarrow$ TVOUTR

Note 8. Between TVOUTL and TVOUTR with analog inputs AINL+/-, AINR+/-, 1kHz/0dB.

Note 9. The PSR is applied to VD with 1kHz, 100mV.

Note 10. THD+N: -80dB(min. at 2Vrns)

ANALOG CHARACTERISTICS (VIDEO)					
(Ta = 25°C; VP = 12V, VD= 5V; VVD1 = VVD2 = 5V; unless otherwise specified.)					
Parameter	**Conditions**	**min**	**typ**	**max**	**Units**
Sync Tip Clamp Voltage	at output pin.		0.7		V
Chrominance Bias Voltage	at output pin.		2.2		V
Gain	Input = 0.3Vp-p, 100kHz	5.5	6	6.5	dB
Interchannel Gain Mismatch	TVRC, TVG, TVB. Input = 0.3Vp-p, 100kHz.	-0.5	-	0.5	dB
Frequency Response	Input=0.3Vp-p, 100kHz to 6MHz	-1.0		1.0	dB
Input Impedance	Chrominance input (internally biased)	40	60	-	kΩ
Input Signal	f = 100kHz, maximum with distortion < 1.0%	-	-	1.5	Vpp
Load Resistance	(Note 11)	150	-	-	Ω
Load Capacitance	C1 (Note 11) C2 (Note 11)			400 15	pF pF
Dynamic Output Signal	f = 100kHz, maximum with distortion < 1.0%	-	-	3	Vpp
Y/C Crosstalk	f = 4.43MHz, 1Vp-p input. Among TVVOUT, TVRC and VCRVOUT outputs.	-	−50	-	dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW = 15kHz to 5MHz.	-	74	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	0.3	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	0.3	-	Degree

Note 11. Refer the Figure 1.
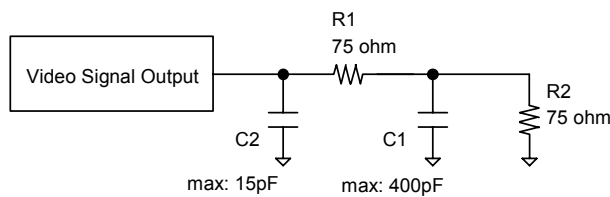
Figure 1. Load Resistance R1+R2 and Load Capacitance C1/C2.

SWITCHING CHARACTERISTICS

(Ta = 25°C; VP = 11.4 ~ 12.6V, VD = 4.75 ~ 5.25V, VVD1 = VVD2 = 4.75 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I²C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time	tHD:STA	0.6		-	μs
(prior to first clock pulse)					
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note 12)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise	tSP	0		50	ns
Suppressed by Input Filter					
Capacitive load on bus	Cb			400	pF
Reset Timing					
PDN Pulse Width (Note 13)	tPD	150			ns

Note 12. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 13. The AK4707 should be reset by PDN pin = "L" upon power up.
Note 14. I²C is a registered trademark of Philips Semiconductors.

■ **Timing Diagram**
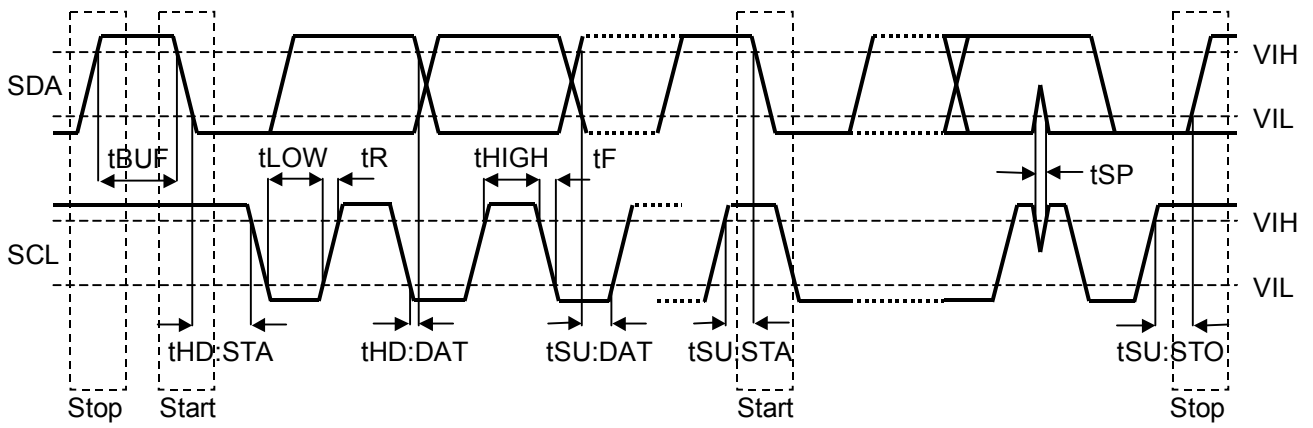
I^{2}C Bus mode Timing
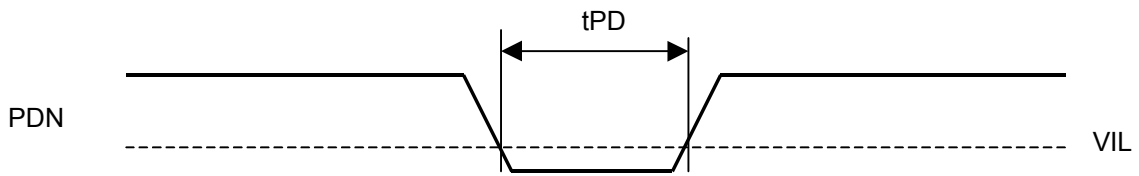
Power-down Timing

OPERATION OVERVIEW

1. System Reset and Power-down options

The AK4707 should be reset once by bringing PDN pin = "L" upon power-up. The AK4707 has several operation modes. The PDN pin, AUTO bit, BIAS bit, STBY bit and AMP bit control operation modes as shown in Table 1 and Table 2.

Mode	PDN pin	AUTO bit	STBY bit	BIAS bit	Mode
0	"L"	*	*	*	Full Power-down
1	"H"	1	*	*	Auto Startup mode (Power-on default)
2	"H"	0	1	1	Standby & Mute
3	"H"	0	1	0	Standby
4	"H"	0	0	1	Mute (AMP power down)
5	"H"	0	0	0	Normal operation (AMP operation)

Table 1. Operation Mode Settings (*: Don't Care)

Mode			Register Control	Audio Bias Level	Video Output	TVFB, TVSB	VCRSB
0	Full Power-down		Not available	Power down	Hi-Z	Hi-Z	Pull-down (1)
1	Auto Startup mode (Power-on default)	No video input	Available				
		Video input (2)		Active	Active	Active	Active
2	Standby & Mute			Power down	Hi-Z / Active		
3	Standby			Active			
4	Mute (AMP power down)			Power down			
5	Normal operation (AMP operation)			Active (3)			

Note 15. Internally pulled down by 120kΩ (typ) resistor.
Note 16. Video input to TVVIN or VCRVIN.
Note 17. TVOUTL/R are muted by Mute bit in the default state.

Table 2. Status of each operation modes

■ Full Power-down Mode

The AK4707 should be reset once by bringing PDN pin = "L" upon power-up.

>   PDN pin: Power down pin
>   L: Device power down.
>   H: Normal operation.

■ Auto Startup Mode

After when the PDN pin is set to "H", the AK4707 is in the auto startup mode. In this mode, all blocks except for the video detection circuit are powered down. Once the video detection circuit detects video signal from TVVIN pin or VCRVIN pin, the AK4707 goes to the stand-by mode automatically and sends "H" pulse via INT pin. The sources of TVOUTL/R are fixed to VCRINL/R, the sources of VCROUTL/R are fixed to TVINL/R respectively. The source of DC- restore circuit is VCRVIN pin. To exit the auto startup mode, set the AUTO bit to "0".

>   AUTO bit (00H D3): Auto startup bit
>   0: Auto startup disable. (Manual startup)
>   1: Auto startup enable. (default)

■ Bias Mode

When the BIAS bit = "1", the bias voltage on the audio output goes to GND level. Bringing BIAS bit to "0" changes this bias voltage smoothly from GND to VP/2 by 2sec (typ.). This removes the huge click noise related the sudden change of bias voltage at power-on. The change of BIAS bit from "1" to "0" also makes smooth transient from VP/2 to GND by 2sec (typ). This removes the huge click noise related the sudden change of bias voltage at power-off.

>   BIAS bit (00H D1): Bias-off bit
>   0: Normal operation.
>   1: Set the audio bias to GND. (default)

■ Standby Mode

When the AUTO bit = BIAS bit = "0" and the STBY bit = "1", the AK4707 is forced into TV-VCR loop through mode. In this mode, the sources of TVOUTL/R pins are fixed to VCRINL/R pins; the sources of VCROUTL/R are fixed to TVINL/R pins respectively. All register values themselves are NOT changed by STBY bit = "1".

>   STBY bit (00H D0): Standby bit
>   0: Normal operation.
>   1: Standby mode. (default)

■ Normal Operation Mode

To change analog switches, set the AUTO bit, BIAS bit and STBY bit to "0". The AK4707 is in power-down mode until PDN pin = "H". The Figure 2 shows an example of the system timing at the power-down and power-up by PDN pin.

■ Typical Operation Sequence (auto setup mode)

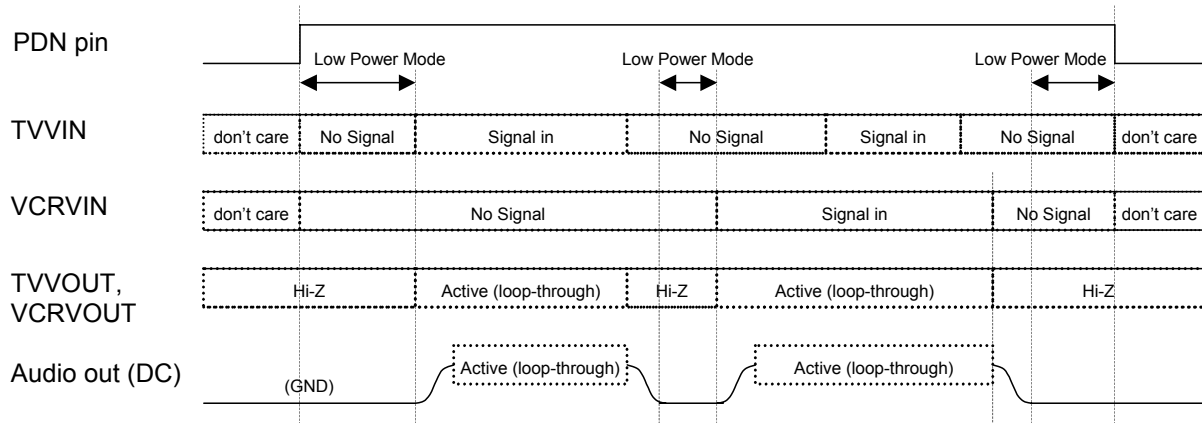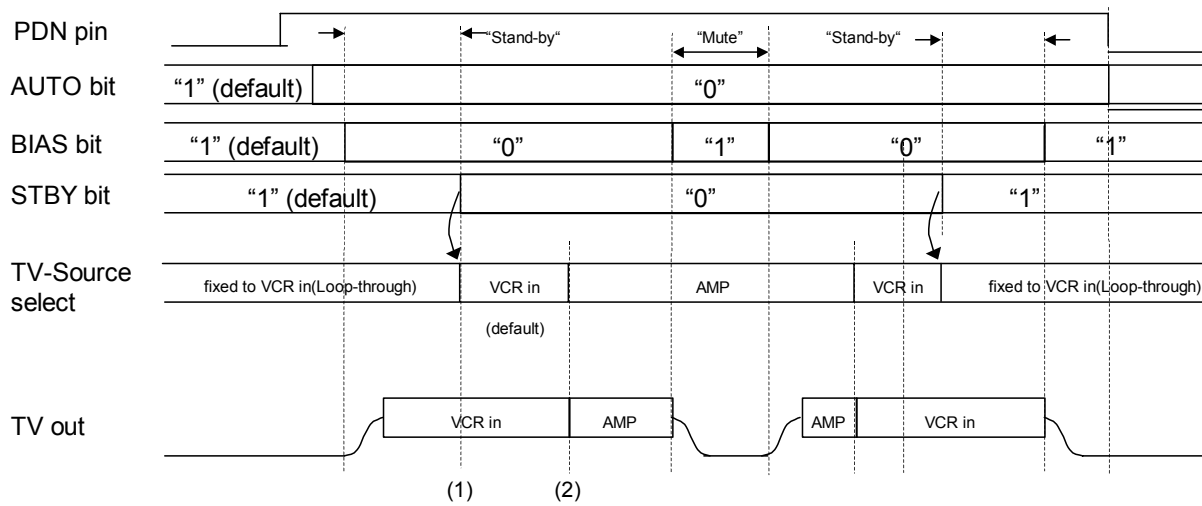Figure 2 shows an example of the system timing at auto setup mode.

Figure 2. Typical operating sequence (auto setup mode)

■ Typical Operation Sequence (except auto setup mode)

Figure 3 shows an example of the system timing at auto setup mode.

Notes:
   (1) Set the STBY bit = "0" to pass for 20.2ms after set the MUTE bit = "0", to prevent the click noise (1).
   (2) Mute the analog outputs externally if click noise (2) affects the system.

Figure 3. Typical operating sequence (except auto setup mode)

2. Audio Block

■ Switch Control

The AK4707 has switch matrixes designed primarily for SCART routing. Those are controlled via the control register as shown in, Table 3 and Table 4 (Please refer to the Block Diagram).

(01H: D1-D0)

TV1	TV0	Source of TVOUTL/R
0	0	AMP
0	1	VCRIN (default)
1	0	Mute
1	1	(Reserved)

Table 3. TVOUT Switch Configuration

(01H: D5-D4)

VCR1	VCR0	Source of VCROUTL/R
0	0	AMP
0	1	TVIN (default)
1	0	Mute
1	1	(Reserved)

Table 4. VCROUT Switch Configuration

■ Volume Control #0 (7-Level Volume)

The AK4707 has a 7-level volume control (Volume #0) as shown in Table 5. The volume reflects the change of register value immediately.
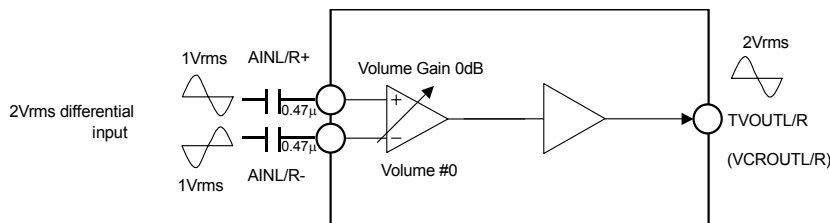
Figure 4. Volume #0(Volume Gain=0dB:default), Full Differential Stereo Input

(02H: D5-D3)

L2	L1	L0	Volume #0 Gain	Output Level (Typ)
1	1	1	+12dB	2Vrms (with 0.5Vrms differential input)
1	1	0	+9dB	-
1	0	1	+6dB	2Vrms (with 1Vrms differential input)
1	0	0	+3dB	-
0	1	1	0dB	2Vrms (with 2Vrms differential input: default)
0	1	0	-3dB	-
0	0	1	-6dB	1Vrms (with 2Vrms differential input)
0	0	0	Mute	-

Table 5. Volume #0, Full Differential Stereo Input
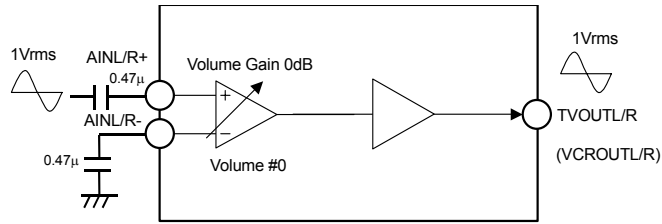
Figure 5. Volume #0(Volume Gain=0dB:default), Single-ended Input

(02H: D5-D3)

VOL2	VOL1	VOL0	Volume #0 Gain	Output Level (Typ)
1	1	1	+12dB	2Vrms (with 0.5Vrms input)
1	1	0	+9dB	-
1	0	1	+6dB	2Vrms (with 1Vrms input)
1	0	0	+3dB	-
0	1	1	0dB	1Vrms (with 1Vrms input: default)
0	1	0	-3dB	-
0	0	1	-6dB	0.5Vrms (with 1Vrms input)
0	0	0	Mute	-

Table 6. Volume #0, Single-ended Input

■ **MUTE Control**

To minimize the click noise at setting the MUTE bit = "1", the AK4707 has a zero-cross detection. When the ZERO bit = "1", the zero-cross detection function is enabled. TVOUTL/R outputs analog common voltage at the input signal first zero-cross point from setting the MUTE bit = "1" or when the zero-cross is not detected within the time set by ZTM1-0 bits (12.8msec to 102.4msec). TVOUTL/R outputs of TV1-0 switch at the input signal first zero-cross point from setting the MUTE bit = "0" or when the zero-cross is not detected within the time set by ZTM1-0 bits. The zero-cross is detected on L/R channels at the TV1/0 selector independently. To disable this function, set the ZERO bit to "0".

    ZERO: Zero-cross detection enable for TV1/0 selector
      0: Disable
      1: Enable (default)

3. Video Block

■ Video Switch Control

The AK4707 has switches for TV and VCR. Each switch can be controlled via registers independently. When AUTO bit = "1" or STBY bit = "1", these switches setting is ignored and set to fixed configuration (loop-through mode). Refer the auto setup mode and standby mode.

(04H: D2-D0)

Mode	VTV2-0 bit	Source of TVVOUT pin	Source of TVRC pin	Source of TVG pin	Source of TVB pin
Shutdown	000	(Hi-Z)	(Hi-Z)	(Hi-Z)	(Hi-Z)
Encoder CVBS /RGB	001	ENCV pin (Encoder CVBS)	ENCRC pin (Encoder Red,C)	ENCG pin (Encoder Green)	ENCB pin (Encoder Blue)
Encoder Y/C 1	010	ENCV pin (Encoder Y)	ENCRC pin (Encoder C)	Hi-Z	(Hi-Z)
Encoder Y/C 2	011	ENCY pin (Encoder Y)	ENCC pin (Encoder C)	Hi-Z	(Hi-Z)
VCR (default)	100	VCRVIN pin (VCR CVBS)	VCRRC (VCR Red,C)	VCRG pin (VCR Green)	VCRB pin (VCR Blue)
TV CVBS	101	TVVIN pin (TV CVBS)	(Hi-Z)	(Hi-Z)	(Hi-Z)
(Reserved)	110	-	-	-	-
(Reserved)	111	-	-	-	-

Table 7. TV video output (Refer Note 18.)

(04H: D5-D3)

Mode	VVCR2-0 bit	Source of VCRVOUT pin
Shutdown	000	(Hi-Z)
Encoder CVBS or Y/C 1	001	ENCV pin (Encoder CVBS)
Encoder CVBS or Y/C 2	010	ENCY pin (Encoder CVBS)
TV CVBS (default)	011	TVVIN pin (TV CVBS)
VCR	100	VCRVIN pin (VCR CVBS)
(Reserved)	101	-
(Reserved)	110	-
(Reserved)	111	-

Table 8. VCR video output (Refer Note 18.)

Note 18. When input the video signal via ENCRC pin or VCRRC pin, set CLAMP1-0 bits respectively.

■ **Video Output Control (05H: D6-D0)**

Each video output can be set to Hi-Z individually via control registers. These settings are ignored when the AUTO bit = "1".

> TVV: TVVOUT output control
> TVR: TVRCOUT output control
> TVG: TVGOUT output control
> TVB: TVBOUT output control
> VCRV: VCRVOUT output control
> TVFB: TVFB output control
>   0: Hi-Z. (default)
>   1: Active.

■ **Clamp and DC-restore circuit control (06H: D6-D5, D3-D2)**

Each CVBS and Y input has the sync tip clamp circuit. The sync tip voltage at each output is 0.7V (typ). This corresponds 0.35V (typ) at the SCART connector when matched by 75Ω resistors. The CLAMP1-0 bits select the input circuit for ENCRC pin (Encoder Red/Chroma) and VCRRC pin (VCR Red/Chroma) respectively. VCLP1-0 bits select the source of DC-restore circuit.

> CLAMP1: Encoder Red/Chroma (ENCRC pin) input clamp control
>   0: DC restore clamp active (for RED signal. default)
>   1: Biased (for Chroma signal)
>
> CLAMP0: VCR R/C (VCRRC pin) input clamp control
>   0: DC restore clamp active (for RED signal)
>   1: Biased (for Chroma signal. default)
>
> VCLP1-0: DC restore source control
>   When the AUTO bit = "1", the source is fixed to VCRVIN.

VCLP1 bit	VCLP0 bit	Sync Source of DC Restore
0	0	ENCV (default)
0	1	ENCY
1	0	VCRVIN
1	1	(Reserved)

Table 9. DC restore source control

4. Blanking Control

The AK4707 supports Fast Blanking signals and Slow Blanking (Function Switching) signals for TV/VCR SCART.

■ Input/Output Control for Fast/Slow Blanking

FB1-0: TV Fast Blanking output control (07H: D1-D0)

FB1 bit	FB0 bit	TVFB pin Output Level
0	0	0V (default)
0	1	2V<, 4V(typ) at 150Ω load
1	0	Same as VCR FB input (4V/0V)
1	1	(Reserved)

Table 10. TV Fast Blanking output (Note: minimum load is 150Ω)

SBT1-0: TV Slow Blanking output control (07H: D3-D2)

SBT1 bit	SBT0 bit	TVSB pin Output Level
0	0	< 2V (default)
0	1	5V <, < 7V
1	0	(Reserved)
1	1	10V <

Table 11. TV Slow Blanking output (Note: minimum load is 10kΩ)

SBV1-0: VCR Slow Blanking output control (07H: D5-D4)

SBV1 bit	SBV0 bit	VCRSB pin Output Level
0	0	< 2V (default)
0	1	5V <, < 7V
1	0	(Reserved)
1	1	10V <

Table 12. VCR Slow Blanking output (Note: minimum load is 10kΩ)

SBIO1-0: TV/VCR Slow Blanking I/O control (07H: D7-D6)

SBIO1 bit	SBIO0 bit	VCRSB pin Direction	TVSB pin Direction	
0	0	Output (Controlled by SBV1-0 bits)	Output (Controlled by SBT1-0 bits)	(default)
0	1	(Reserved)	(Reserved)	
1	0	Input (Stored in SVCR1-0 bits)	Output (Controlled by SBT1-0 bits)	
1	1	Input (Stored in SVCR1-0 bits)	Output (Same output as VCR SB)	

Table 13. TV/VCR Slow Blanking I/O control

5. Monitor Options and INT function

■ Monitor Options (08H: D4-D0)

The AK4707 has several detection functions. SVCR1-0 bits, FVCR bit, VCMON bit and TVMON bit reflect the input DC level of VCR slow blanking, the input DC level of VCR fast blanking and signals input to TVVIN or VCRVIN pins.

SVCR1-0: VCR Slow blanking status monitor
SVCR1-0 bits reflect the voltage at VCRSB pin only when the VCRSB is in the input mode.
When the VCRSB is in the output mode, SVCR1-0 bits hold previous value.

VCRSB pin input level	SVCR1 bit	SVCR0 bit
< 2V	0	0
4.5V to 7V	0	1
(Reserved)	1	0
9.5V <	1	1

Table 14. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor
This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR bit
< 0.4V	0
1V <	1

Table 15. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VCMON: VCRVIN pin video input monitor (MCOMN bit = "1"),
          TVVIN pin or VCRVIN pin video input monitor (MCOMN bit = "0")
    0: No video signal detected.
    1: Detects video signal.

TVMON: TVVIN pin video input monitor (active when MCOMN bit = "1")
    0: No video signal detected.
    1: Detects video signal.

AUTO (00H D3)	MCOMN (09H D7)	TVVIN signal	VCRVIN signal	TVMON (08H D4)	VCMON (08H D3)
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	1
1	*	0	0	0	0
1	*	0	1	0	1
1	*	1	0	0	1
1	*	1	1	0	1

*:don't care,

Note 19. TVVIN/VCRVIN signal: signal 0 = No signal applied, signal 1 = signal applied
Table 16. TV/VCR Monitor Function

■ **INT Function and Mask Options (09H: D3-D1)**

Changes of the 08H status can be monitored via the INT pin. The INT pin is the open drain output and goes "L" for 2μs (typ.) when the status of 08H is changed. This pin should be connected to VD (typ. 5V) through 10kohm resistor.
MTV bit, MVC bit, MCOMN bit, MFVCR bit and MSVCR bit control the reflection of the status change of these monitors onto the INT pin from report to prevent to masks each monitor.
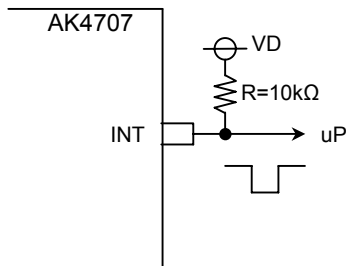

Figure 6. INT pin

MVC: VCMON Mask. Refer Table 18
MTV: TVMON Mask. Refer Table 17
MCOMN: Refer Table 16

AUTO (00H D3)	TVMON (08H D4)	MTV (09H D4)	INT
0	No Change	0	Hi-Z
0	No Change	1	Hi-Z
0	Change	0	Generates "L" Pulse
0	Change	1	Hi-Z
1	No Change	0	Hi-Z
1	No Change	1	Hi-Z

Note 20. When the STBY bit = "0", the TV Monitor Mask function is enabled.
Note 21. When AUTO bit = "1", TVMON does not change.
Table 17. TV Monitor Mask

AUTO (00H D3)	VCMON (08H D3)	MVC (09H D3)	INT
0	No Change	0	Hi-Z
0	No Change	1	Hi-Z
0	Change	0	Generates "L" Pulse
0	Change	1	Hi-Z
1	No Change	0	Hi-Z
1	No Change	1	Hi-Z
1	Change	0	Generates "L" Pulse
1	Change	1	Generates "L" Pulse

Note 22. When the STBY bit = "0", the VCR Monitor Mask function is enabled.
Table 18. VCR Monitor Mask

MFVCR: FVCR Monitor mask.
    0: Change of FVCR is reflected to INT pin. (default)
    1: Change of FVCR is NOT reflected to INT pin.

MSVCR: SVCR1-0 Monitor mask
    0: Change of SVCR1-0 is reflected to INT pin. (default)
    1: Change of SVCR1-0 is NOT reflected to INT pin.

6. Control Interface

I^{2}C-bus Control Mode

1. WRITE Operations

Figure 7 shows the data transfer sequence in I^{2}C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 13). After the START condition, a slave address is sent. This address is 7bits long followed by an eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4707, the AK4707 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 15). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4707. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 9). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 10). The AK4707 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 13).

The AK4707 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4707 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 15) except for the START and the STOP condition.
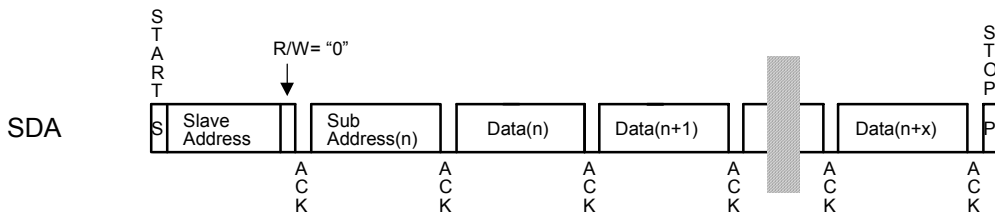

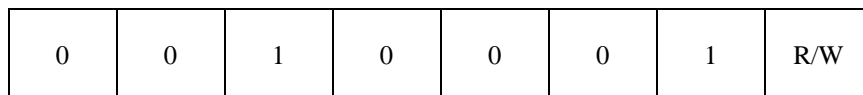Figure 7. Data transfer sequence at the I^{2}C-bus mode

0	0	1	0	0	0	1	R/W

Figure 8. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 9. The second byte

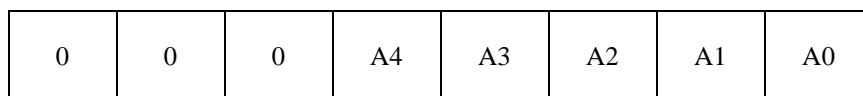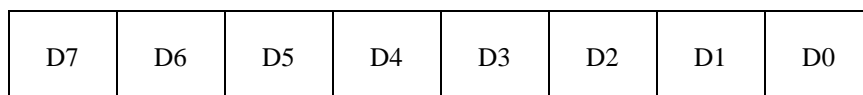| D7	D6	D5	D4	D3	D2	D1	D0

Figure 10. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4707 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4707 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4707 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4707 discontinues transmission.
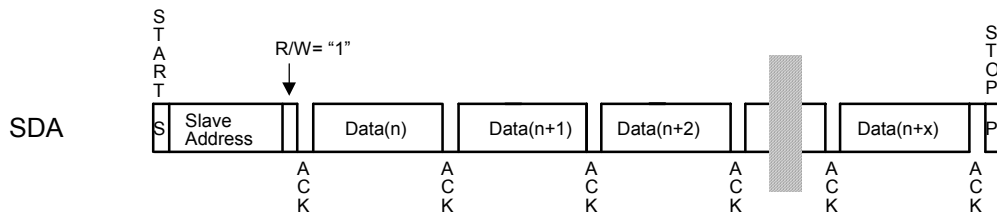

Figure 11. CURRENT ADDRESS READ

2-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address (R/W bit = "0") and then the register address to read. After the register's address is acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4707 generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4707 discontinues transmission.
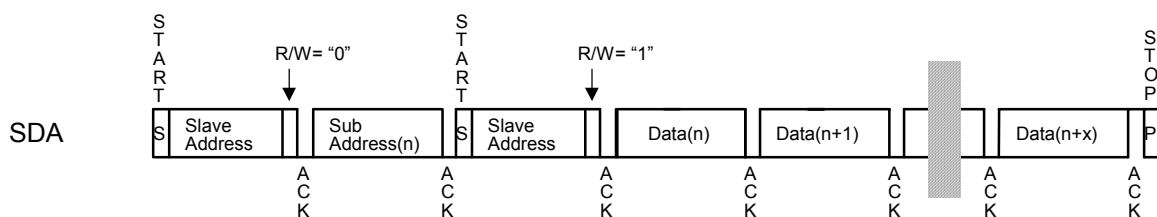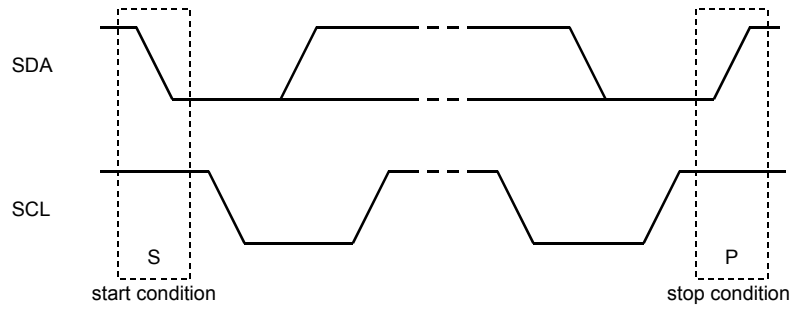

Figure 12. RANDOM ADDRESS READ
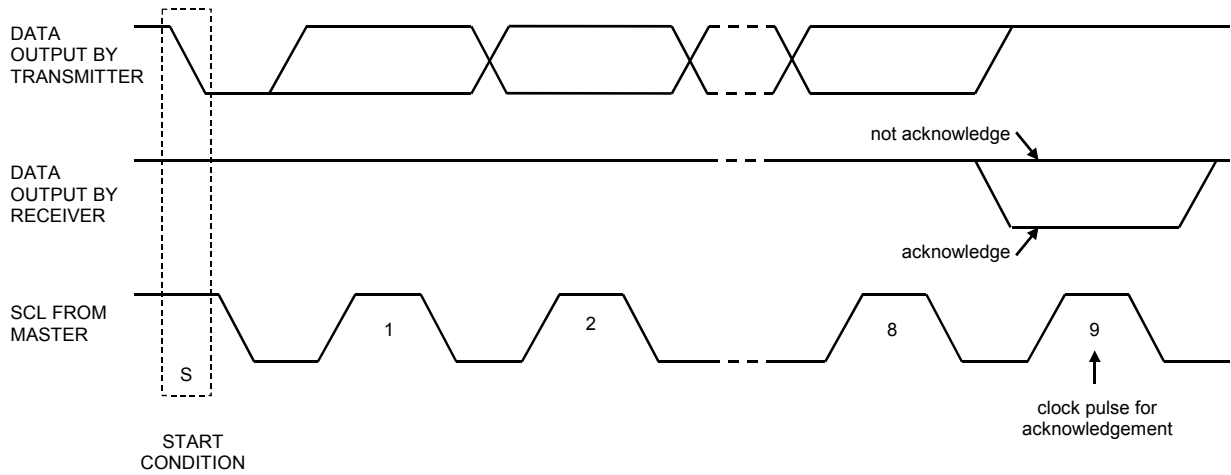
Figure 13. START and STOP conditions

Figure 14. Acknowledge on the I^{2}C-bus
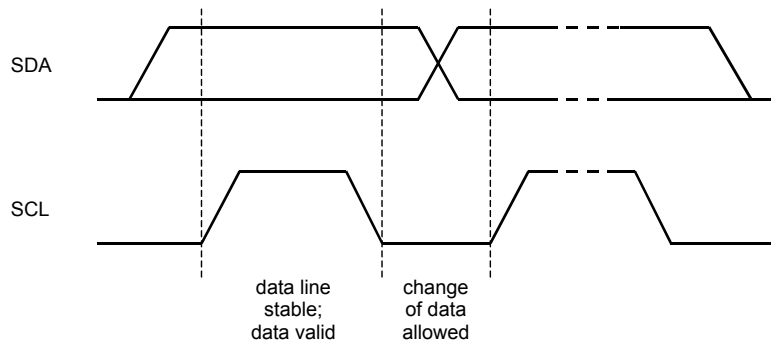
Figure 15. Bit transfer on the I^{2}C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	AUTO	0	BIAS	STBY
01H	Switch	MUTE	0	VCR1	VCR0	MONO	0	TV1	TV0
02H	Main Volume	0	0	L2	L1	L0	1	1	1
03H	Zerocross	0	VMONO	0	0	0	ZERO	ZTM1	ZTM0
04H	Video switch	0	0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
05H	Video output enable	0	TVFB	0	VCRV	TVB	TVG	TVR	TVV
06H	Video clamp	0	VCLP1	VCLP0	0	CLAMP1	CLAMP0	0	0
07H	S/F Blanking control	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
08H	S/F Blanking monitor	0	0	0	TVMON	VCMON	FVCR	SVCR1	SVCR0
09H	Monitor mask	MCOMN	0	0	MTV	MVC	MFVCR	MSVCR	0

When the PDN pin goes "L", the registers are initialized to their default values.
While the PDN pin = "H", all registers can be accessed.
Do not write any data to the register over 09H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	AUTO	0	BIAS	STBY
R/W		R/W							
Default		0	0	0	0	1	0	1	1

STBY: Standby control
   0: Normal Operation
   1: Standby Mode (default). All registers are not initialized.

Source of TVOUT	:	fixed to VCRIN,
Source of VCROUT	:	fixed to TVIN
Source of TVVOUT	:	fixed to VCRVIN (or Hi-Z),
Source of TVRC	:	fixed to VCRRC (or Hi-Z),
Source of TVG	:	fixed to VCRG (or Hi-Z),
Source of TVB	:	fixed to VCRB (or Hi-Z),
Source of VCRVOUT	:	fixed to TVVIN (or Hi-Z),
Source of TVFB	:	fixed to VCRFB (or Hi-Z),
Source of TVSB	:	fixed to VCRSB.

BIAS: Audio output control
   0: Normal operation
   1: ALL Audio outputs to GND (default)

AUTO: Auto startup bit
   0: Auto startup disable (Manual startup).
   1: Auto startup enable (default).
    Note 23. When the SBIO1 bit = "1"(default = "0"), the change of AUTO bit may cause a "L" pulse on INT pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Switch	MUTE	0	VCR1	VCR0	MONO	1	TV1	TV0
R/W		R/W							
Default		1	0	0	1	0	1	0	1

TV1-0: TVOUTL/R pins source switch
   00: AMP
   01: VCRINL/R pins (default)
   10: MUTE
   11: Reserved

MONO: Mono select for TVOUTL/R pins
   0: Stereo. (default)
   1: Mono. (L+R)/2

VCR1-0: VCROUTL/R pins source switch
   00: AMP
   01: TVINL/R pins (default)
   10: MUTE
   11: Reserved

MUTE: Mute switch
   0: Normal operation
   1: Mute (default)
      When Mute bit = "1", TVOUTL/R outputs VCOM voltage after TVOUTL/R output is zero-crossing
      (ZERO bit= "1").
      Set the MUTE bit= "1" to pass for 100ms after setting the PDN pin="H".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Main volume	0	0	L2	L1	L0	1	1	1
R/W		R/W							
Default		0	0	0	1	1	1	1	1

L2-0: Volume #0 control
  Those registers control both Lch and Rch of Volume #0.
     111:   Volume gain = +12dB
     110:   Volume gain = +9dB
     101:   Volume gain = +6dB
     100:   Volume gain = +3dB
     011:   Volume gain = +0dB (default)
     010: Volume gain = -3dB
     001: Volume gain = -6dB
     000: MUTE

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Zerocross	0	VMONO	0	0	0	ZERO	ZTM1	ZTM0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

ZTM1-0: The time length control of zero-cross timeout
  00:   typ. 12.8ms, max. 20.2ms (default)
  01:   typ. 25.6ms
  10:   typ. 51.2ms
  11:   typ. 102.4ms

ZERO: Zero-cross detection enable for TVOUT output
  0: Disable
      The TVOUTL/R outputs VCOM voltage immediately without zero-cross when MUTE bit = "1".
      The TVOUTL/R outputs of TV1-0 switch immediately without zero-cross when MUTE bit = "0".
  1: Enable (default)
      The TVOUTL/R outputs VCOM voltage when timeout or zero-cross before timeout when MUTE bit = "1".
      The TVOUTL/R outputs of TV1-0 switch when timeout or zero-cross before timeout when MUTE bit = "0".

VMONO: Mono select for VCROUTL/R pins
  0: Stereo. (default)
  1: Mono. (L+R)/2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Video switch	0	0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
R/W		R/W							
Default		0	0	0	1	1	1	0	0

VTV2-0: Selector for TV video output
    Refer the Table 7.

VVCR2-0: Selector for VCR video output
    Refer the Table 8.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Output Enable	0	TVFB	0	VCRV	TVB	TVG	TVR	TVV
R/W		R/W							
Default		0	0	0	0	0	0	0	0

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
TVFB: TVFB output control
    0: Hi-Z (default)
    1: Active.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Video Clamp	0	VCLP1	VCLP0	0	CLAMP1	CLAMP0	0	0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

CLAMP1: Encoder R/Chroma (ENCRC pin) input clamp control
    0: DC restore clamp active (for RED signal. default)
    1: Biased (for Chroma signal.)

CLAMP0: VCR R/C (VCRC pin) input clamp control
    0: DC restore clamp active (for RED signal)
    1: Biased (for Chroma signal. default.)

VCLP1-0: DC restore source control
    00:   ENCV pin (default)
    01:   ENCY pin
    10:   VCRVIN pin
    11:   (Reserved)
    When the AUTO bit = "1", the source is fixed to VCRVIN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	S/F Blanking	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
R/W		R/W							
Default		0	0	0	0	0	0	0	0

FB1-0: TV Fast Blanking output control (for TVFB pin)
    00:   0V (default)
    01:   2V<, 4V(typ.) at 150Ω load
    10:   follow VCR FB input (4V/0V)
    11:   (Reserved)

SBT1-0: TV Slow Blanking output control (for TVSB pin. minimum load is 10kΩ.)
    00:   < 2V (default)
    01:   5V <, < 7V
    10:   (Reserved)
    11:   10V <

SBV1-0: VCR Slow Blanking output control (for VCRSB pin. minimum load is 10kΩ.)
    00:   < 2V (default)
    01:   5V <, < 7V
    10:   (Reserved)
    11:   10V <

SBIO1-0: TV/VCR Slow Blanking I/O control
    Refer the Table 13.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	SB/FB monitor	0	0	0	TVMON	VCMON	FVCR	SVCR1	SVCR0
	R/W	READ							
	Default	0	0	0	0	0	0	0	0

SVCR1-0: VCR Slow blanking status monitor
   SVCR1-0 bits reflect the voltage at VCRSB pin only when the VCRSB is in the input mode.
   When the VCRSB is in the output mode, SVCR1-0 bits hold previous value.

VCRSB pin input level	SVCR1 bit	SVCR0 bit
< 2V	0	0
4.5V to 7V	0	1
(Reserved)	1	0
9.5V <	1	1

Table 19. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor
   This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR bit
< 0.4V	0
1V <	1

Table 20. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VCMON:
TVMON:
   Refer the Table 16.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Monitor mask	MCOMN	0	0	MTV	MVC	MFVCR	MSVCR	0
	R/W	R/W							
	Default	0	0	0	0	1	0	0	0

MSVCR: SVCR1-0 bits Monitor mask
   0: The INT pin reflects the change of SVCR1-0 bit. (default)
   1: The INT pin does not reflect the change of SVCR1-0 bits.

MFVCR: FVCR Monitor mask
   0: The INT pin reflects the change of FVCR bit. (default)
   1: The INT pin does not reflect the change of FVCR bit.

MVC: VCR input monitor mask
   Refer the Table 18.

MTV: TV input monitor mask
   Refer the Table 17.

MCOMN: Monitor mask option
   Refer the Table 16.

SYSTEM DESIGN

Figure 16 and Figure 17 shows the system connection diagram example. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.
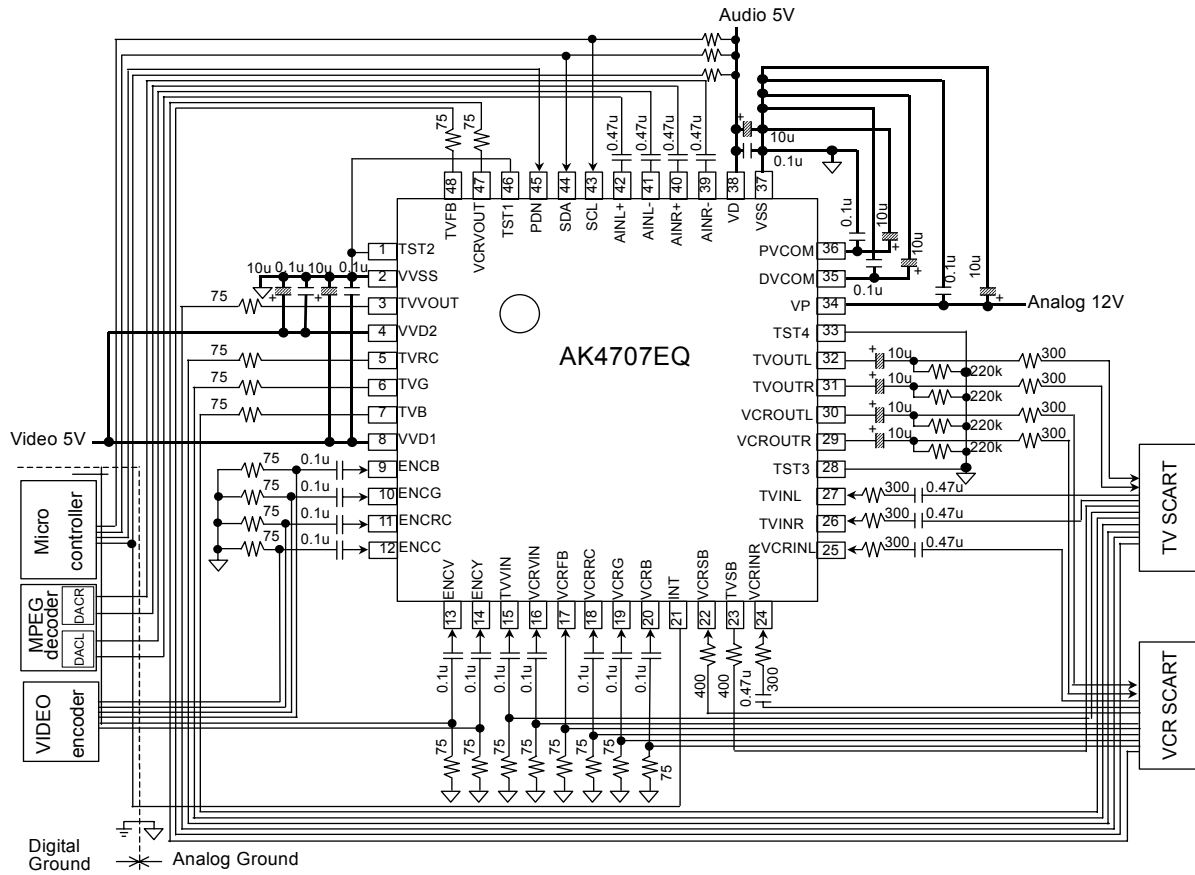

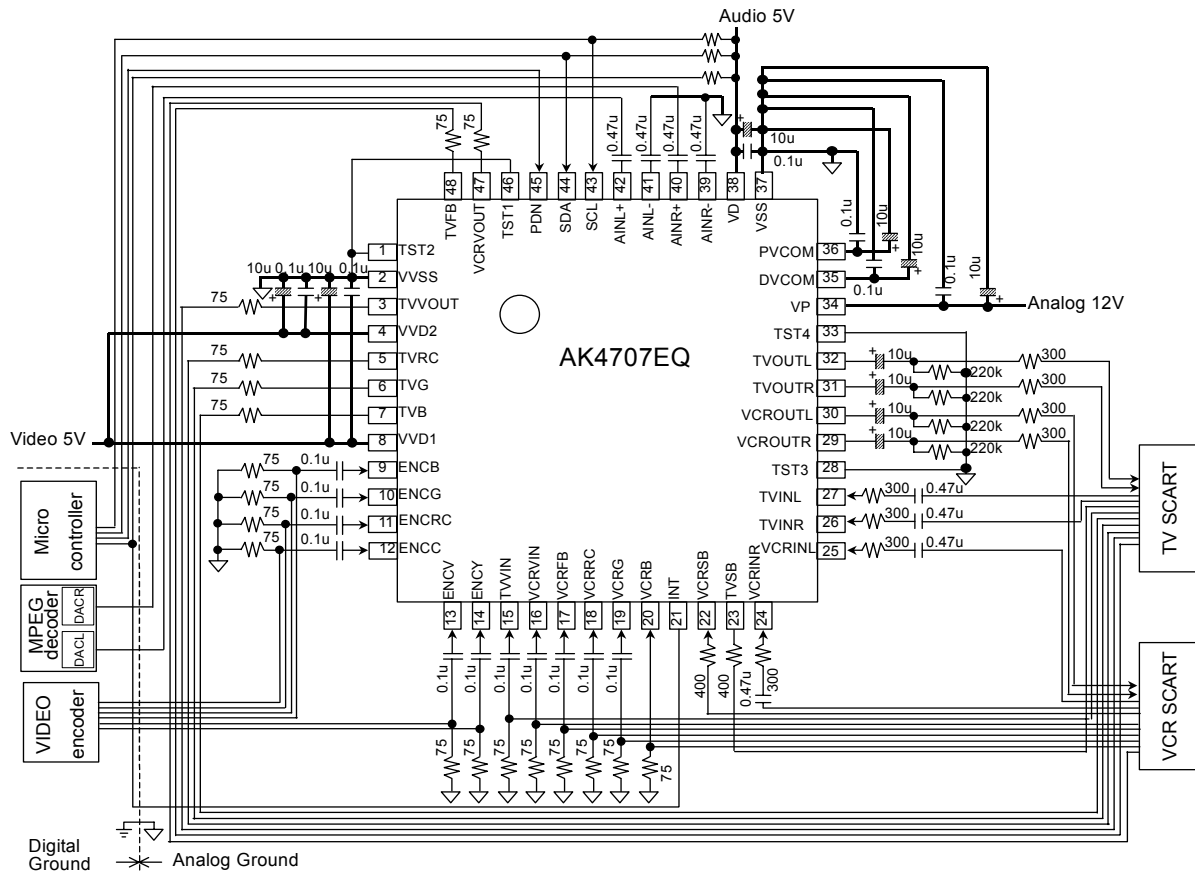Figure 16. Typical Connection Diagram (Full Differential Stereo Input)

Figure 17. Typical Connection Diagram (Single-ended Input)

■ **Grounding and Power Supply Decoupling**

VD, VP, VVD1, VVD2, VSS and VVSS should be supplied from analog supply unit with low impedance and be separated from system digital supply. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor should be attached to these pins to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitor should be placed as near to VD, VP, VVD1, VVD2 as possible.

■ **Voltage Reference**

Each DVCOM/PVCOM are signal ground of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor should be attached to these VCOM pins to eliminate the effects of high frequency noise. No load current may be drawn from these VCOM pins. All signals, especially clocks, should be kept away from these VCOM pins in order to avoid unwanted coupling into the AK4707.
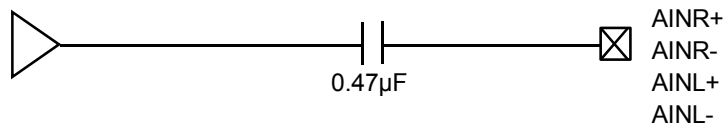
■ **Analog Audio Outputs**

The analog outputs are also single-ended and centered on 5.6V(typ.). The output signal range is typically 2Vrms. The DC voltage on analog outputs are eliminated by AC coupling.
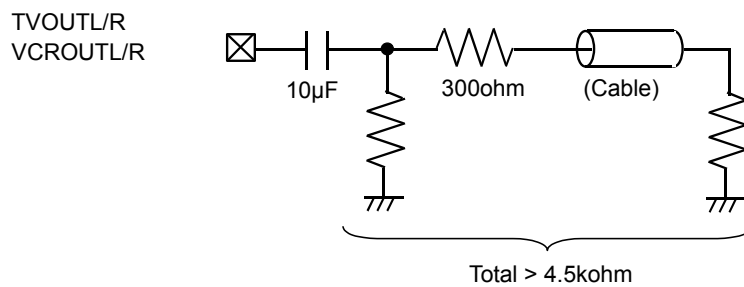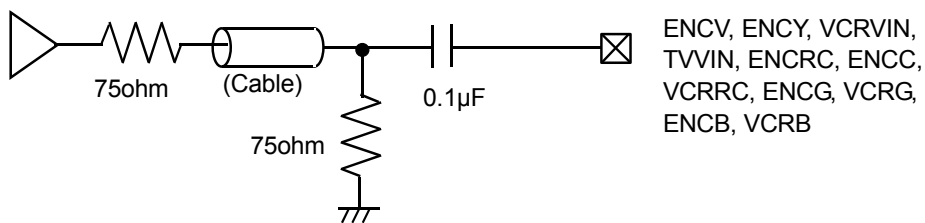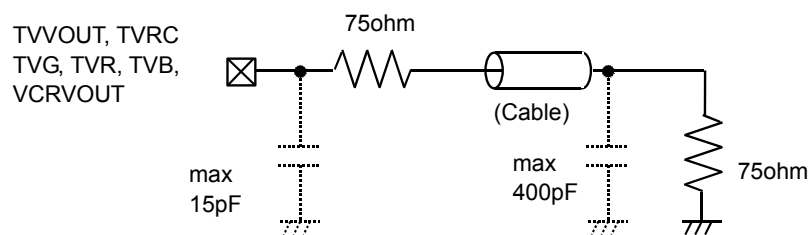
■ **External Circuit Example**

Analog Audio Input pin
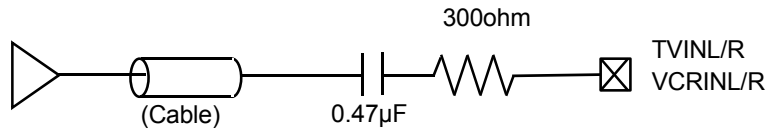
```
                                            300ohm
   ▷────────▭────────┤├──────/\/\/\──────⊠   TVINL/R
            (Cable)      0.47µF                   VCRINL/R
```

Analog Audio Input pin

```
   ▷──────────────────┤├─────────────────⊠   AINR+
                         0.47µF               AINR-
                                              AINL+
                                              AINL-
```

Analog Audio Output pin

```
   TVOUTL/R
   VCROUTL/R
      ⊠────┤├────┬────/\/\/\────▭────────┐
          10µF    │   300ohm   (Cable)    │
                 ╲╱                      ╲╱
                 ╱╲                      ╱╲
                  ⏚                       ⏚

              └────────────────┬──────────────┘
                          Total > 4.5kohm
```

Analog Video Input pin

```
                                                 ENCV, ENCY, VCRVIN,
   ▷───/\/\/\───▭──────┬───────┤├────────⊠      TVVIN, ENCRC, ENCC,
       75ohm  (Cable)   │      0.1µF             VCRRC, ENCG, VCRG,
                       ╲╱                        ENCB, VCRB
                       ╱╲
                    75ohm
                        ⏚
```

Analog Video Output pin

```
                           75ohm
   TVVOUT, TVRC
   TVG, TVR, TVB,
   VCRVOUT
      ⊠────┬────/\/\/\────▭────────┬────┐
           ┊            (Cable)     ┊    ╲╱
           ┊                        ┊    ╱╲  75ohm
          max                      max    ⏚
          15pF                     400pF
```

Slow Blanking pin

TVSB
VCRSB

400ohm
(max 500ohm)

max 3nF
(with 400ohm)

min: 10k ohm

Fast Blanking Input pin

75ohm
(Cable)

75ohm

VCRFB

Fast Blanking Output pin

75ohm

TVFB

(Cable)

75ohm
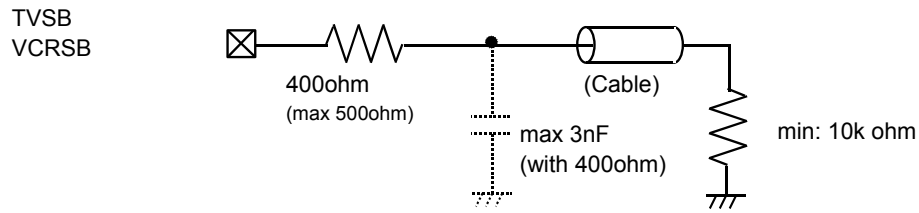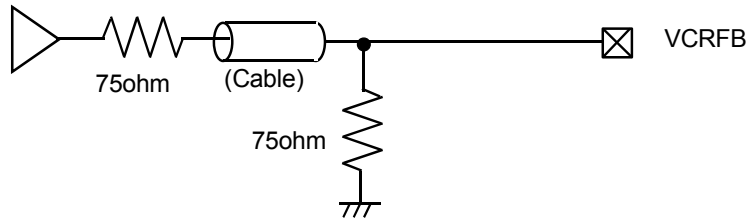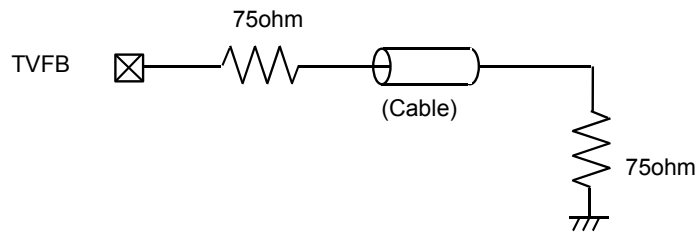
PACKAGE

48pin LQFP(Unit:mm)
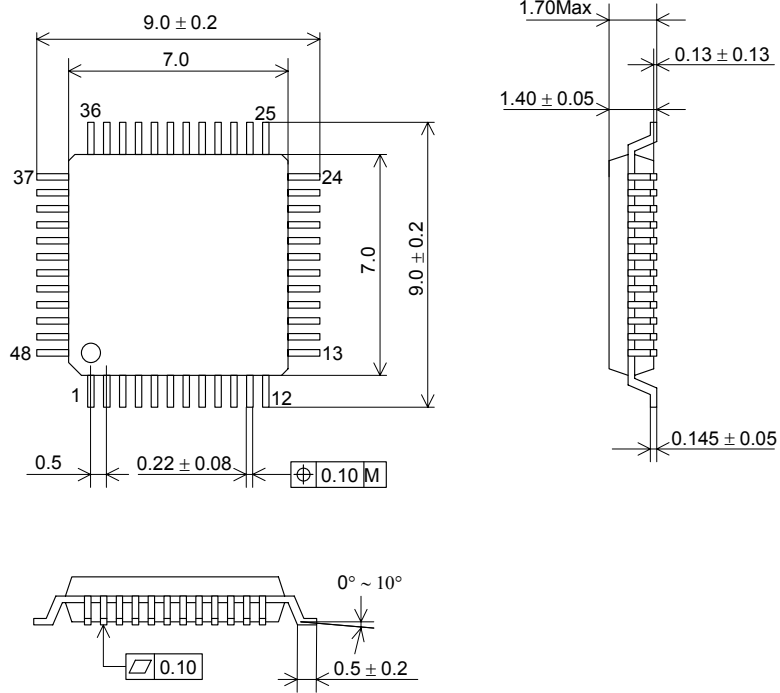
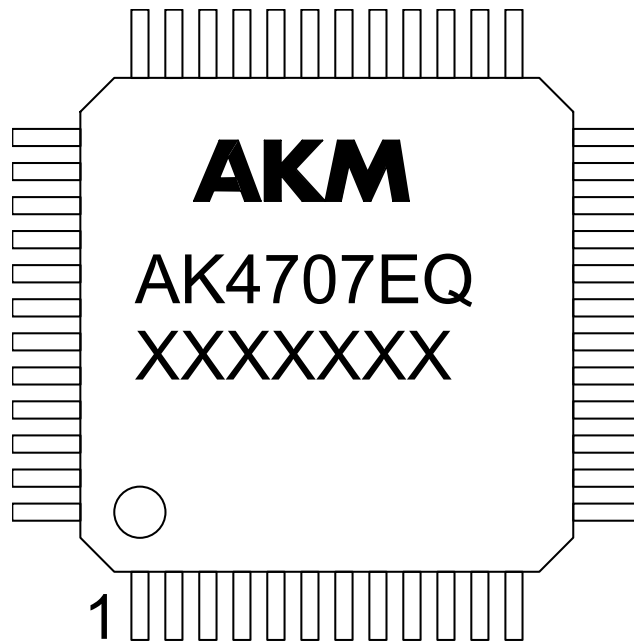### ■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING

AKM

AK4707EQ

XXXXXXX

XXXXXXXX: Date code identifier

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/10/16	00	First Edition		

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