AK4958

24bit Stereo CODEC with MIC/SPK/VIDEO-AMP & LDO

GENERAL DESCRIPTION

The AK4958 is a 24-bit stereo CODEC with a microphone, speaker, video amplifiers and LDO. The input circuits include a microphone amplifier and the output circuits include a speaker amplifier. It is suitable for portable application with recording/playback function. A one channel composite In/Out video amplifier is also integrated. The AK4958 is available in a small 32-pin BGA (3.5mm x 3.5mm, 0.5mm pitch: AK4958EG) and a 25-pin CSP (2.2mm x 2.2mm, 0.4mm pitch: AK4958ECB) packages saving mounting area on the board.

FEATURES

1. Recording Functions

- **Analog Input**
  - **(AK4958EG)**
    - **Stereo Single-ended input with two Selectors**
  - **(AK4958ECB)**
    - **Stereo Single-ended input**
- **Microphone Amplifier**
  - **(+30dB, +25dB, +21dB, +18dB, +15dB, +12dB, +6dB, 0dB)**
- **Digital ALC (Automatic Level Control)**
  - **- Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute**
  - **- Motor Noise Reduction Circuit**
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
  - **S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)**
- **Microphone Sensitivity Compensation (with Moving Average Data Output Circuit)**
- **Automatic Wind Noise Reduction Filter**
- **5-Band Notch Filter**
  - **Include Dynamic Gain Control**
- **Stereo Separation Emphasis Circuit**
- **Digital Microphone Interface**

2. Playback Functions

- **Soft Mute**
- **Digital ALC (Automatic Level Control)**
  - **- Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute**
- **Digital Volume Control**
  - **- +6dB ~ –89.5dB, 0.5dB Step & Mute)**
- **Stereo Separation Emphasis Circuit**
- **Stereo Line Output**
  - **- Output Voltage: 1Vrms (AVDD= 3.3V)**
  - **- S/(N+D): 85dB**
  - **- S/N: 92dB**
- **Mono Mixing Output**
- **Mono Speaker-Amplifier**
  - **- S/(N+D): 65dB@150mW, 60dB@250mW,**
  - **- S/N: 90dB**
  - **- BTL Output**
  - **- Output Power: 400mW@8Ω (AVDD=3.3V)**
- **Analog Mixing: BEEP Input**
- **Bass Boost Circuit**
- **3-band Dynamic Range Control Circuit**

3. Master Clock:
Reference Clock Input Frequency
(1) MCKI Reference PLL Mode
Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
(2) BICK Reference PLL Mode
Frequencies: 32fs or 64fs (BICK pin)
(3) External Clock Mode
Frequencies: 256fs, 512fs or 1024fs (MCKI pin)
Output Master Clock Frequency: 64fs/128fs/256fs/512fs

4. Sampling Frequencies
- **MCKI Reference PLL Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **BICK Reference PLL Master Mode:**
  8kHz ~ 48kHz
- **EXT Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

5. Master/Slave Mode

6. μP I/F:
(AK4958EG)
- **3-wire Serial, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)**

(AK4958ECB)
- **I^2C Bus (Ver 1.0, 400kHz Fast-Mode)**

7. Master/Slave Mode

8. Audio Interface Format: MSB First, 2's complement
- **ADC: 24bit MSB justified, 16/24bit I^2S**
- **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 24bit I^2S**

9. Video Functions
- **One Composite Signal Input**
- **Video Amplifier for Composite Signal Output**
  Gain: +12 / +16.5dB
- **Low Pass Filter**

10. Ta = –30 ~ 85°C

11. Power Supply:
(AK4958EG)
- **Analog Power Supply (AVDD): 2.8 ~ 3.6V**
- **Digital Power Supply (DVDD): 1.6 ~ 2.0V**
- **Digital I/O Power Supply (TVDD): 1.6 or DVDD – 0.2 ~ 3.6V**

(AK4958ECB)
- **Analog Power Supply (AVDD): 2.8 ~ 3.6V**
- **Digital & Digital I/O Power Supply (DTVDD): 1.6 ~ 2.0V**

12. Package:
(AK4958EG)
- **32pin BGA (3.5 x 3.5 mm, 0.5mm pitch)**

(AK4958ECB)
- **25pin CSP (2.2 x 2.2 mm, 0.4mm pitch)**

■ Block Diagram

▪ AK4958EG

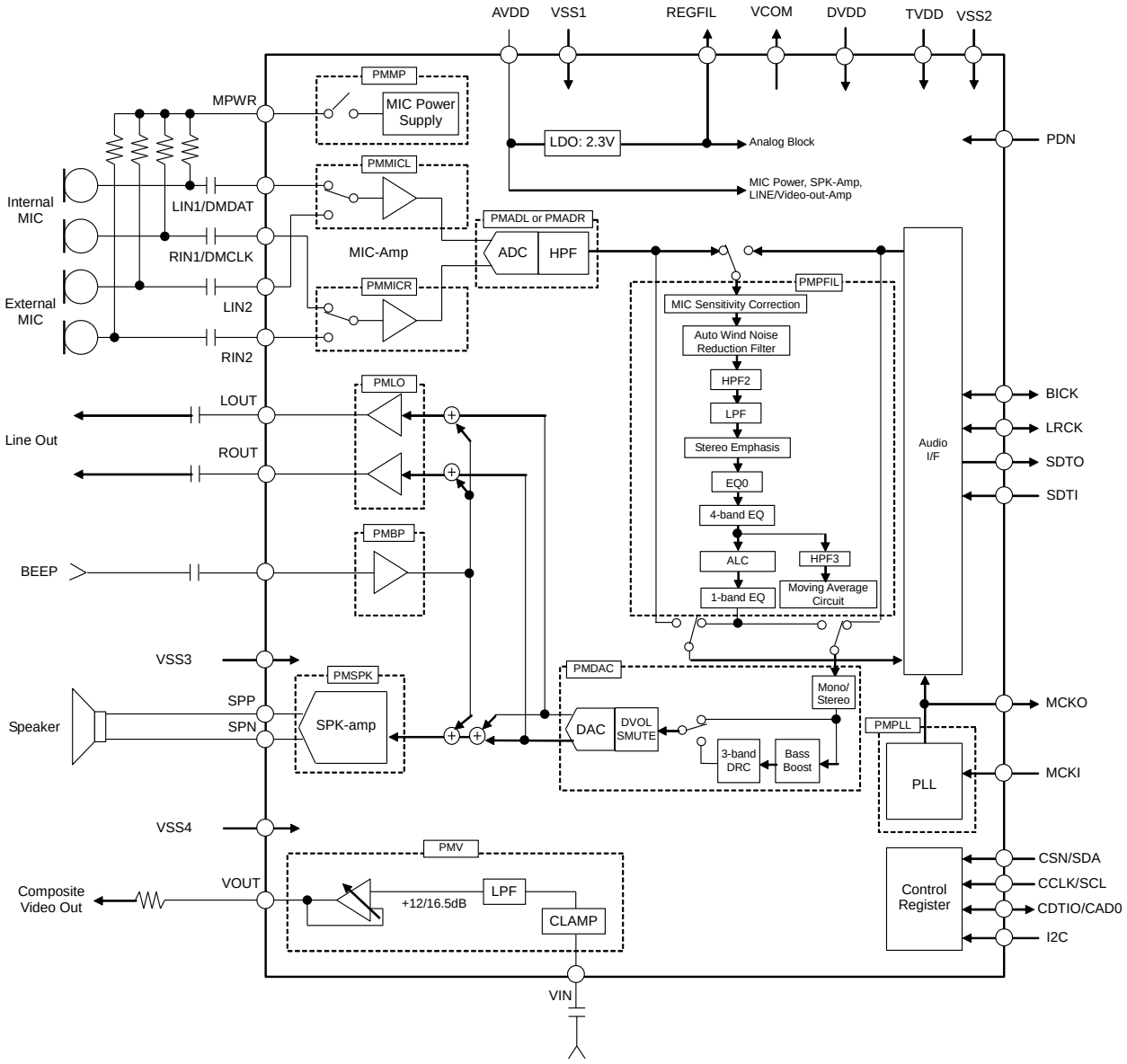


Figure 1. Block Diagram (AK4958EG)

▪ AK4958ECB

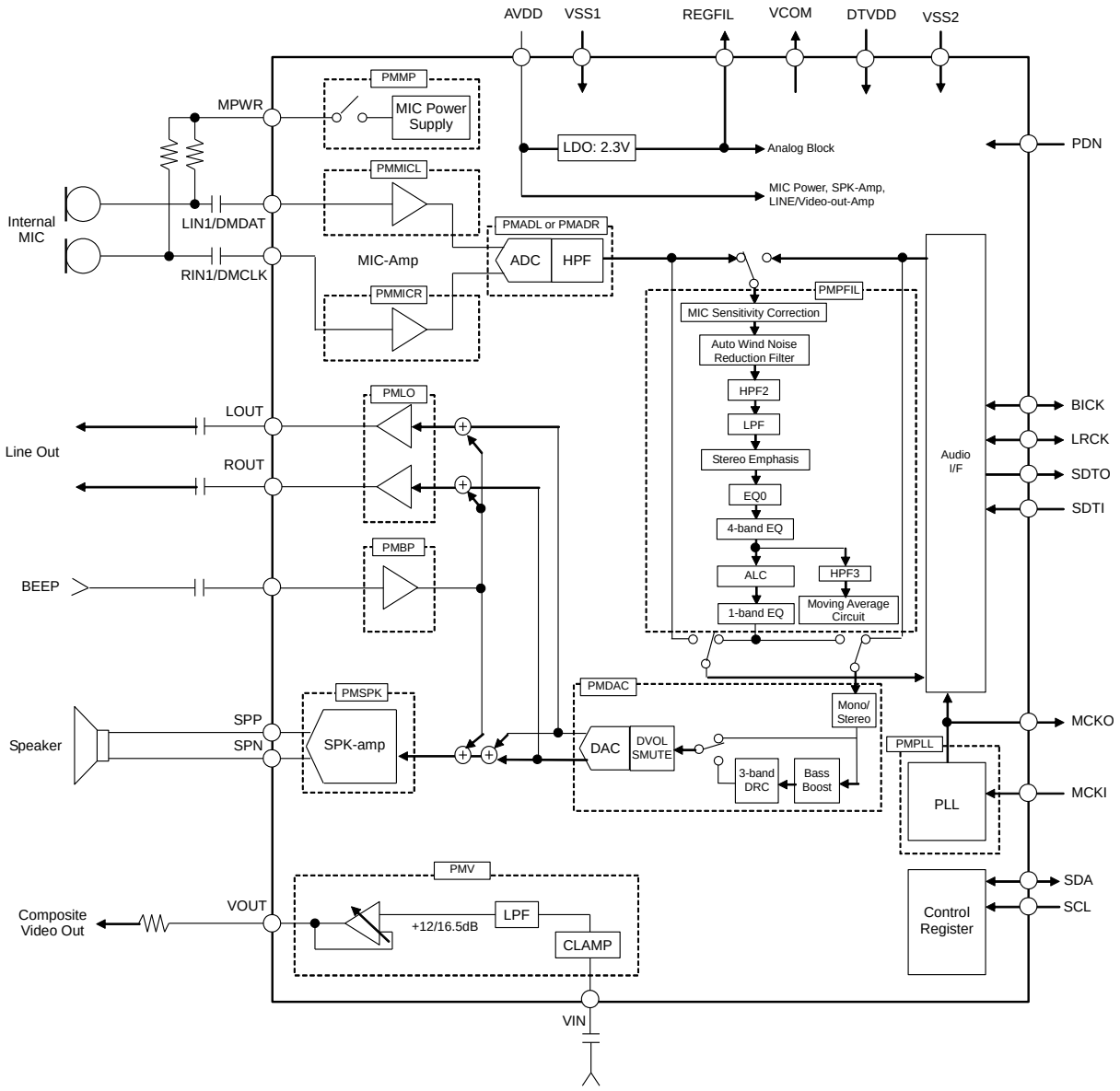


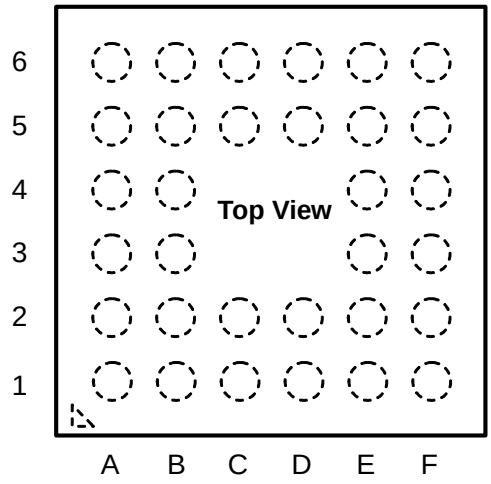
Figure 2. Block Diagram (AK4958ECB)

■ Ordering Guide

AK4958EG	–30 ~ +85°C	32-pin BGA (0.5mm pitch)
AK4958ECB	–30 ~ +85°C	25-pin CSP (0.4mm pitch)
AKD4958EG	Evaluation board for AK4958EG	
AKD4958ECB	Evaluation board for AK4958ECB	

■ Pin Layout

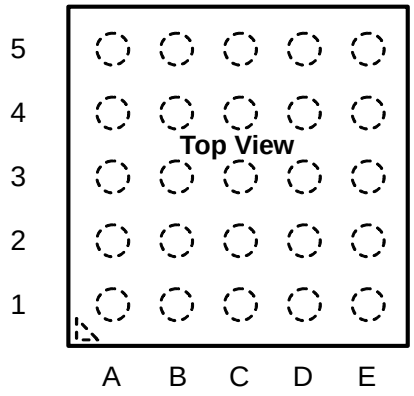
▪ AK4958EG



6	MPWR	ROUT	REGFIL	VCOM	VSS1	VIN
5	RIN2	BEEP	LOUT	AVDD	VOUT	VSS4
4	RIN1 /DMCLK	LIN2			SPP	SPN
3	LIN1 /DMDAT	I2C			VSS2	VSS3
2	CDTIO /CAD0	CSN /SDA	SDTI	MCKO	MCKI	DVDD
1	CCLK /SCL	LRCK	BICK	SDTO	TVDD	PDN
	A	B	C	D	E	F

Top View

▪ AK4958ECB



5	PDN	VSS2	SPP	SPN	VIN
4	MCKO	MCKI	DTVDD	VOUT	VSS1
3	SDTI	SDTO	BEEP	AVDD	VCOM
2	LRCK	BICK	RIN1 /DMCLK	LOUT	REGFIL
1	SCL	SDA	LIN1 /DMDAT	MPWR	ROUT
	A	B	C	D	E

Top View

■ Comparison Table of the AK4958EG and AK4958ECB

Function	AK4958EG	AK4958ECB
Digital I/O Voltage	TVDD = 1.6 or DVDD-0.2 ~ 3.6V	DTVDD = 1.6V ~ 2.0V *Digital Power and Digital Interface Supply share a pin.
Number of VSS Pin	Four pins	Two pins
ADC Input Channel	2 Stereo (LIN1/RIN1, LIN2/RIN2)	1 Stereo (LIN1/RIN1)
Control I/F mode	3-wire / I2C	I2C *Slave address "0010011"
Package	32BGA (3.5 x 3.5mm, 0.5mm pitch)	25CSP (2.2 x 2.2mm, 0.4mm pitch)

PIN/FUNCTION (AK4958EG)

No	Pin Name	I/O	Function
Power Supply			
D5	AVDD	-	Analog Power Supply, 2.8 ~ 3.6V This pin must be connected to VSS1 through a 0.1µF ceramic capacitor.
D6	VCOM	O	Common Voltage Output Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.
E6	VSS1	-	Ground 1
F2	DVDD	-	Digital Power Supply, 1.6 ~ 2.0V This pin must be connected to VSS2 through a 0.1µF ceramic capacitor.
E1	TVDD	-	Digital Interface Supply, 1.6 or DVDD-0.2V ~ 3.6V
C6	REGFIL	O	LDO Voltage Output pin for Analog Logic (typ 2.3V) This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.
E3	VSS2	-	Ground 2
F3	VSS3	-	Ground 3
F5	VSS4	-	Ground 4
Audio Interface			
E2	MCKI	I	Master Clock Input (Note 1)
D2	MCKO	O	Master Clock Output
B1	LRCK	I/O	Channel Clock Pin (Note 1)
C1	BICK	I/O	Audio Serial Data Clock Pin (Note 1)
C2	SDTI	I	Audio Serial Data Input (Note 1)
D1	SDTO	O	Audio Serial Data Output
Control Register Interface			
B2	CSN	I	Chip Select Pin (I2C pin = "L") (Note 1)
	SDA	I/O	Control Data Input/Output (I2C pin = "H") (Note 1)
A1	CCLK	I	Control Data Clock Pin (I2C pin = "L") (Note 1)
	SCL	I	Control Data Clock Pin (I2C pin = "H") (Note 1)
A2	CDTIO	I/O	Control Data Input/Output (I2C pin = "L") (Note 1)
	CAD0	I	Chip Address Select Pin (I2C pin = "H") (Note 1)
B3	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial (Note 1)

Note 1. All input pins except analog input pins (BEEP, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

No	Pin Name	I/O	Function
Microphone Block			
3	LIN1	I	Lch Analog Input 1 (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input (DMIC bit = "1") (Note 1)
4	RIN1	I	Rch Analog Input 1 (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock (DMIC bit = "1")
5	LIN2	I	Lch Analog Input 2
6	RIN2	I	Rch Analog Input 2
2	MPWR	O	Microphone Power Supply
MIN Block			
1	BEEP	I	BEEP Signal Input
Lineout Block			
31	LOUT	O	Lch Analog Output
32	ROUT	O	Rch Analog Output
Speaker Block			
21	SPP	O	Speaker Amp Positive Output
22	SPN	O	Speaker Amp Negative Output
Video Block			
25	VIN	I	Composite Video Input
24	VOUT	O	Composite Video Output
Other Functions			
18	PDN	I	Reset & Power-down Pin (Note 1) "L": Reset & Power-down, "H": Normal Operation

Note 1. All input pins except analog input pins (BEEP, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

PIN/FUNCTION (AK4958ECB)

No	Pin Name	I/O	Function
Power Supply			
D3	AVDD	-	Analog Power Supply, 2.8 ~ 3.6V This pin must be connected to VSS1 through a 0.1µF ceramic capacitor.
E3	VCOM	O	Common Voltage Output Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.
E4	VSS1	-	Ground 1
C4	DTVDD	-	Digital Power & Digital Interface Supply, 1.6 ~ 2.0V This pin must be connected to VSS2 through a 0.1µF ceramic capacitor.
E2	REGFIL	O	LDO Voltage Output pin for Analog Logic (typ 2.3V) This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.
B5	VSS2	-	Ground 2
Audio Interface			
B4	MCKI	I	Master Clock Input (Note 2)
A4	MCKO	O	Master Clock Output
A2	LRCK	I/O	Channel Clock (Note 2)
B2	BICK	I/O	Audio Serial Data Clock (Note 2)
A3	SDTI	I	Audio Serial Data Input (Note 2)
B3	SDTO	O	Audio Serial Data Output
Control Register Interface			
B1	SDA	I/O	Control Data Input/Output (Note 2)
A1	SCL	I	Control Data Clock Pin (Note 2)
Microphone Block			
C1	LIN1	I	Lch Analog Input 1 (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input (DMIC bit = "1") (Note 2)
C2	RIN1	I	Rch Analog Input 1 (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock Pin (DMIC bit = "1")
D1	MPWR	O	Microphone Power Supply
BEEP Block			
C3	BEEP	I	BEEP Signal Input
Lineout Block			
D2	LOUT	O	Lch Analog Output
E1	ROUT	O	Rch Analog Output
Speaker Block			
C5	SPP	O	Speaker Amp Positive Output
D5	SPN	O	Speaker Amp Negative Output
Video Block			
E5	VIN	I	Composite Video Input
D4	VOUT	O	Composite Video Output
Other Functions			
A5	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation

Note 2. All input pins except analog input pins (BEEP, LIN1, RIN1, VIN) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, LOUT, ROUT, BEEP, RIN2, LIN2, VIN, VOUT	These pins must be open.
	LIN1, RIN1	DMIC bit = "0", and these pins must be open.
Digital	MCKO, SDTO	These pins must be open.
	MCKI, SDTI	These pins must be connected to VSS2.
	LRCK, BICK	M/S bit = "0", and these pins must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(AK4958EG: VSS1=VSS2=VSS3=VSS4=0V, AK4958ECB: VSS1=VSS2=0V; Note 3)

Parameter			Symbol	min	max	Unit
Power Supplies (AK4958EG)	Analog		AVDD	–0.3	6.0	V
	Digital		DVDD	–0.3	2.5	V
	Digital I/O		TVDD	–0.3	6.0	
Power Supplies (AK4958ECB)	Analog		AVDD	–0.3	6.0	V
	Digital, Digital I/O		DTVDD	–0.3	2.5	
Input Current, Any Pin Except Supplies			IIN	-	±10	mA
Analog Input Voltage (Note 4)			VINA	–0.3	AVDD+0.3	V
Digital Input Voltage	(AK4958EG, Note 5)		VIND	–0.3	TVDD+0.3	V
	(AK4958ECB, Note 6)		VIND	–0.3	DTVDD+0.3	V
	(Note 8)		VIND	–0.3	6.0	V
Ambient Temperature (powered applied)			Ta	–30	85	°C
Storage Temperature			Tstg	–65	150	°C
Maximum Power Dissipation (Note 8)		AK4958EG	Pd1	-	460	mW
		AK4958ECB	Pd1	-	460	mW

Note 3. All voltages are with respect to ground. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.

Note 4. BEEP, LIN1, RIN1, LIN2, RIN2, VIN, I2C pins

Note 5. PDN, CDTIO, SDTI, LRCK, BICK and MCKI pins

Note 6. PDN, SDTI, LRCK, BICK, MCKI pins

Note 7. CSN/SDA and CCLK/SCL pins

Note 8. This power is the AK4958 internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 80°C/W at JESD51-9 (2p2s) for the AK4958EG and 56°C/W for the AK4958ECB. When Pd =460mW and the θja is 80°C/W for the AK4958EG, and 56°C/W for the AK4958ECB, the junction temperature does not exceed 125°C. In this case, the AK4958 will not be damaged by its internal power dissipation. Therefore, the AK4958EG should be used in the condition of θja ≤ 80°C/W, and the AK4958ECB should be used in the condition of θja ≤ 56°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AK4958EG)

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 9)	Analog	AVDD	2.8	3.3	3.6	V
	Digital	DVDD	1.6	1.8	2.0	V
	Digital I/O (Note 10)	TVDD	1.6 or DVDD-0.2	1.8	3.6	V

Note 3. All voltages are with respect to ground.

Note 9. The power-up sequence between AVDD, DVDD and TVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 10. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

*** When TVDD is powered ON and the PDN pin is "L", AVDD and DVDD can be powered ON/OFF. When the AK4958EG is powered ON from power-down state, the PDN pin must be "H" after all power supplies (AVDD, DVDD and TVDD) are ON.**

RECOMMENDED OPERATING CONDITIONS (AK4958ECB)

(VSS1=VSS2 =0V; Note 3)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 9)	Analog	AVDD	2.8	3.3	3.6	V
	Digital, Digital I/O	DTVDD	1.6	1.8	2.0	V

Note 3. All voltages are with respect to ground.

Note 11. The power-up sequence between AVDD and DTVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

*** When DTVDD is powered ON and the PDN pin is "L", AVDD can be powered ON/OFF. When the AK4958ECB is powered ON from power-down state, the PDN pin must be "H" after all power supplies (AVDD and DTVDD) are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; fs=48kHz, BICK=64fs;Signal Frequency=1kHz; 24bit Data; Measurement Bandwidth =20Hz ~ 20kHz; unless otherwise specified; AK4958EG: AVDD = 3.3V, DVDD = TVDD= 1.8V;VSS1=VSS2=VSS3=VSS4=0V, AK4958ECB: AVDD = 3.3V, DTVDD = 1.8V; VSS1=VSS2=0V)

Parameter			min	typ	max	Unit
Microphone Amplifier: LIN1, RIN1, LIN2, RIN2 pins						
Input Resistance			20	30	42	kΩ
Gain	MGAIN2-0 bits = "000"		-1	0	+1	dB
	MGAIN2-0 bits = "001"		+5	+6	+7	dB
	MGAIN2-0 bits = "010"		+11	+12	+13	dB
	MGAIN2-0 bits = "011"		+14	+15	+16	dB
	MGAIN2-0 bits = "100"		+17	+18	+19	dB
	MGAIN2-0 bits = "101"		+20	+21	+22	dB
	MGAIN2-0 bits = "110"		+24	+25	+26	dB
	MGAIN2-0 bits = "111"		+29	+30	+31	dB
Microphone Power Supply: MPWR pin						
Output Voltage	MICL bit = "0"		2.2	2.4	2.6	V
	MICL bit = "1"		1.8	2.0	2.2	V
Output Noise Level (A-weighted)			-	–108	-	dBV
Load Resistance			0.5	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	100	-	dB
ADC Analog Input Characteristics AK4958EG: LIN1/RIN1/LIN2/RIN2 pins → ADC (Programmable Filter = OFF) AK4958ECB: LIN1/RIN1 pins → ADC (Programmable Filter = OFF)						
Resolution			-	-	24	Bits
Input Voltage (Note 12)		(Note 13)	-	0.261	-	Vpp
		(Note 14)	1.86	2.07	2.28	Vpp
S/(N+D) (–1dBFS)		(Note 13)	73	83	-	dBFS
		(Note 14)	-	85	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 13)	78	88	-	dB
		(Note 14)	-	96	-	dB
S/N (A-weighted)		(Note 13)	78	88	-	dB
		(Note 14)	-	96	-	dB
Interchannel Isolation		(Note 13)	75	90	-	dB
		(Note 14)	-	100	-	dB
Interchannel Gain Mismatch		(Note 13)	-	0	0.5	dB
		(Note 14)	-	0	0.5	dB
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	80	-	dB

Note 12. Vin = 0.9 x 2.3Vpp (typ) @MGAIN2-0 bits = "000" (0dB)
Note 13. MGAIN2-0 bits = "110" (+18dB)
Note 14. MGAIN2-0 bits = "000" (0dB)

Parameter			min	typ	max	Unit
DAC Characteristics:						
Resolution			-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, DVOL=OVOL =0dB, R_L=10kΩ , PMBP bit = "0", LVCM1-0 bits = "01"						
Output Voltage (Note 15)	(0dBFS)	LVCM0 bit = "0"	-	2.26	-	Vpp
		LVCM0 bit = "1"	-	1.00	-	Vrms
Output Voltage (Note 15)	(–3dBFS)	LVCM0 bit = "0"	1.44	1.60	1.76	Vpp
		LVCM0 bit = "1"	1.82	2.00	2.22	Vpp
S/(N+D) (–3dBFS)			75	85	-	dBFS
S/N (A-weighted)			82	92	-	dB
Interchannel Isolation			85	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	80	-	dB
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, DVOL=OVOL =0dB, R_L=8Ω, BTL						
Output Voltage (AK4958EG)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
S/(N+D) (AK4958EG)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	65	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			20	60	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
S/N (AK4958EG) SPKG1-0 bits = "01", –0.5dBFS (Po=250mW) (A-weighted)			80	90	-	dB
Output Voltage (AK4958ECB)			-	-	-	
SPKG1-0 bits = "00", –0.7dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.7dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.85dBFS (Po=400mW)			-	1.79	-	Vrms
S/(N+D) (AK4958ECB)						
SPKG1-0 bits = "00", –0.7dBFS (Po=150mW)			-	65	-	dB
SPKG1-0 bits = "01", –0.7dBFS (Po=250mW)			20	60	-	dB
SPKG1-0 bits = "10", –0.85dBFS (Po=400mW)			-	20	-	dB
S/N (AK4958ECB) SPKG1-0 bits = "01", –0.7dBFS (Po=250mW) (A-weighted)			80	90	-	dB
Load Resistance			6.8	-	-	Ω
Load Capacitance			-	-	100	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	60	-	dB

Note 15. The output voltage does not track the AVDD.

Parameter			min	typ	max	Unit
BEEP Input: BEEP pin, Internal Resistance Mode (PMBP bit =“1”, BPM bit = “0”, BPVCM bit = “0”, BPLVL3-0 bits = “0000”)						
Input Resistance			46	66	86	kΩ
Maximum Input Voltage (Note 16)			-	-	1.54	Vpp
Gain						
	MIN → LOUT	LVCM1-0 bits = “00”	–1	0	+1	dB
		LVCM1-0 bits = “01”	-	+2.0	-	dB
		LVCM1-0 bits = “10”	-	+2.0	-	dB
		LVCM1-0 bits = “11”	-	+4.0	-	dB
	MIN → SPP/SPN (Note 17)					
		ALC2 bit = “0”, SPKG1-0 bits = “00”	+4.4	+6.4	+8.4	dB
		ALC2 bit = “0”, SPKG1-0 bits = “01”	-	+8.4	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “10”	-	+11.1	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “11”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “00”	-	+8.4	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “01”	-	+10.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “10”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “11”	-	+15.1	-	dB
BEEP Input: BEEP pin, External Resistance mode (PMBP bit =“1”, BPM bit = “1”, BPVCM bit = “0”, BPLVL3-0 bits = “0000”), External Input Resistance= 66kΩ						
Maximum Input Voltage			-	-	1.54	Vpp
Gain (Note 18)						
	BEEP → LOUT	LVCM1-0 bits = “00”	–4.5	0	+4.5	dB
		LVCM1-0 bits = “01”	-	+2.0	-	dB
		LVCM1-0 bits = “10”	-	+2.0	-	dB
		LVCM1-0 bits = “11”	-	+4.0	-	dB
	BEEP → SPP/SPN					
		ALC2 bit = “0”, SPKG1-0 bits = “00”	+1.9	+6.4	+10.9	dB
		ALC2 bit = “0”, SPKG1-0 bits = “01”	-	+8.4	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “10”	-	+11.1	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “11”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “00”	-	+8.4	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “01”	-	+10.4	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “10”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “11”	-	+15.1	-	dB

Note 16. The maximum value is AVDD Vpp when BPVCM bit = “1”. However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

Note 17. These are the ideal values with no load resistance. When an 8Ω is connected the value degrades about 0.4dB for the AK4958EG and about 0.2dB for the AK4958ECB.

Note 18. The gain is in inverse proportion to external input resistance.

Parameter		min	typ	max	Unit
Video Signal Input					
External Resistor (Note 20)	R1 (Figure 3)	0.075	-	1.6	kΩ
External Capacitor	C1 (Figure 3)	0.02	0.047	0.2	μF
Maximum Input Voltage: VG1-0 bits = "10" (+12dB)		-	0.6	-	Vpp
Pull Down Current		-	0.125	-	μA
Video Analog Output (Figure 4)					
Output Gain fin =100kHz Sine wave Input (Note 19)	VG1-0 bits = "10", 0.5Vpp Input	11.5	12.0	12.5	dB
	VG1-0 bits = "11", 0.3Vpp Input	16.0	16.5	17.0	
Clamp Level (Note 19)		-	50	100	mV
S/N (Note 21) VG1-0 bits = "10"(+12dB)	BW = 100kH ~ 6MHz, S = 0.35Vpp Input	60	67	-	dB
Maximum Output Voltage (Note 19)	fin =100kHz (Sine wave)	2.54	-	-	Vpp
Secondary Harmonic Distortion VG1-0 bits = "10"(+12dB) fin = 3.58MHz	430mVpp: –20 ~ 100IRE, Sine Wave Input (Flat Field = 100 IRE Burst = –20IRE)	-	–45	–35	dB
Load Resistance		140	150	-	Ω
Load Capacitance	C2 (Figure 4)	-	-	15	pF
	C3 (Figure 4)	-	-	400	pF
PSRR (Note 22) VG1-0 bits = "10"(+12dB)	fin = 10kHz	-	45	-	dB
	fin = 100kHz	-	30	-	dB
LPF for VIN signal : (Note 19)					
Frequency Response (fin = 100kHz, 0.5Vpp, Sine wave Input), C2=15pF, C3=400pF					
	Response at 6.75MHz	–3.0	–0.5	+2.0	dB
	Response at 27MHz	-	–47	–20	
Group Delay	|GD3MHz–GD6MHz|	-	15	100	ns

Note 19. This is a value at measurement point in Figure 4. 0.5Vpp input is the value when VG1-0 bit ="10"(+12dB). Input amplitude is in inverse proportion to the gain. S/N and Secondary Harmonic Distortion values are measured at measuring point 2.

Note 20. PMV bit must be set to "0" if the resistor value exceeds the range from 0.075 to 1.6kΩ in case of the input signal is stopped or the input circuit of the VIN pin is powered down.

Note 21. S/N = 20xlog (Output Voltage[Vpp]/Noise Level[Vrms]). Output Voltage = 0.7 [Vpp].

Note 22. PSRR is applied to AVDD with 500mVpp sine wave when DC level of -20IRE, 0IRE and 100IRE are input to the VIN pin.

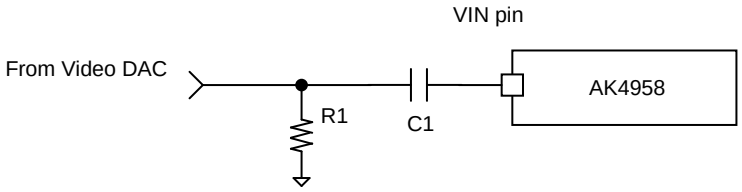


Figure 3. External Resistor of Video Signal Input pin

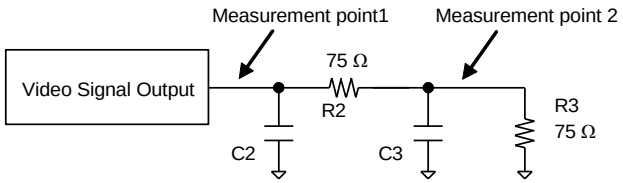


Figure 4. Load Capacitance C2 and C3

Parameter		min	typ	max	Unit
Power Supplies:					
Power Up (PDN pin = "H")					
All Circuit Power-up (Note 23)					
	AVDD	-	10.5	15	mA
	DVDD +TVDD	-	2.8	4.2	mA
MIC + ADC (Note 24)					
	AVDD	-	2.5	-	mA
	DVDD +TVDD	-	0.9	-	mA
DAC + Lineout (Note 25)					
	AVDD	-	2.2	-	mA
	DVDD +TVDD	-	0.7	-	mA
DAC + SPK-Amp (Note 26)					
	AVDD	-	3.3	-	mA
	DVDD +TVDD	-	0.7	-	mA
Video Block (Note 27)					
	AVDD	-	5.3	-	mA
Power Down (PDN pin = "L") (Note 28)					
AVDD+DVDD+TVDD		-	1	5	μA

Note 23. When PMADL=PMADR=PMDAC=PMPFIL=PMLO=PMSPK=PMPLL=MCKO=PMBP=PMMP =PMMICR =PMMICL =M/S =PMV bits = "1", SPK-amp No load, no signals are input to LIN/RIN and BEEP pins, black signal is input to the VIN pin, no output from the LOUT/ROUT pin and "0" data input to the SDTI pin in PLL Master Mode (MCKI=13.5MHz, FS3-0 bits = "1011"). In this case, the output current of the MPWR pin is 0mA. The path settings are, BRDAC= ADCPF = PFSDO bits = "1", PFDAC bit= "0", DACS = DACL bits = "1", and BEEPS = BEEPL bits = "0". MG2-0 bits = "000", HPF = LPF = FIL3 = EQ0 = EQ1~5 = ALC1~2 bits = "0", MONO1-0 bits = "00", DVOL7-0 bits = "C0H", and SMUTE bit = "0".

Note 24. When PMADL = PMADR = PMMICL = PMMICLR bits = "1" and no signals are input to the LIN/RIN pin in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"). The path setting is ADCPF=PFSDO bits = "0".

Note 25. When PMDAC = PMLO = "1", "0" data input to the SDTI pin, and no output from the LOUT/ROUT pin in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"). The path settings are BRDAC= PFDAC bit = "0", DACL bit = "1", and DACS =BEEPS =BEEPL bits = "0". MONO1-0 bits = "00", DVOL7-0 bits = "0CH", and SMUTE bit = "0".

Note 26. When PMDAC = PMSPK =SPPSN bits = "1", "0" data input to the SDTI pin, and No load at SPK-amp in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"). The path settings are MONO1-0 bits= "00", DVOL7-0 bits "C0H", and SMUTE bit = "0".

Note 27. When PMV bit = "1", No-load, and the black signal is input to the VIN pin.

Note 28. Digital input pins (MCKI, LRCK, BICK, SDTI, CSN/SDA, CCLK/SCL, CDTIO/CAD0, I2C pins) are fixed to TVDD (AK4958EG), DTVDD(AK4958ECB) or VSS2, and the I2C pin is fixed to AVDD or VSS.

FILTER CHARACTERISTICS

(Ta =25°C; fs=48kHz; AK4958EG: AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V, AK4958ECB: AVDD=2.8 ~ 3.6V, DTVDD = 1.6 ~ 2.0V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 29)	±0.16dB	PB	0	-	18.8	kHz
	–0.66dB		-	21.1	-	kHz
	–1.1dB		-	21.7	-	kHz
	–6.9dB		-	24.1	-	kHz
Stopband (Note 29)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 30)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response (Note 29)	–3.0dB	FR	-	3.7	-	Hz
	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 29)	±0.05dB	PB	0	-	21.8	kHz
	–6.0dB		-	24	-	kHz
Stopband (Note 29)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 30)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 29. The passband and stopband frequencies scale with fs (sampling frequency). Each response refers to that of 1kHz. For example, it is 0.454 x fs (ADC) when PB=21.7kHz (@–1.1dB).

Note 30. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (1st order HPF + 1st order LPF + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta =25°C; fs=48kHz, AK4958EG: AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V; AK4958ECB: AVDD=2.8~3.6V, DTVDD= 1.6~2.0V)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage					
(Except I2C pin, TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
(Except I2C pin, TVDD < 2.2V)	VIH	80%TVDD	-	-	V
(I2C pin)	VIH1	70%AVDD	-	-	V
Low-Level Input Voltage					
(Except I2C pin, TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
(Except I2C pin, TVDD < 2.2V)	VIL	-	-	20%TVDD	V
(I2C pin)	VIL1	-	-	30%AVDD	V
Input Leakage Current	Iin1	-	-	±10	µA
Audio Interface & Serial µP Interface (CDTIO, SDA MCKO, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital Microphone Interface (DMDAT pin Input ; DMIC bit = "1")					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Input Leakage Current	Iin2	-	-	±10	µA
Digital Microphone Interface (DMCLK pin Output ; DMIC bit = "1")					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V

Note 31. TVDD means DTVDD for the AK4958ECB.

Note 32. The external pull-up resistors at the SDA and SCL pins should be connected to the voltage that is TVDD (DTVDD) or more and 6V or less.

SWITCHING CHARACTERISTICS

(Ta =25°C; fs=48kHz; C_L=20pF; AK4958ECB: AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V, AK4958ECB: AVDD=2.8 ~ 3.6V, DTVDD = 1.6 ~ 2.0V)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = "0100"	fCLK	-	11.2896	27	MHz
	PLL3-0 bits = "0110"	fCLK	-	12	-	MHz
	PLL3-0 bits = "0111"	fCLK	-	24	-	MHz
	PLL3-0 bits = "1100"	fCLK	-	13.5	-	MHz
	PLL3-0 bits = "1101"	fCLK	-	27	-	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
MCKO Output Timing						
Frequency	PS1-0 bits = "00"	fMCK	-	256fs	-	Hz
	PS1-0 bits = "01"	fMCK	-	128fs	-	Hz
	PS1-0 bits = "10"	fMCK	-	64fs	-	Hz
	PS1-0 bits = "11" (Note 33)	fMCK	-	512fs	-	Hz
Duty Cycle		dMCK	40	50	60	%
LRCK Output Timing						
Frequency		fs	-	Table 6	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	32fs	-	Hz
	BCKO bit = "1"	tBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
MCKO Output Timing						
Frequency	PS1-0 bits = "00"	fMCK	-	256fs	-	Hz
	PS1-0 bits = "01"	fMCK	-	128fs	-	Hz
	PS1-0 bits = "10"	fMCK	-	64fs	-	Hz
	PS1-0 bits = "11" (Note 33)	fMCK	-	512fs	-	Hz
Duty Cycle		dMCK	40	50	60	%
LRCK Input Timing						
Frequency		fs	-	Table 6	-	Hz
Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Frequency		tBCK	32fs	-	64fs	Hz
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

Note 33. When MCKO=512fs, fs=8, 11.025, 12, 16, 32kHz are not available.

Parameter			Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)							
LRCK Input Timing							
	Frequency	PLL3-0 bits = "0010"	fs	-	fBCK/32	-	Hz
		PLL3-0 bits = "0011"	fs	-	fBCK/64	-	Hz
	Duty		Duty	45	-	55	%
BICK Input Timing							
	Frequency	PLL3-0 bits = "0010"	tBCK	0.2352	-	1.536	MHz
		PLL3-0 bits = "0011"	tBCK	0.4704	-	3.072	MHz
	Pulse Width Low		tBCKL	0.4/tBCK	-	-	s
	Pulse Width High		tBCKH	0.4/tBCK	-	-	s
External Slave Mode							
MCKI Input Timing							
	Frequency	FS1-0 bits = "00"	fCLK	-	256fs	-	Hz
		FS1-0 bits = "01"	fCLK	-	1024fs	-	Hz
		FS1-0 bits = "10" or "11"	fCLK	-	512fs	-	Hz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
	Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing							
	Frequency	FS1-0 bits = "00"	fs	7.35	-	48	kHz
		FS1-0 bits = "01"	fs	7.35	-	13	kHz
		FS1-0 bits = "10"	fs	7.35	-	24	kHz
		FS1-0 bits = "00"	fs	7.35	-	48	kHz
	Duty		Duty	45	-	55	%
BICK Input Timing							
	Frequency		tBCK	32fs	-	64fs	Hz
	Pulse Width Low		tBCKL	130	-	-	ns
	Pulse Width High		tBCKH	130	-	-	ns
External Master Mode							
MCKI Input Timing							
	Frequency	256fs (FS1-0 bits = "00")	fCLK	1.8816	-	12.288	MHz
		512fs (FS1-0 bits = "10")	fCLK	3.7632	-	13.312	MHz
		512fs (FS1-0 bits = "11")	fCLK	3.7632	-	24.576	MHz
		1024fs (FS1-0 bits = "01")	fCLK	7.5264	-	13.312	MHz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
	Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing							
	Frequency	FS1-0 bits = "00"	fs	-	fCLK/256	-	kHz
		FS1-0 bits = "01"	fs	-	fCLK/1024	-	kHz
		FS1-0 bits = "10" or "11"	fs	-	fCLK/512	-	kHz
	Duty Cycle		Duty	-	50	-	%
BICK Output Timing							
	Frequency	BCKO bit = "0"	tBCK	-	32fs	-	Hz
		BCKO bit = "1"	tBCK	-	64fs	-	Hz
	Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 34)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 34)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 34)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Mode) (Note 35)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 36)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 36)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 38)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 39)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 34. BICK rising edge must not occur at the same time as LRCK edge.
Note 35. The AK4958ECB does not support 3-wire Mode.
Note 36. CCLK rising edge must not occur at the same time as CSN edge.
Note 37. I²C-bus is a trademark of NXP B.V.
Note 38. It is the time of 10% potential change of the CDTIO pin when R_L=1kΩ (pull-up or TVDD).
Note 39. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

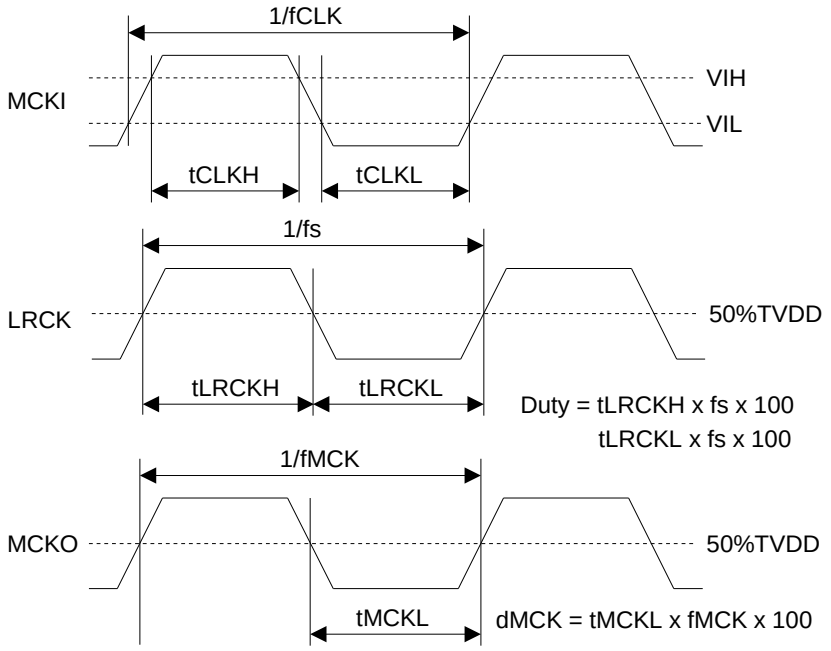
Parameter		Symbol	min	typ	max	Unit
Digital Audio Interface Timing; C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	s
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tDSDS	50	-	-	ns
DMDAT Hold Time		tDSDH	0	-	-	ns
Power-down & Reset Timing						
PDN Accept Pulse Width	(Note 40)	tAPD	200	-	-	ns
PDN Reject Pulse Width	(Note 40)	tRPD	-	-	50	ns
PMADL or PMADR "↑" to SDTO valid	(Note 41)					
ADRST1-0 bits ="00"		tPDV	-	1059	-	1/fs
ADRST1-0 bits ="01"		tPDV	-	267	-	1/fs
ADRST1-0 bits ="10"		tPDV	-	531	-	1/fs
ADRST1-0 bits ="11"		tPDV	-	135	-	1/fs
VCOM Voltage						
Rising Time	(Note 42)	tRVCM	-	0.6	2.0	ms

Note 40. The AK4958 can be reset by the PDN pin = "L". The PDN pin must be held "L" for more than 200ns for a certain reset. The AK4958 is not reset by the "L" pulse less than 50ns.

Note 41. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

Note 42. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2μF and the REGFIL pin is 2.2μF. The capacitance variation should be ±50%.

■ Timing Diagram



Note 43. MCKO is not available at EXT Master mode.
Figure 5. Clock Timing (PLL/EXT Master mode)

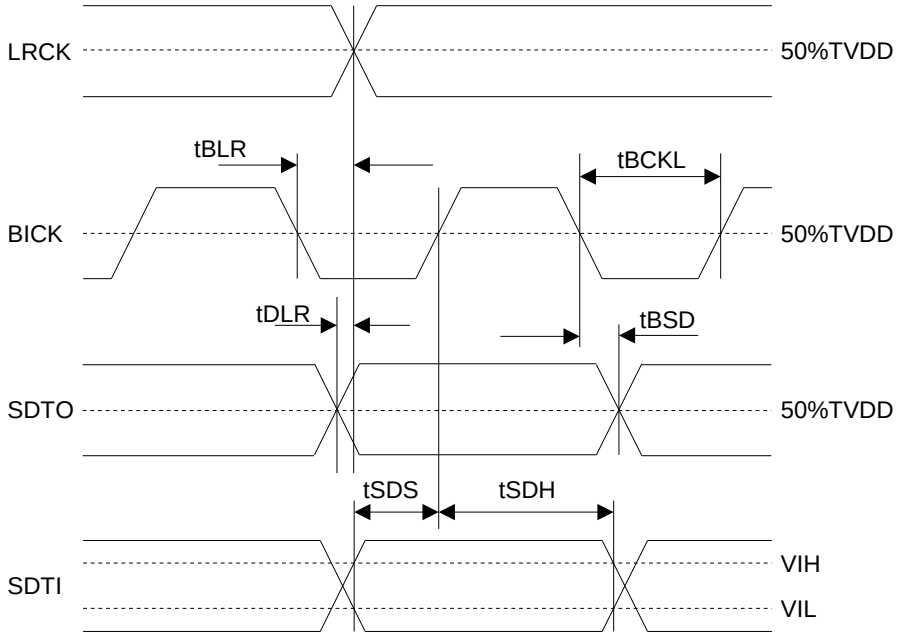


Figure 6. Audio Interface Timing (PLL/EXT Master mode)

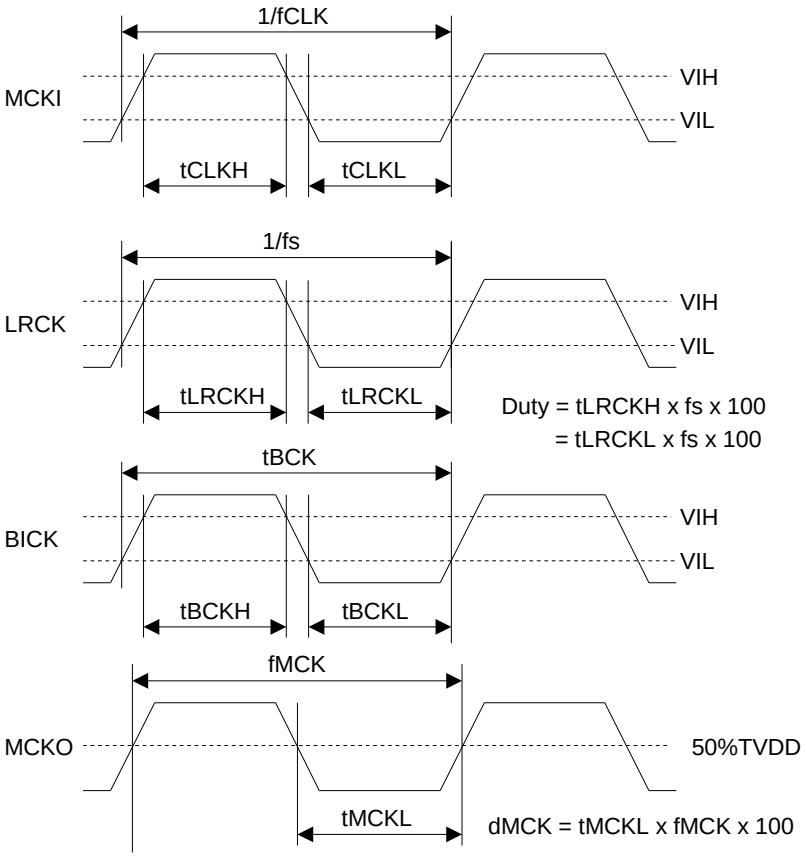


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

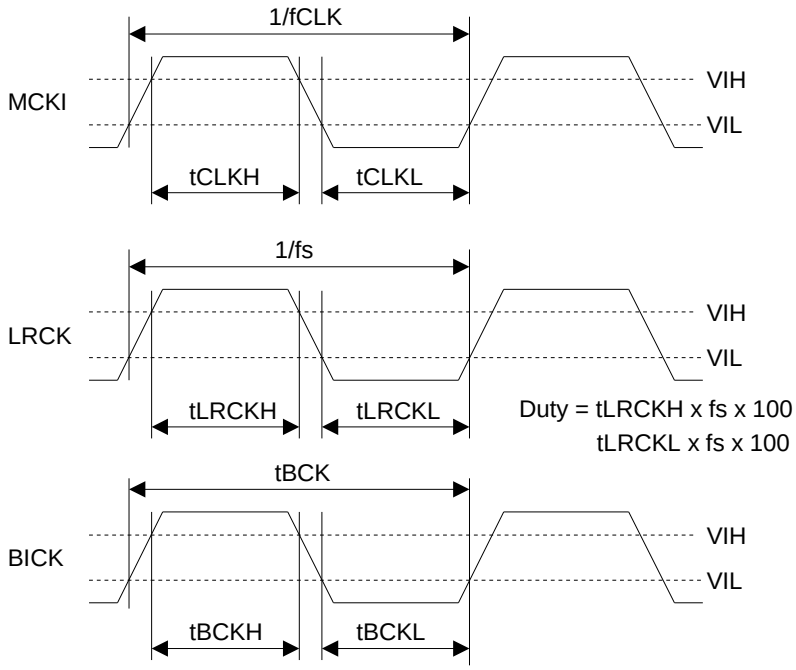


Figure 8. Clock Timing (EXT Slave mode)

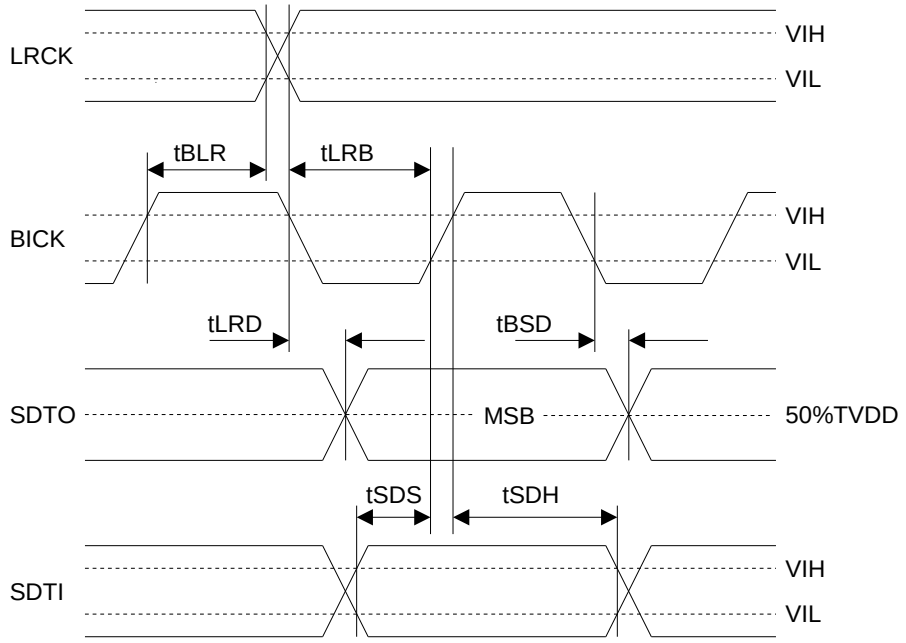


Figure 9. Audio Interface Timing (PLL/EXT Slave mode)

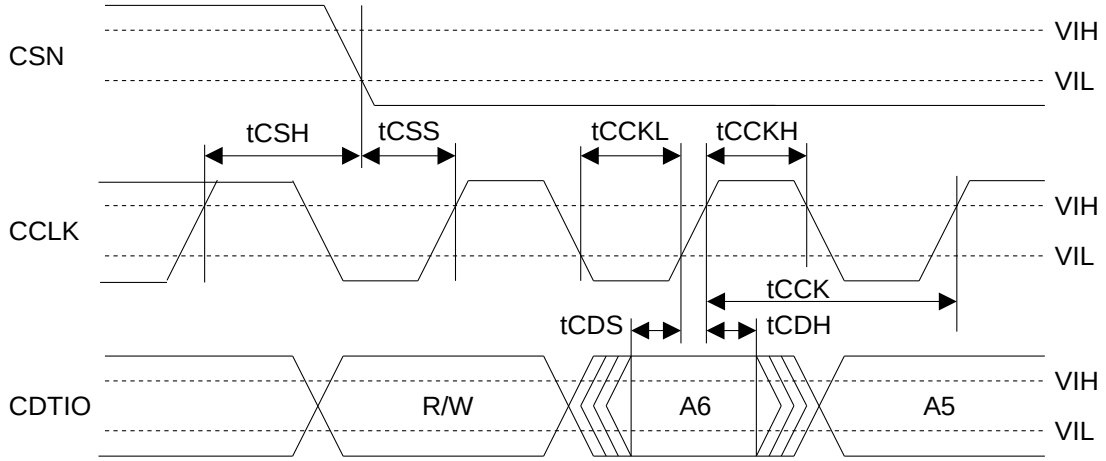


Figure 10. WRITE Command Input Timing

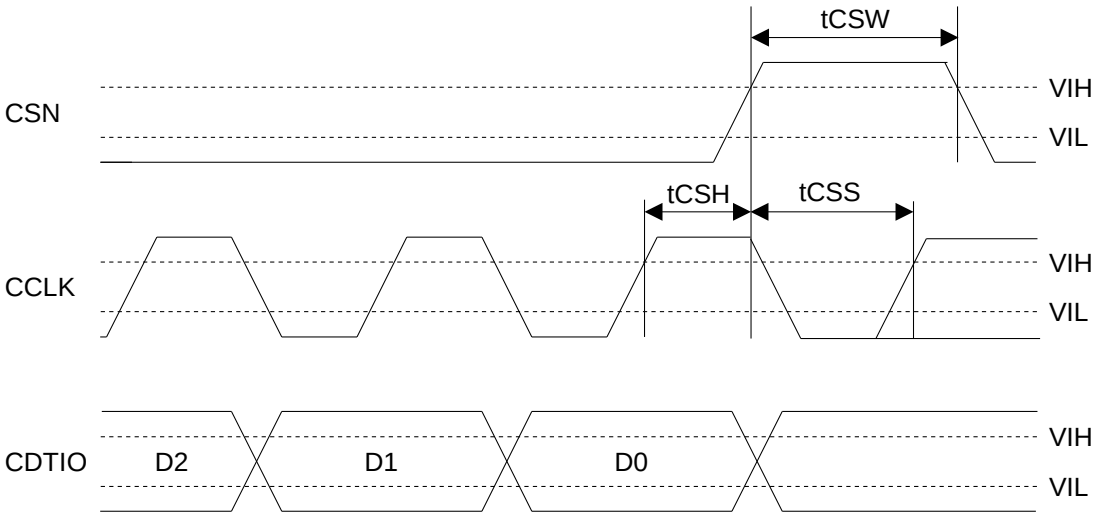


Figure 11. WRITE Data Input Timing

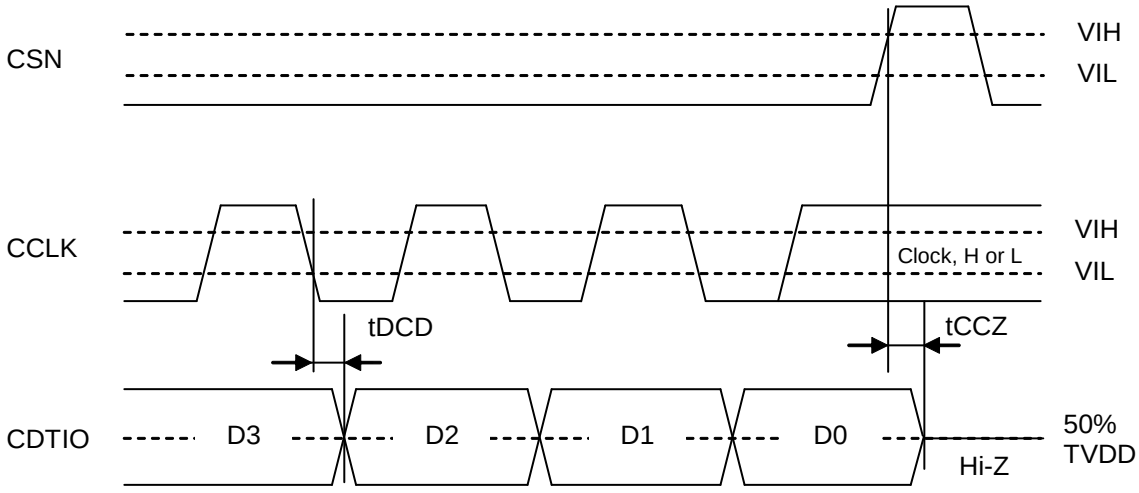


Figure 12. Read Data Output Timing

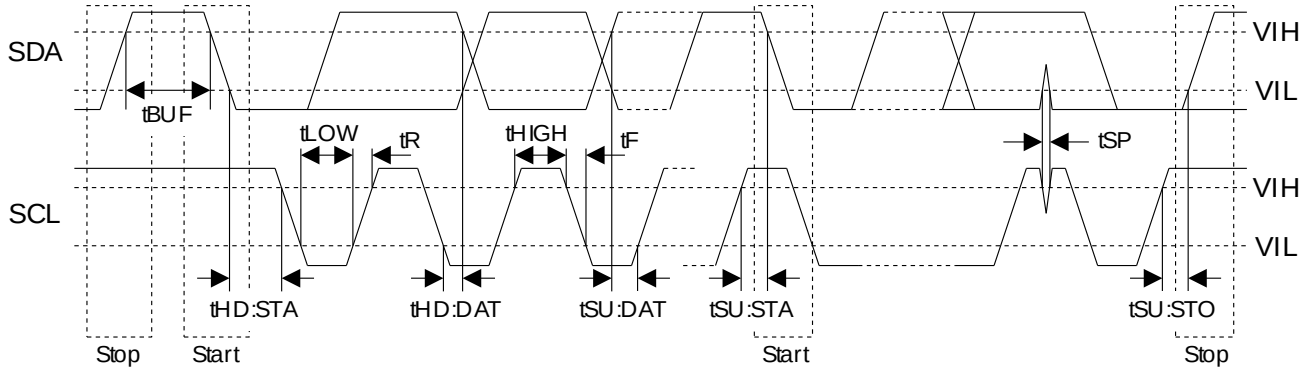
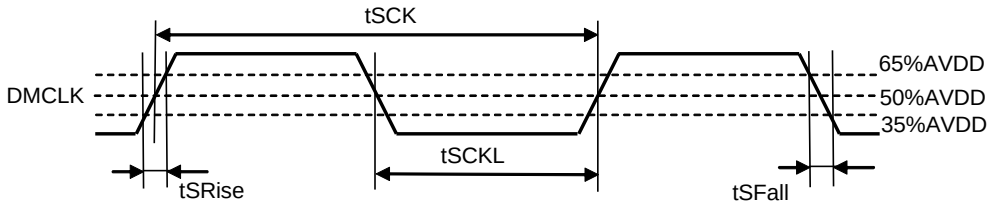


Figure 13. I^{2}C Bus Mode Timing



dSCK = 100 x tSCKL / tSCK

Figure 14. DMCLK Clock Timing

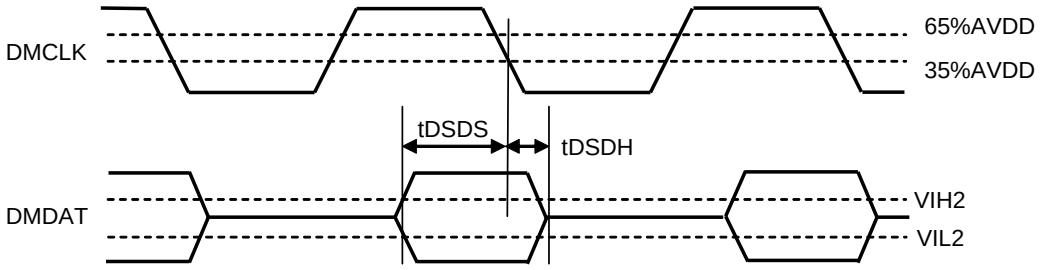


Figure 15. Audio Interface Timing (DCLKP bit = "1")

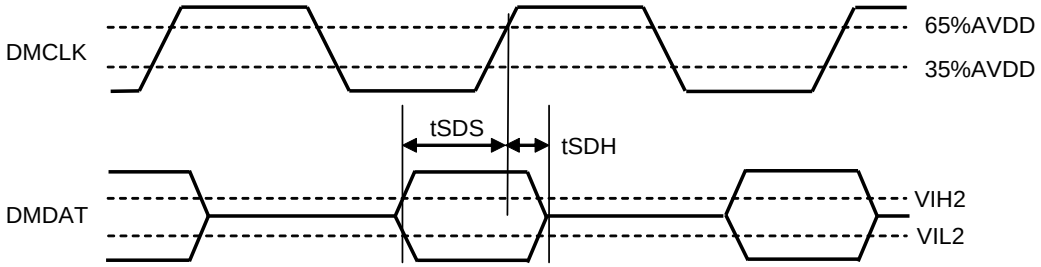


Figure 16. Audio Interface Timing (DCLKP bit = "0")

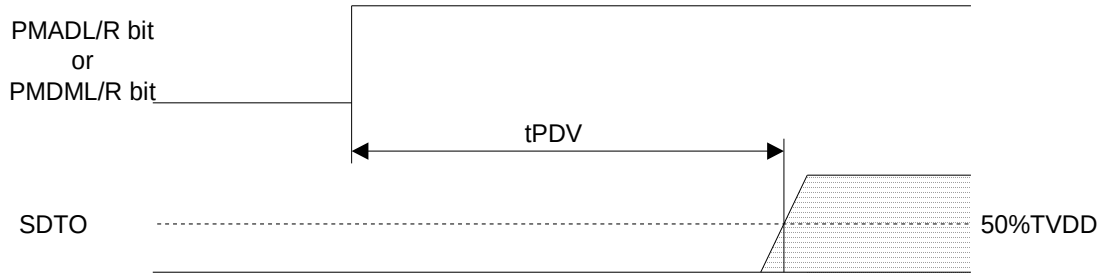


Figure 17. Power Down & Reset Timing 1

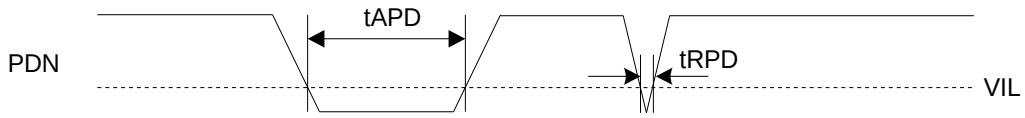


Figure 18. Power Down & Reset Timing 2

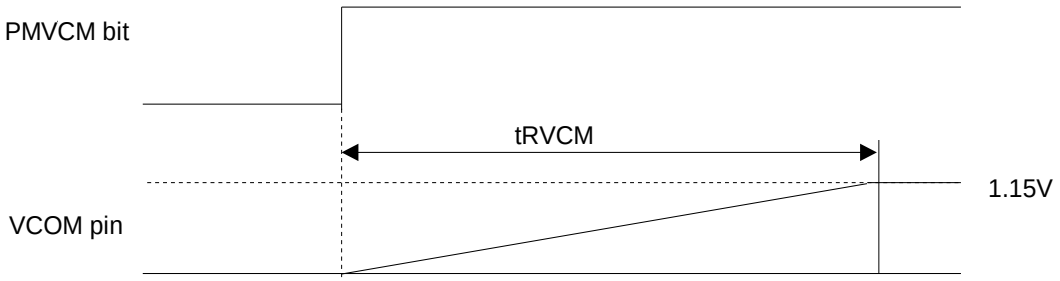
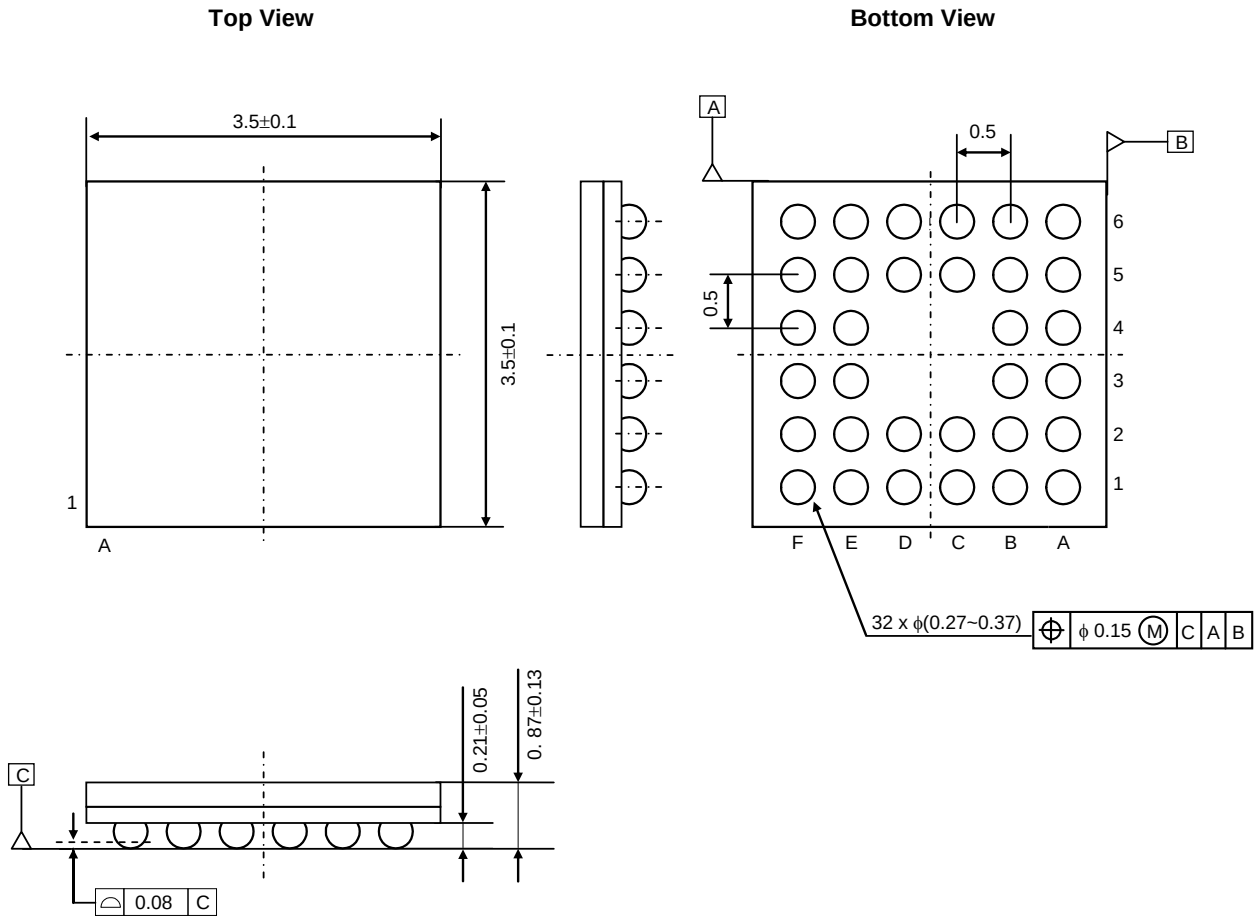


Figure 19. VCOM Rising Timing

PACKAGE (AK4958EG)

32pin BGA (Unit: mm)

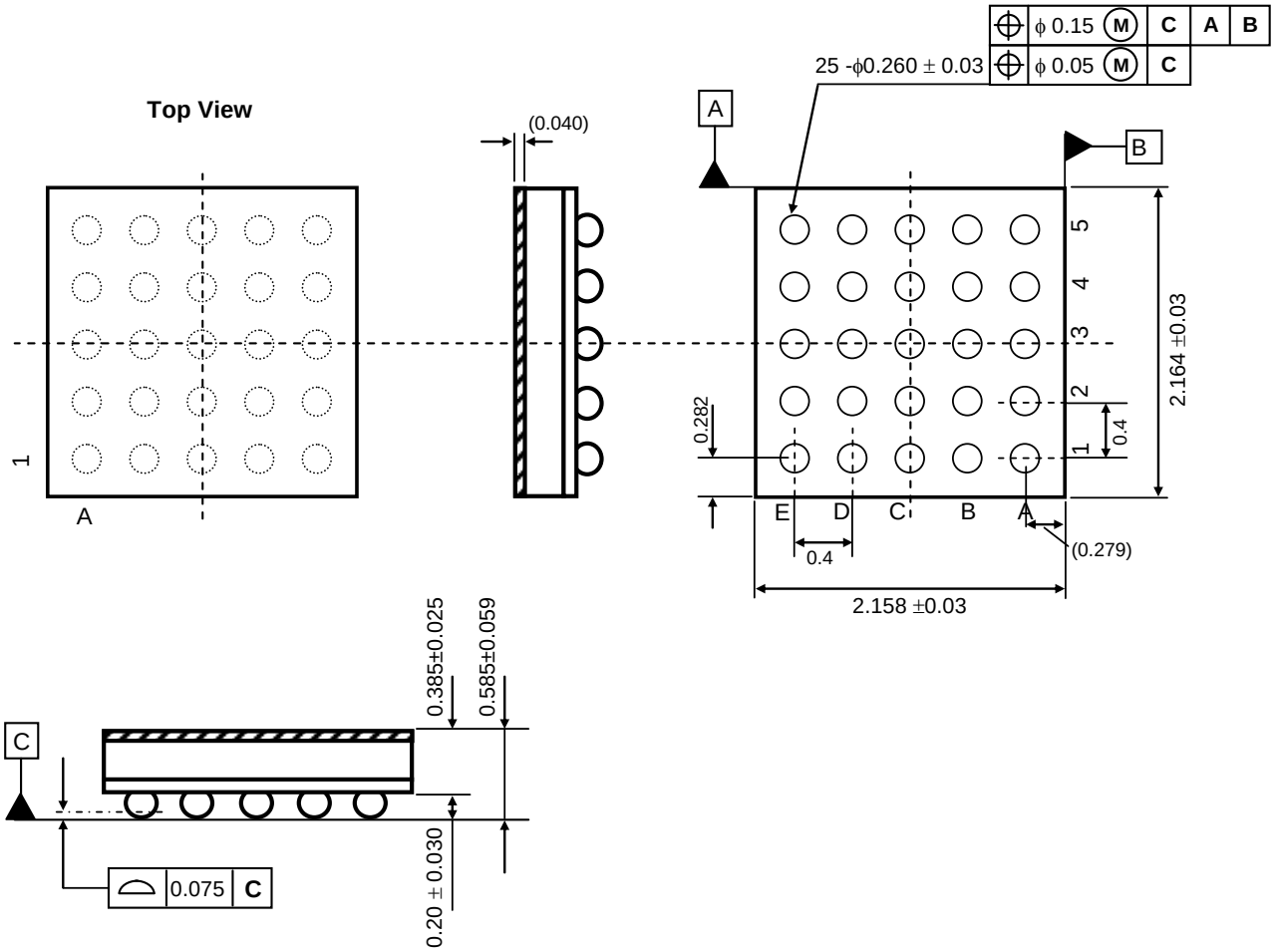


■ Material & Lead finish

Package material: Epoxy Resin, Halogen (Br and Cl) free
Solder ball material: SnAgCuNi (LF35)

PACKAGE (AK4958ECB)

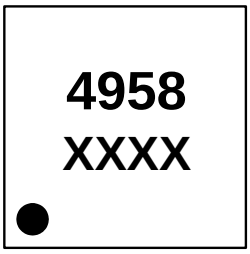
25pin CSP (Unit: mm)



■ Material & Lead finish

Package material: Polyimide Resin, Halogen (Br and Cl) free
Solder ball material: SnAgCu

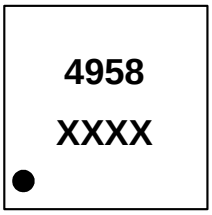
MARKING (AK4958EG)



A1

XXXX: Date code (4 digit)
Pin #A1 indication

MARKING (AK4958ECB)



A1

XXXX: Date code (4 digit)
Pin #A1 indication

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page/Line	Contents
13/09/13	00	First Edition		
13/10/25	01	Error Correction	31	Package dimension was corrected. (AK4958EG) Stand off: 0.16±0.5 → 0.21±0.05 Total thickness: Max 1 → 0.87±0.13

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